GC02M2 CSP

1/5’’2Mega CMOS Image Sensor

Datasheet

V1.0

2020-09-07

Ordering Information

◆ **GC02M2-C24Y0**

(Colored , 24 PIN-CSP)

◆ **GC02M2-C24YA**

(Colored , 24 PIN-CSP)

**Please contact Galaxycore sales representative for details*

GENERATION REVISION HISTORY

Version.	Effective Date	Description of Changes	Prepared by
V1.0	2020-09-07	Document Release	AE Dept.

Galaxycore Incorporation

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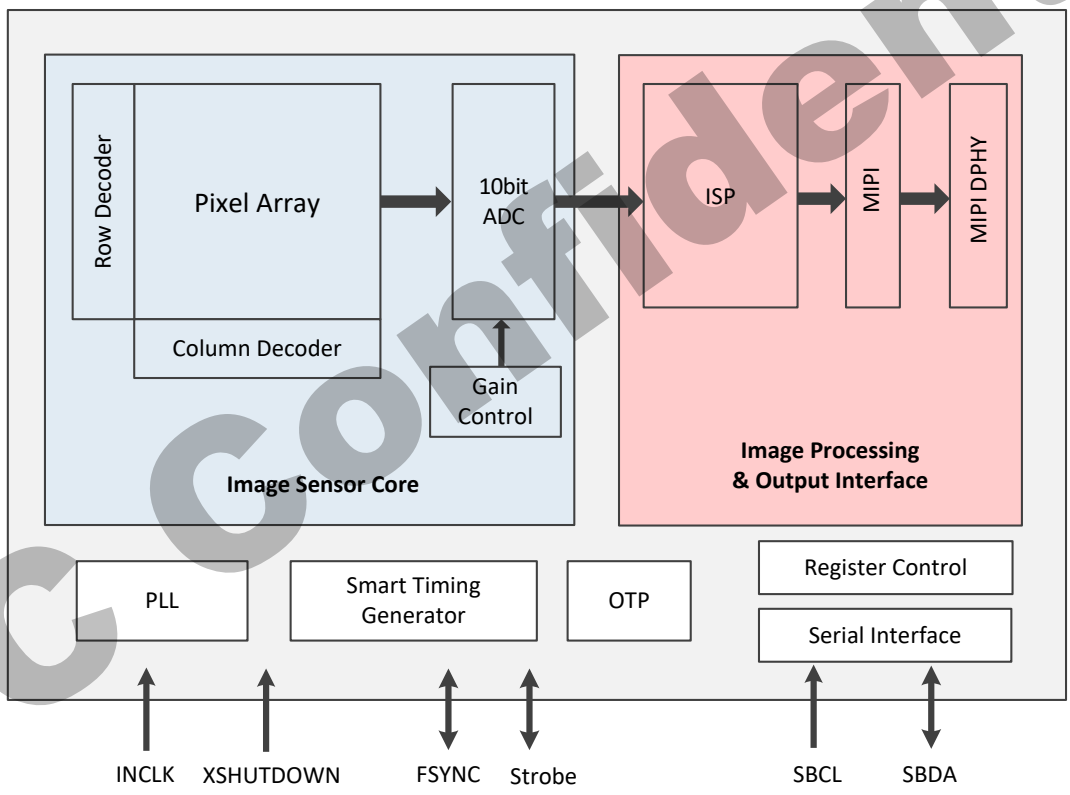
1. Sensor Overview

1.1 General Description

GC02M2 is a high quality 2Mega CMOS image sensor, for mobile phone camera applications and digital camera products. GC02M2 incorporates a 1612H x 1212V active pixel array, on-chip 10-bit ADC, and image signal processor. It is programmable through a simple two-wire serial interface and has very low power consumption. It provides RAW10 and RAW8 data formats with MIPI interface.

Figure 1: Block Diagram



1.2 Features

- Optical size: 1/5 inch
- Pixel size: 1.75um x 1.75um FSI
- Active pixel array: 1600x1200
- Color Filter: Bayer
- Output formats: Raw 10bit/8bit
- Power supply requirement: AVDD28: 2.7~3V (2.8V)
  DVDD: 1.7~1.9V (1.8V)
  IOVDD: 1.7~3.0V (1.8V)
- Power Consumption: TBD mW
- Frame rate: 30fps@UXGA
  30fps@HD 720P
  60fps@SVGA
- MIPI 1-lane
- PLL support
- Frame sync support (master/slave mode)
- Strobe support
- Windowing support
- Image Flip : Horizontal/Vertical mirror
- Operation Temperature: -20~70℃
- Analog Gain: 10x
- OTP support(136bits for customers) : module information/WB/etc.
- Package: CSP

2. Electrical Characteristics

2.1 Absolute maximum rating

Table 1: Absolute maximum rating

Description	Symbol	Min.	Unit	Note
Analogue absolute max	V_{AVDD_MAX}	3	V	Refer to GND level
Digital absolute voltages	V_{DVDD_MAX}	1.9	V	
IO absolute max	V_{IOVDD_MAX}	3	V	
Digital input voltages	V_{IO_MAX}	3	V	
Storage temperature	T_{STR}	-40 ~ +85	℃	℃

Note: Digital input voltage: INCLK, SBCL, SBDA, XSHUTDOWN, FSYNC

2.2 Operation conditions

Table 2: Operation conditions

Description	Symbol	Min.	Typical	max	Unit
Analog power supply	V_{AVDD}	2.7	2.8	3.0	V
Digital power supply	V_{DVDD}	1.7	1.8	1.9	V
IO power supply	V_{IOVDD}	1.7	1.8	3.0	V
Digital input voltages	V_{IP}	0		IOVDD	V
Test temperature	T_{TEST}	21	25	27	℃
Operating temperature	T_{OPR}	-20		70	℃
performance temperature	T_{SEPC}	0		60	℃

Note: 1. Digital input voltage: INCLK, SBCL, SBDA, XSHUTDOWN, FSYNC

2. Test temperature: image quality test condition

2.3 DC characteristics

Table 3: DC Characteristics

(V_{DVDD}=1.8V, V_{AVDD}=2.8V, V_{IP}=1.8V, T_j=60℃)

Characteristics	Symbol	Condition	Min.	Typical	max	Unit
Input voltage	V_{IH}	-	0.7 x V_{IP}	-	-	V
	V_{IL}	-	-	-	0.3 x V_{IP}	V
Input leakage current	I_{IL}	V_{IN}=V_{IP} or VSS	-10	-	10	μA
High level output voltage	V_{OH}	I_{OH} = -100μA	0.7 x VIO	-	-	V
Low level output voltage	V_{OL}	I_{OL} = 100μA	-	-	0.3 x V_{IO}	V
High-Z output leakage current	I_{OZ}	V_{out}=DVDD or VSS	-10	-	10	μA

Note: 1. Input voltage apply to INCLK, SBCL, SBDA, XSHUTDOWN,FSYNC

2. High-Z output apply to SBCL, SBDA , MIPI output pins when in High-Z state

2.4 AC Characteristics

Figure 2: input clock wave diagram

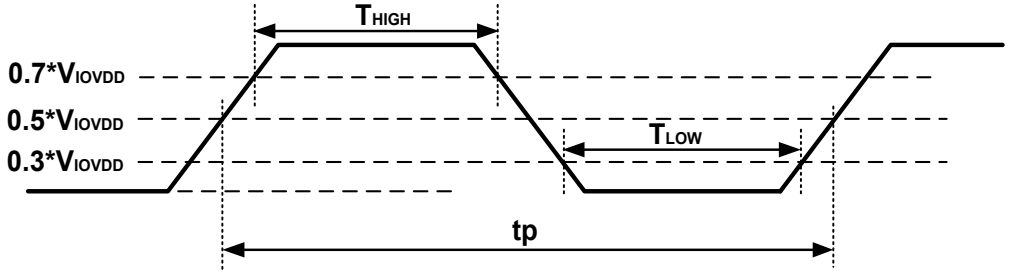


Table 4: AC Characteristics

Item	Symbol	Min.	Typ.	max	unit
Frequency	f_{SCK}	6	24	27	MHz
jitter (period, peak-to-peak)	T_{jitter}			600	ps
High level width	T_{HIGH}	0.4tp		0.6tp	ns
Low level width	T_{LOW}	0.4tp		0.6tp	ns
Duty Cycle	f_{DUTY}	40		60	%

2.5 Power consumption

Table 5: power consumption

Item	Symbol	Min	Typ	Max	Unit
UXGA@30fps	I_{AVDD}	-	TBD	TBD	mA
	I_{DVDD}	-	TBD	TBD	mA
	I_{IOVDD}	-	TBD	TBD	mA
720P@30fps	I_{AVDD}	-	TBD	-	mA
	I_{DVDD}	-	TBD	-	mA
	I_{IOVDD}	-	TBD	-	mA
SVGA@60fps	I_{AVDD}	-	TBD	-	mA
	I_{DVDD}	-	TBD	-	mA
	I_{IOVDD}	-	TBD	-	mA
Standby current	I_{AVDD}	-	TBD	TBD	μA
	I_{DVDD}	-	TBD	TBD	μA
	I_{IOVDD}	-	TBD	TBD	μA
Power off current	I_{total}	-	-	0	μA

Note: 1. All operate current are measured at 24MHz INCLK.

2. Standby current is measured at XSHUTDOWN = L.

3. We recommend that power should be turned off, when lower power consumption is required.

3. Package Specifications

Figure 3: Package diagram

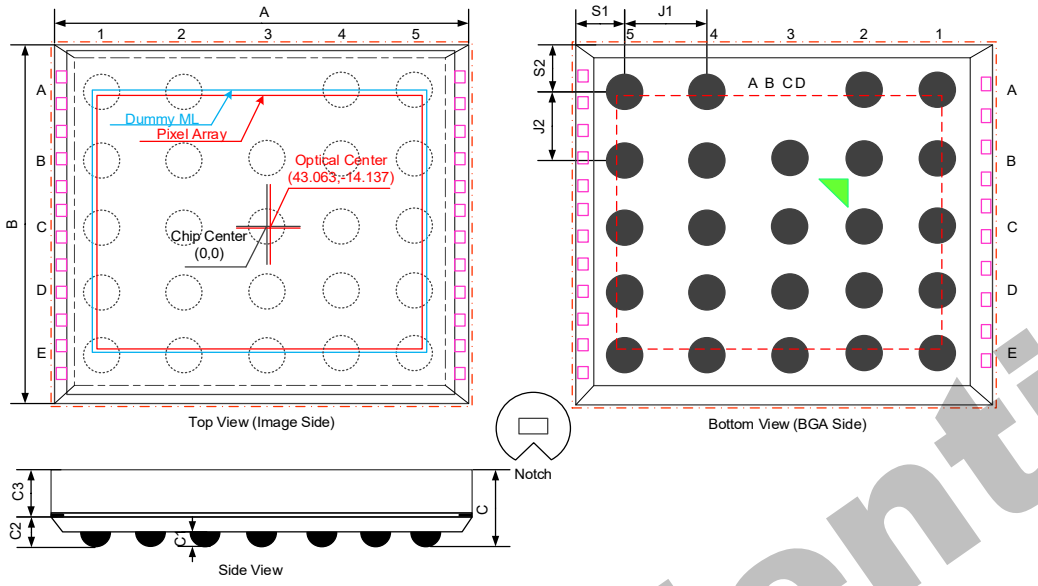


Table 6: package dimension

Description	Symbol	Nominal	Min.	Max.
		Millimeters		
Package Body Dimension X	A	3.6070	3.5820	3.6320
Package Body Dimension Y	B	3.0150	2.9900	3.0400
Package Height	C	0.7400	0.6850	0.7950
Ball Height	C1	0.1300	0.1000	0.1600
Thickness from ball to wafer surface	C2	0.2950	0.2550	DI
Thickness from top glass surface to wafer	C3	0.4450	0.4300	DI
Ball Diameter	D	0.2500	0.2200	0.2800
Total Ball Count	N	24(1NC)	/	/
Ball Count X axis	N1	5	/	/
Ball Count Y axis	N2	5	/	/
Pins Pitch X axis1	J1	0.6700	0.6600	0.6800
Pins Pitch Y axis1	J2	0.5300	0.5200	0.5400
Edge to Ball Center Distance along X	S1	0.4635	0.4335	0.4935
Edge to Ball Center Distance along Y	S2	0.4475	0.4175	0.4775

3.1 Bonding Diagram

Figure 4: Bonding diagram (Top view)

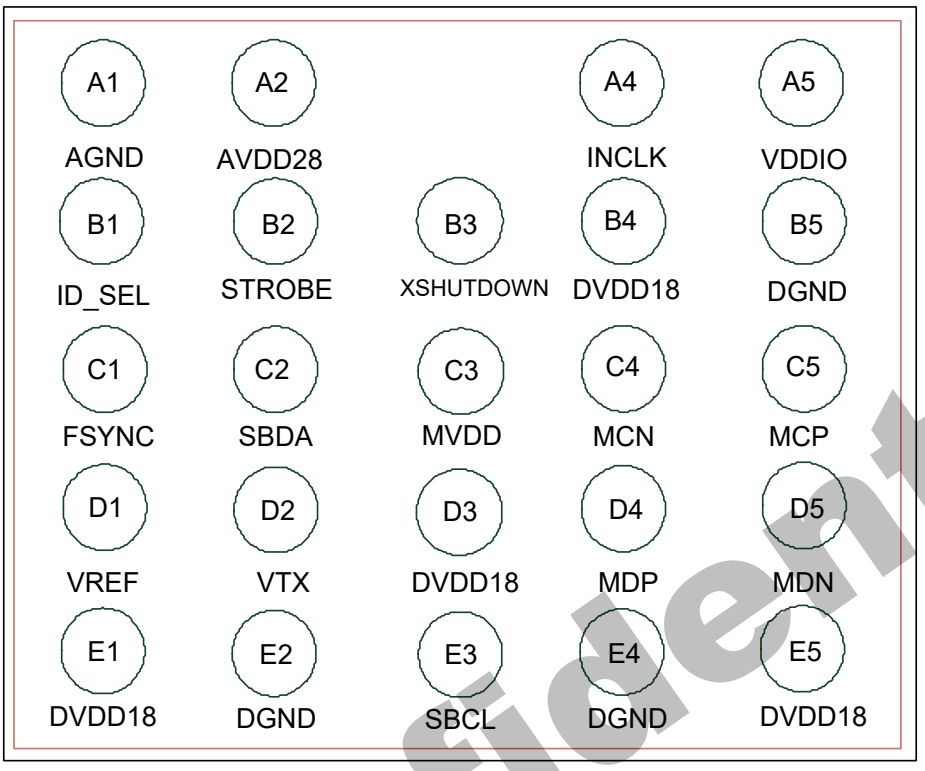
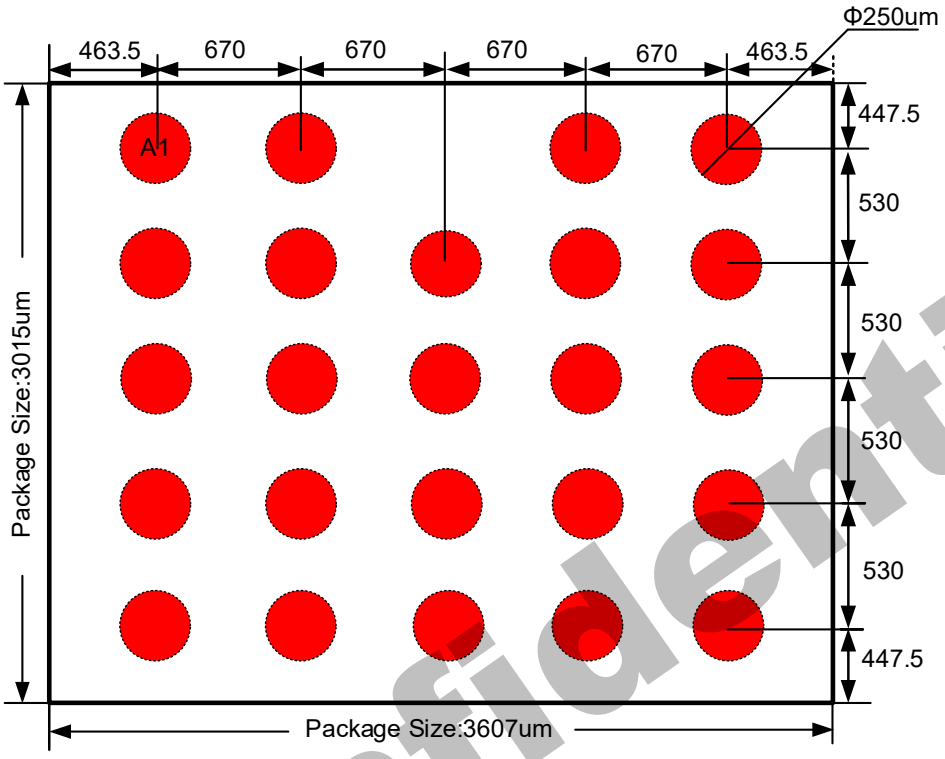


Table 7: Bonding matrix

	1	2	3	4	5
A	AGND	AVDD28	/	INCLK	VDDIO
B	ID_SEL	STROBE	XSHUTDOWN	DVDD18	DGND
C	FSYNC	SBDA	MVDD	MCN	MCP
D	VREF	VTX	DVDD18	MDP	MDN
E	DVDD18	DGND	SBCL	DGND	DVDD18

3.2 PCB Design Diagram

Figure 5: PCB design diagram (Top view)



3.3 Pin Descriptions

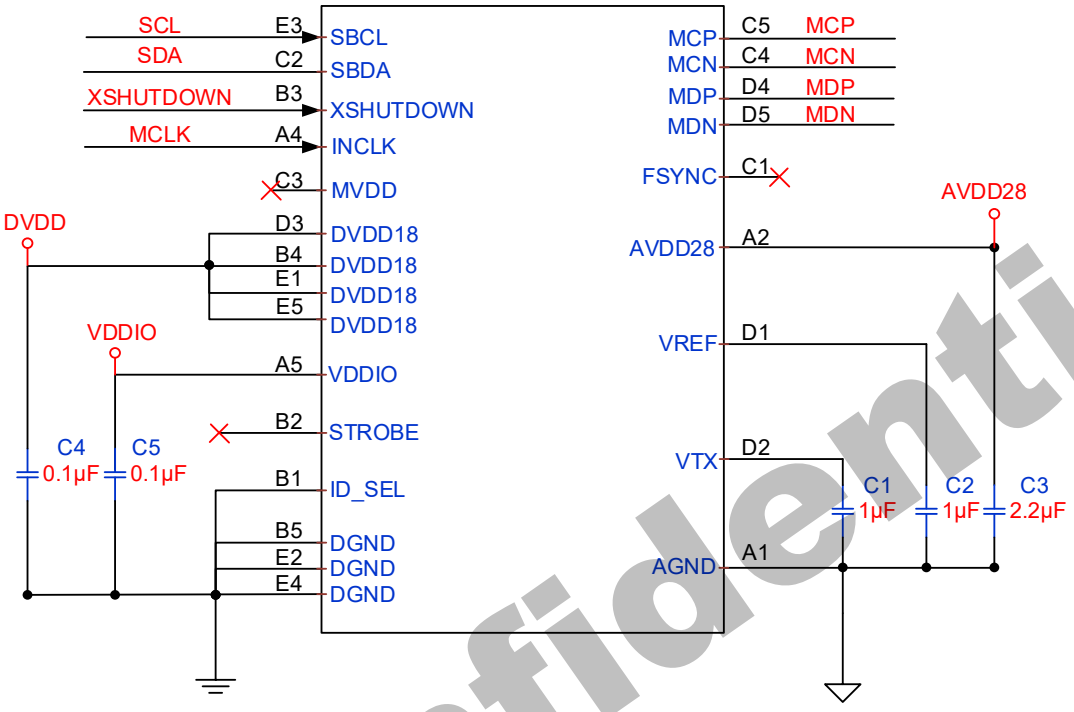
Table 8: Pin Descriptions

Pin	Name	Pin Type	Description
A1	AGND	Ground	Ground for analog.
A2	AVDD28	Power	Main power supply pin: 2.8V (Typ.), please connect capacitor resistance to analog ground.
A4	INCLK	Input	Sensor input clock.
A5	VDDIO	Power	Power supply for I/O circuits: 1.8V(Typ.), Please connect capacity to digital ground.
B1	ID_SEL	Input	IDSEL: 0: 0x6e/0x6f (default) 1: 0x20/0x21
B2	STROBE	I/O	Strobe control.
B3	XSHUTDOWN	Input	Sensor power down control: 0: standby 1: normal work
B4	DVDD18	Power	Power supply for Digital circuits: 1.8V(Typ.), Please connect capacity to digital ground.
B5	DGND	Ground	Ground for digital.
C1	FSYNC	I/O	Frame sync control.
C2	SBDA	I/O	Two-wire serial bus, data
C3	MVDD	Power	Internal power supply.
C4	MCN	Output	MIPI clock (-)
C5	MCP	Output	MIPI clock (+)

Pin	Name	Pin Type	Description
D1	VREF	Power	Internal power supply, please connect capacity to analog ground.
D2	VTX	Power	Internal power supply, please connect capacity to analog ground.
D3	DVDD18	Power	Power supply for Digital circuits: 1.8V(Typ.), Please connect capacity to digital ground.
D4	MDP	Output	MIPI data (+)
D5	MDN	Output	MIPI data (-)
E1	DVDD18	Power	Power supply for Digital circuits: 1.8V(Typ.), Please connect capacity to digital ground.
E2	DGND	Ground	Ground for digital.
E3	SBCL	Input	Two-wire serial bus, clock.
E4	DGND	Ground	Ground for digital.
E5	DVDD18	Power	Power supply for Digital circuits: 1.8V(Typ.), Please connect capacity to digital ground.

3.4 Reference circuit design

Figure 6: reference circuit design diagram



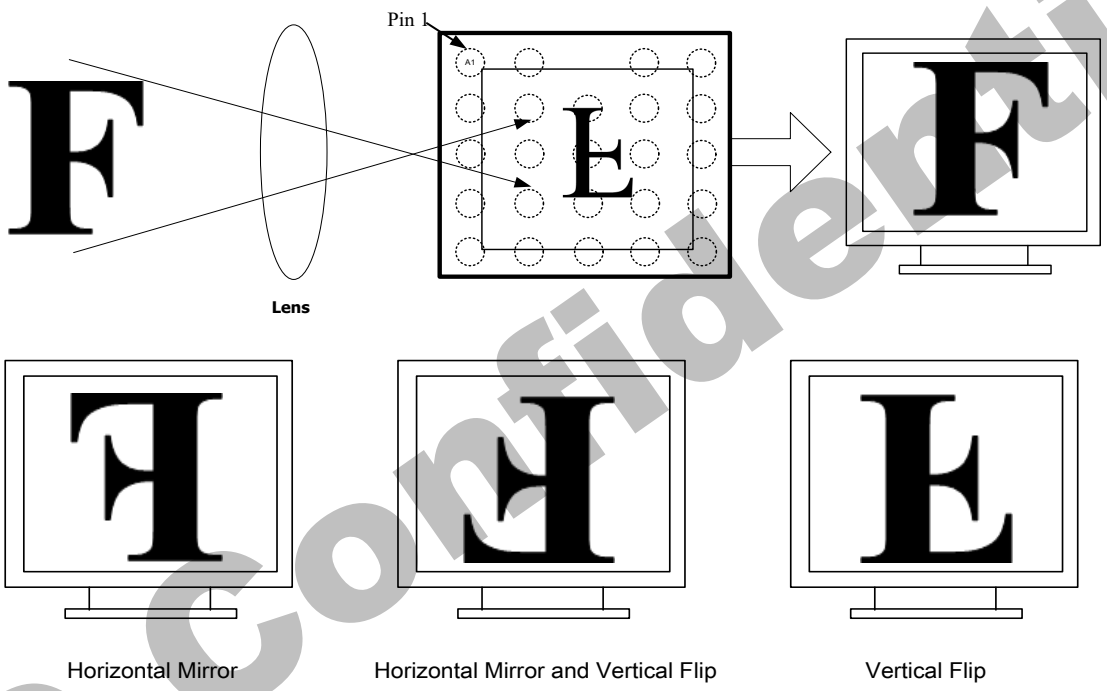
Capacitor No.	Power	Capacitor
C1	VTX	1μF
C2	VREF	1μF
C3	AVDD28	2.2μF
C4	DVDD	0.1μF
C5	VDDIO	0.1μF

4. Optical Specifications

4.1 Readout Position

The GC02M2 default status is readout from the lower left corner with Pin A1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so mirrored image output results when Pin1 is located in the lower left corner.

Figure 7: readout position



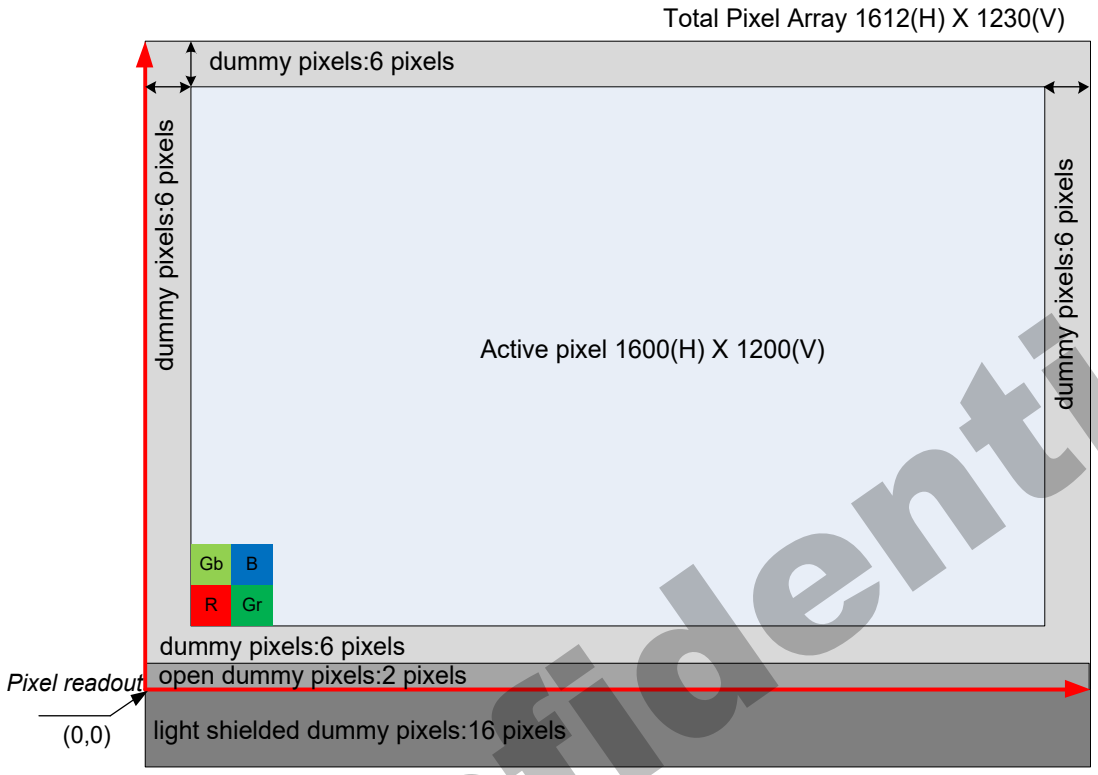
Readout direction can be set by the registers.

Table 9: Mirror and flip info

Function	Register Address	Register Value	First Pixel
Normal	P0:0x17[1:0]	00	R
Horizontal mirror	P0:0x17[1:0]	01	Gr
Vertical Flip	P0:0x17[1:0]	10	Gb
Horizontal Mirror and Vertical Flip	P0:0x17[1:0]	11	B

4.2 Pixel Array

Figure 8: pixel array



4.3 Lens Chief Ray Angle (CRA)

Figure 9: CRA information

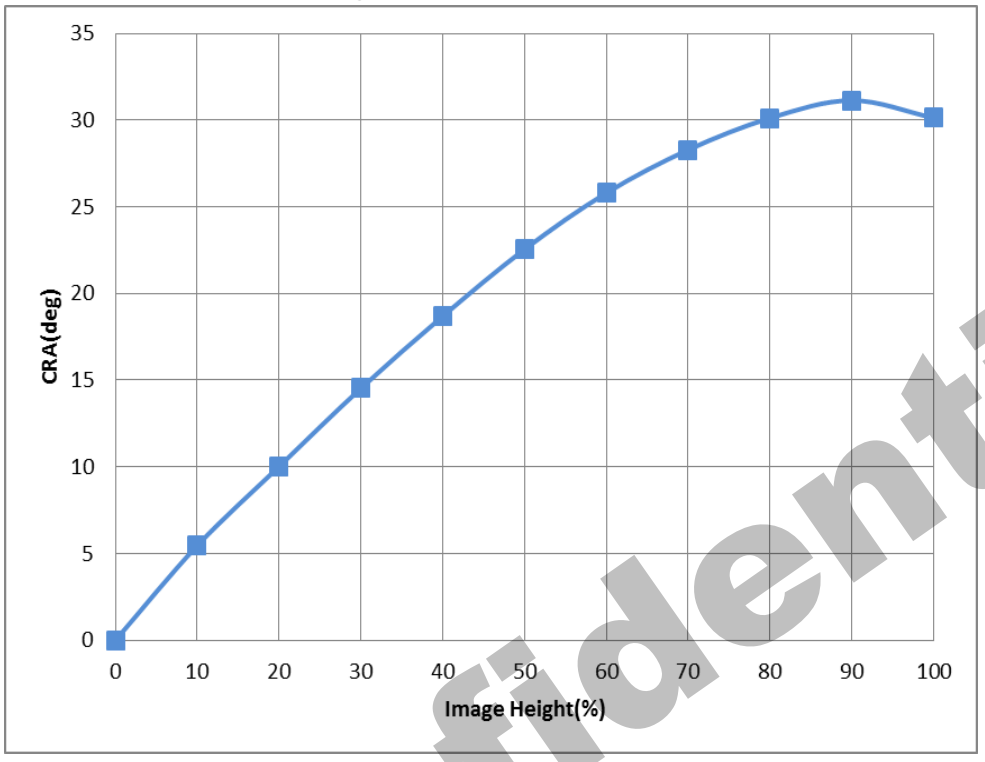


Table 10: CRA information

Image Height (%)	Image Height (mm)	CRA (degree)
0	0.000	0.00
10	0.175	5.46
20	0.350	10.02
30	0.525	14.53
40	0.700	18.69
50	0.875	22.55
60	1.050	25.80
70	1.225	28.29
80	1.400	30.12
90	1.575	31.14
100	1.750	30.13

5. Two-wire Serial Bus Communication

5.1 Protocol

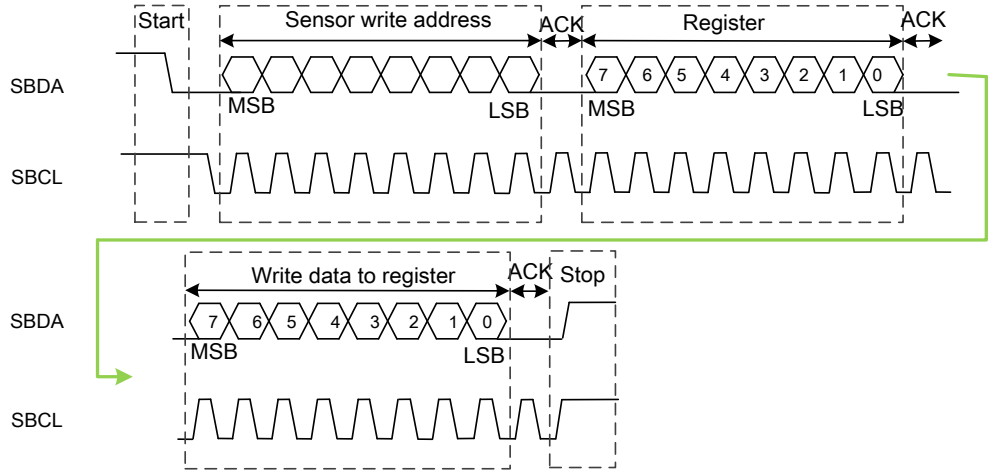
The host must perform the role of a communications master and GC02M2 acts as either a slave receiver or transmitter. The master must do:

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**
- GC02M2 Device Address:

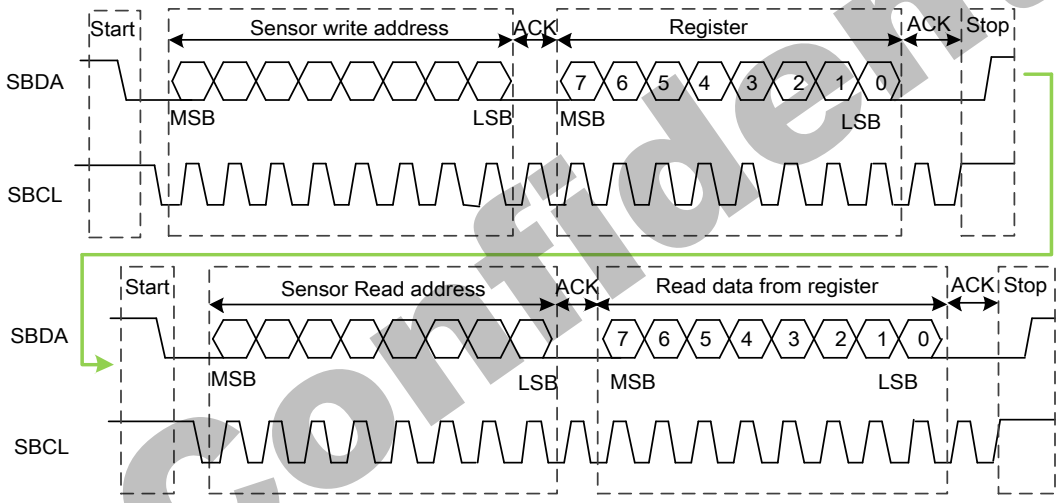
Table 11: CCI device ID

ID_SEL	Slave address write mode	Slave address read mode	comment
0(DGND)	0x6e	0x6f	Address 1
1(IOVDD)	0x20	0x21	Address 2

Write operate



Read Operate



5.2 Serial Bus Timing

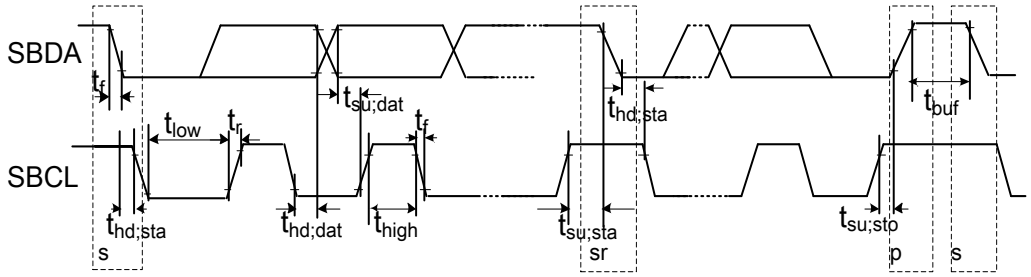
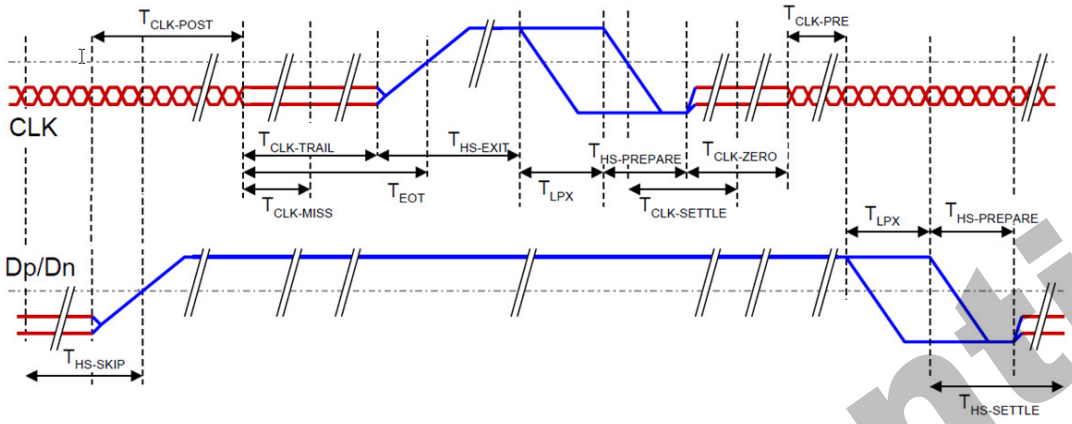


Table 12: Serial Bus Timing

Parameter	Symbol	Min	Typ.	Max	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between a stop and a start	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	600	--	--	ns
Data hold time	$t_{hd;dat}$	0	--	900	ns
Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	pf

6. Applications

6.1 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

  $T_{CLK\_HS\_PREPARE}$: setting by Register P3:0x22

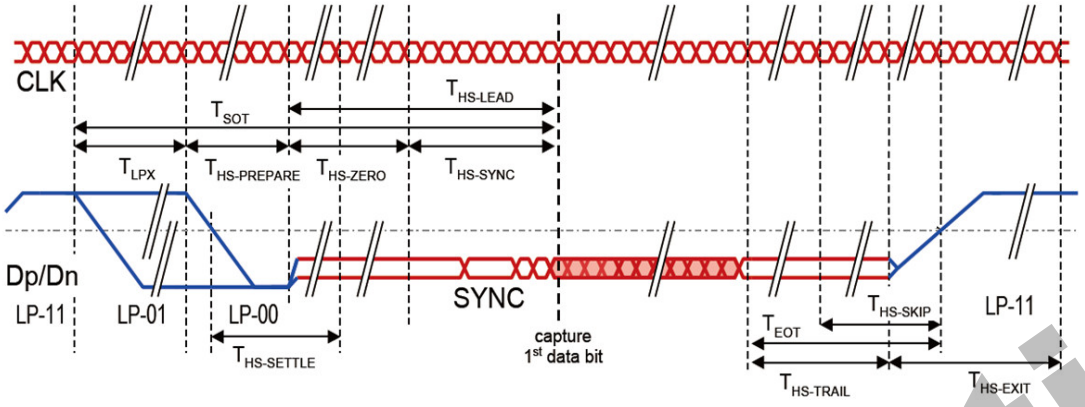
  T_{CLK_ZERO}: setting by Register P3:0x23

  T_{CLK_PRE}: setting by Register P3:0x24

  T_{CLK_POST}: setting by Register P3:0x25

  T_{CLK_TRAIL}: setting by Register P3:0x26

6.2 Data Burst



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

T_{LPX}: setting by Register P3:0x21

$T_{HS\_PREPARE}$: setting by Register P3:0x29

T_{HS_ZERO}: setting by Register P3:0x2a

T_{HS_TRAIL}: setting by Register P3:0x2b

T_{HS_EXIT}: setting by Register P3:0x27

7. Function Description

7.1 Operation mode

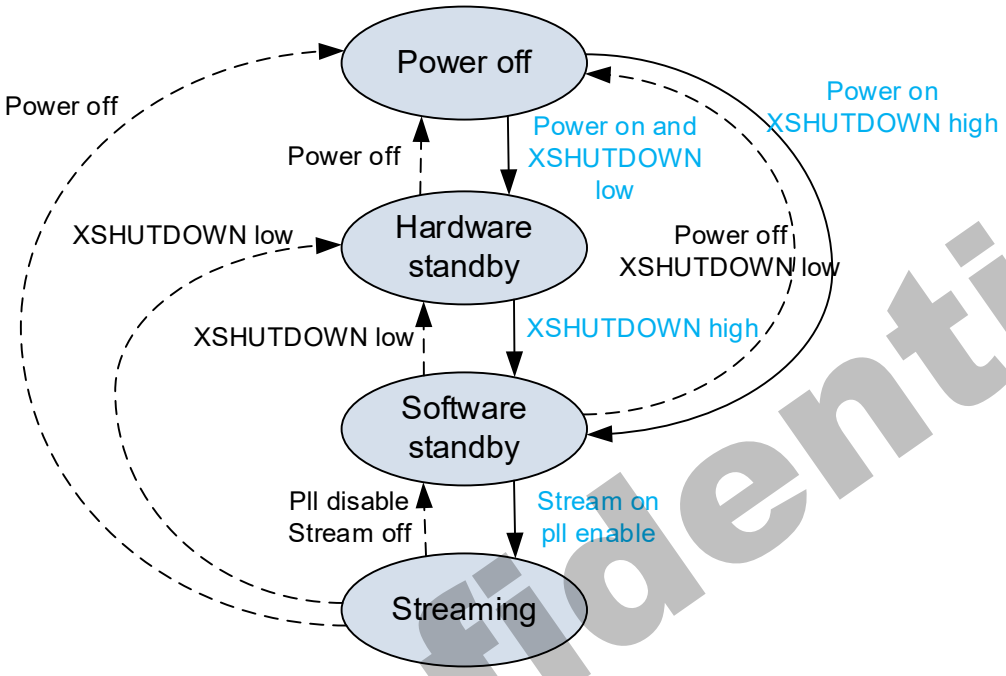


Table 13: Operate State

Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on XSHUTDOWN	XSHUTDOWN low
Software standby	Two- wire serial communication with sensor is possible,PLL is ready for fast return to streaming mode	Stream mode off PLL disable XSHUTDOWN high
Streaming	Sensor is fully powered and streaming image data on the MIPI CSI-2 bus	All Pad Enabled

7.2 Power on Sequence

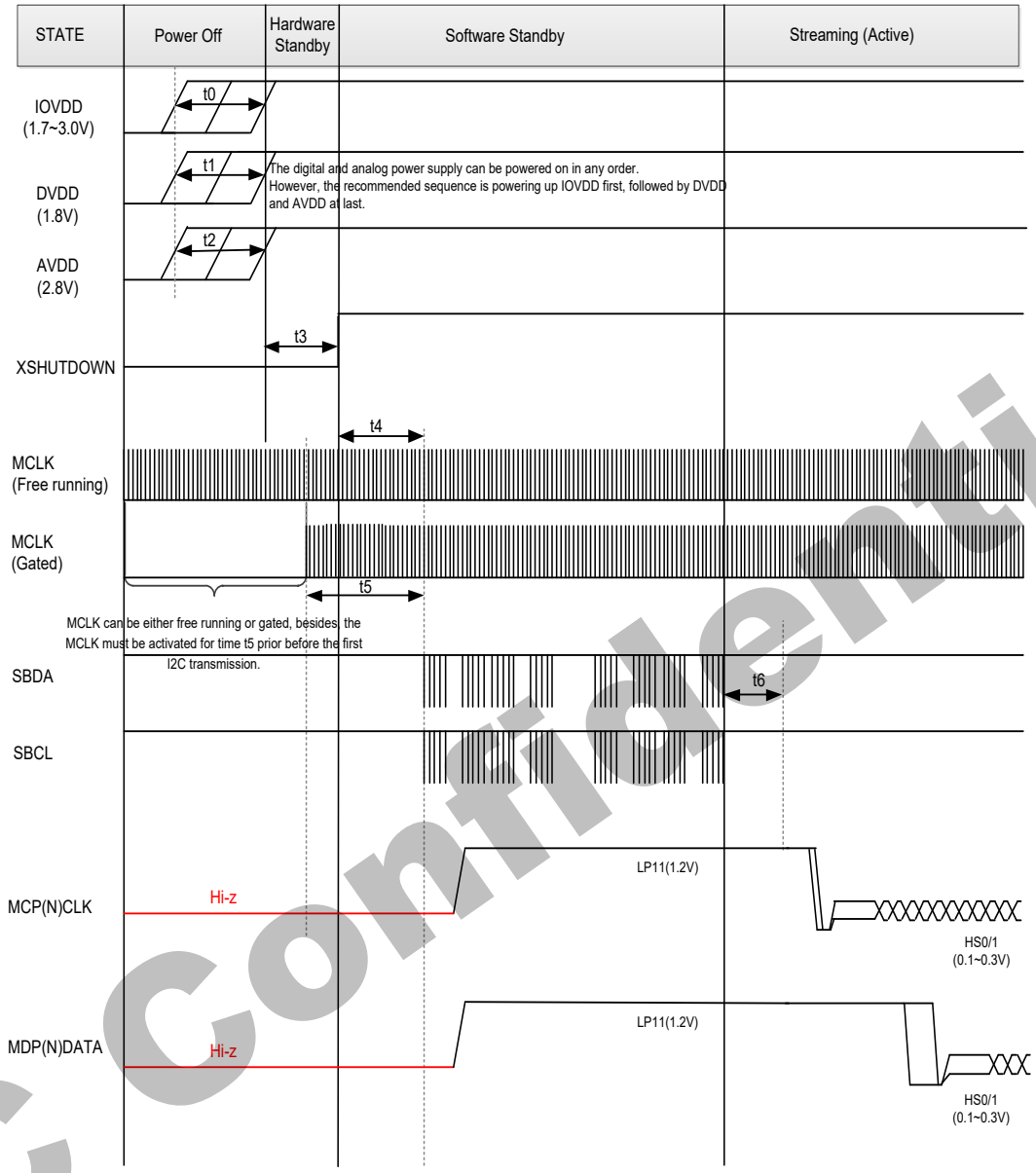


Table 14: Power On Timing

Parameter	Description	Min.	Max.	Unit
t0	IOVDD rising time	IOVDD/DVDD/AVDD may rise in any order. The rising separation can vary from 0μs to indefinite.		μs
t1	DVDD rising time			μs
t2	AVDD rising time			μs
t3	From power on to XSHUTDOWN pull high	0	-	μs
t4	XSHUTDOWN rising to first I2C transaction	50	-	μs
t5	Minimum No. of MCLK cycles prior to the first I2C transaction	1200	-	MCLK
t6	PLL startup/lock time	-	1	ms

Note:

1. IOVDD/DVDD/AVDD can be powered in any order. The recommend sequence is to power up IOVDD first, followed by DVDD and AVDD at last.
2. Register should be reloaded before works.

7.3 Power off Sequence

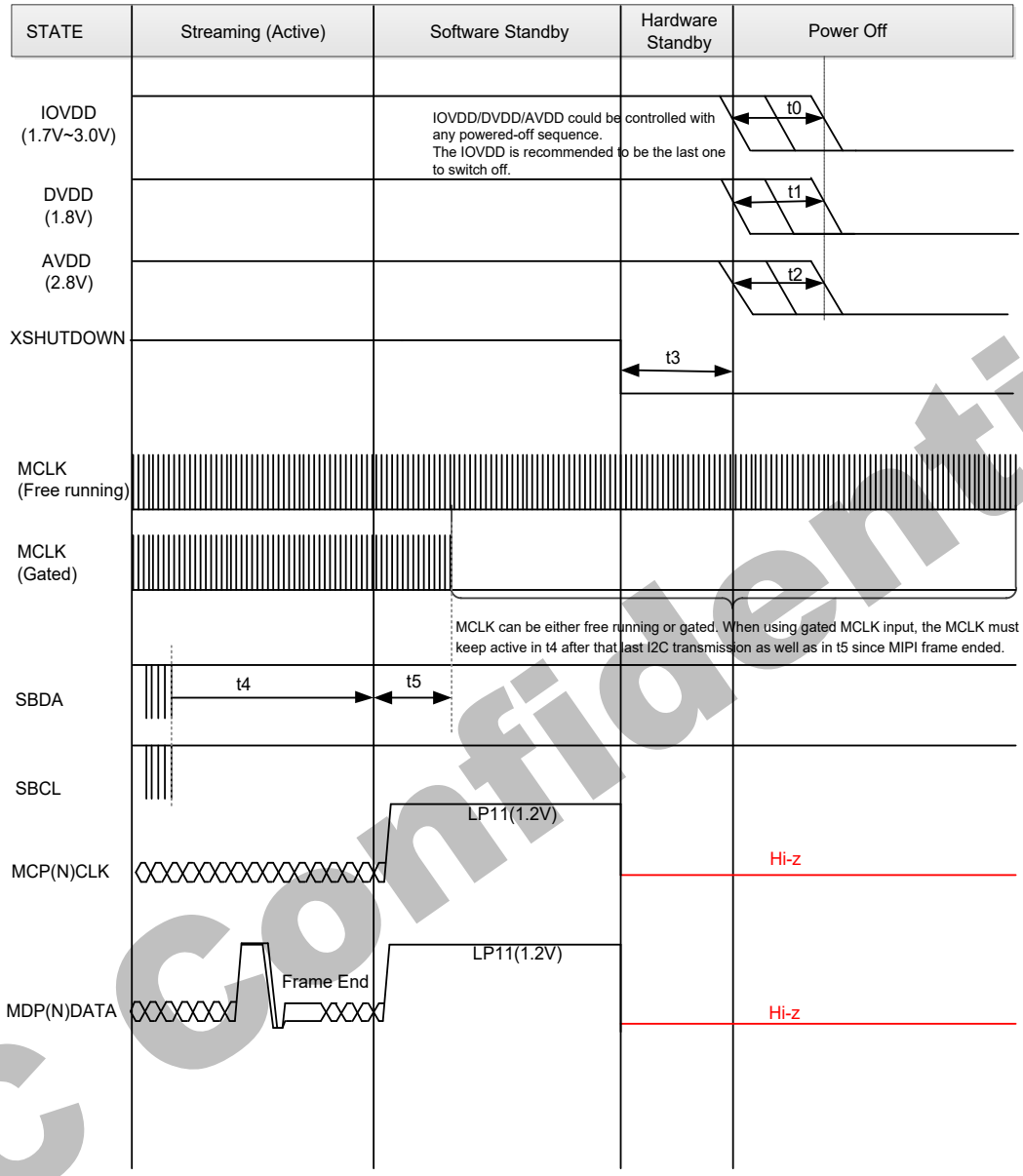


Table 15: Power Off Timing

Parameter	Description	Min.	Max.	Unit
t0	IOVDD fall time	IOVDD/DVDD/AVDD may fall in any order. The fall separation can Vary from 0μs to indefinite.		μs
t1	DVDD fall time			μs
t2	AVDD fall time			μs
t3	From XSHUTDOWN pull down to power off	0		μs
t4	Enter Software Standby CCI command – Device in Software Standby mode	0	-	μs
t5	Minimum number of MCLK cycles after the last CCI transaction or MIPI frame end code.	0		MCLK

Note:

1. IOVDD/DVDD/AVDD can be shut down in any order. The recommend sequence is to power off AVDD and DVDD before IOVDD.
2. If the sensor’s power cannot be shut down, please keep power supply, and set XSHUTDOWN pin low. It can make sensor HW standby.
3. If customers need to change this sequence, please do contact our FAE.

7.4 Black level calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

7.5 Integration time

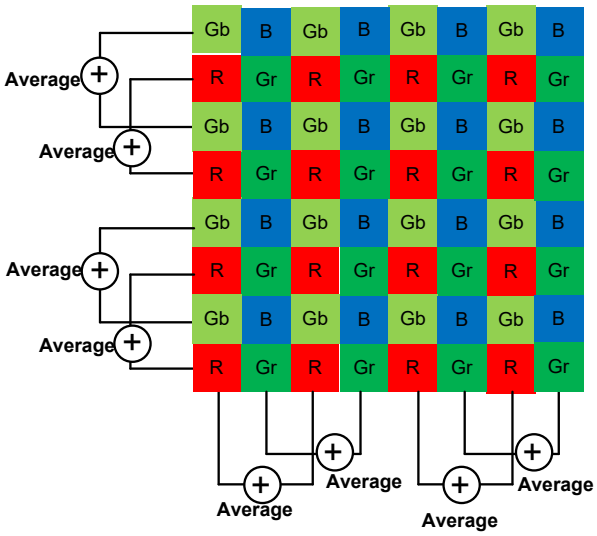
The integration time is controlled by the integration time registers

Table 16: Shutter Time Register

Addr.	Register name	Description
P0:0x03	Shutter time	[7:0] shutter time[13:8]
P0:0x04		[7:0] shutter time[7:0]

7.6 Binning mode

Binning read-out can be used to obtain an image of lower resolution for full field of view. The following diagram describes on 2x2 averaged binning operations. Pixels of two adjacent rows and columns are averaged, and read out as one output pixel.



7.7 Windowing

GC02M2 has a rectangular pixel array 1612 x 1212, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.

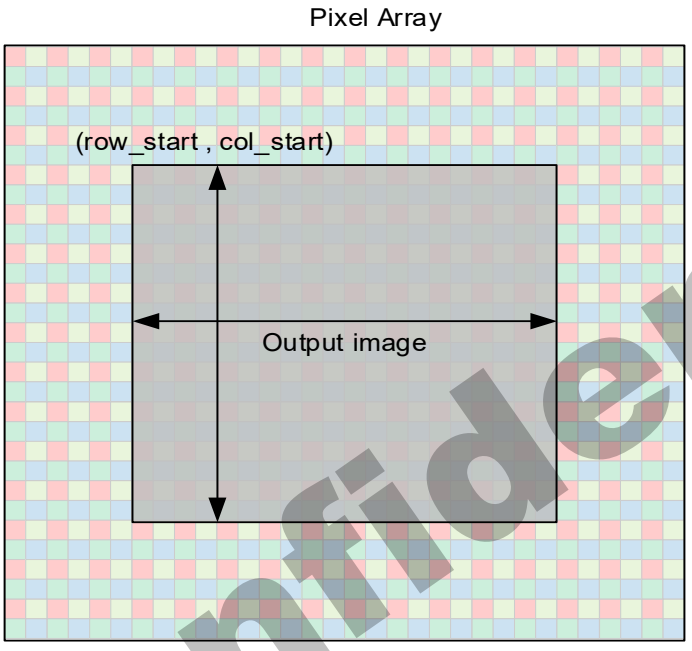
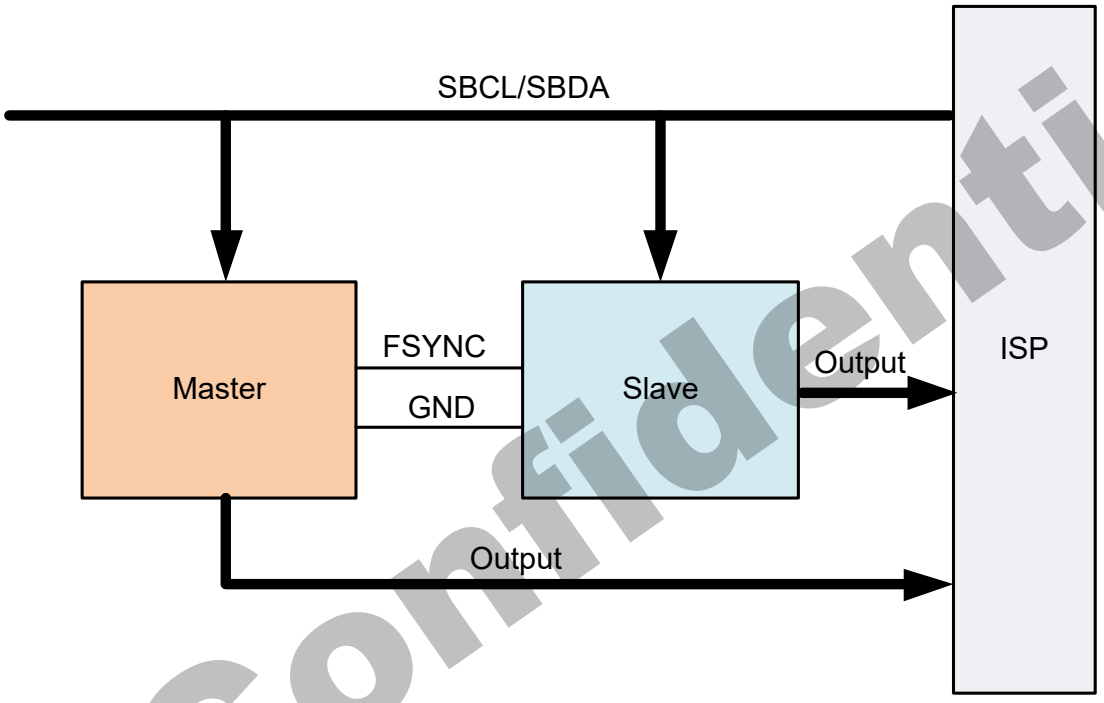


Table 17: Windowing Set Register List

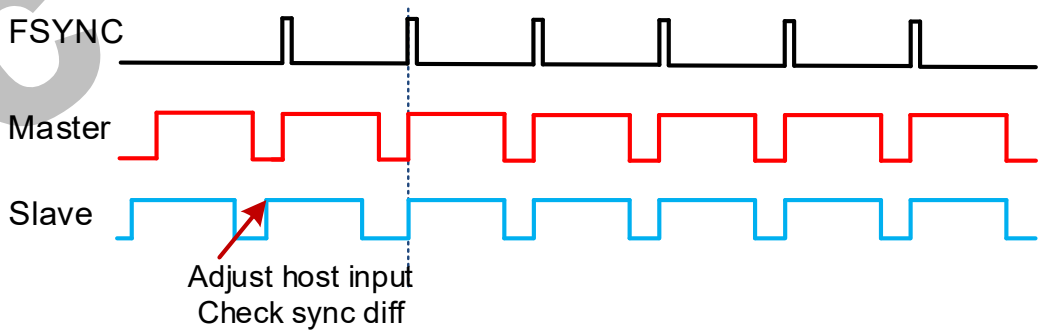
Addr.	Register name	Description
P0:0x0d	win_height	[2:0]win_height[10:8]
P0:0x0e		[7:0]win_height[7:0]
P0:0x0f	win_width	[3:0]win_width[11:8]
P0:0x10		[7:0]win_width[7:0]
P0:0x09	Row start	[2:0]row_start[10:8]
P0:0x0a		[7:0]row_start [7:0]
P0:0x0b	Col start	[2:0]col_start[10:8]
P0:0x0c		[7:1]col_start[7:1]

7.8 Frame sync Mode

GC02M2 can support hardware frame sync for dual camera application. It can be set both master and slave sensor. When use this mode, the two sensor’s FSYNC pin must connect to each other.



Adjust mismatch sync



Dynamic mismatch sync control

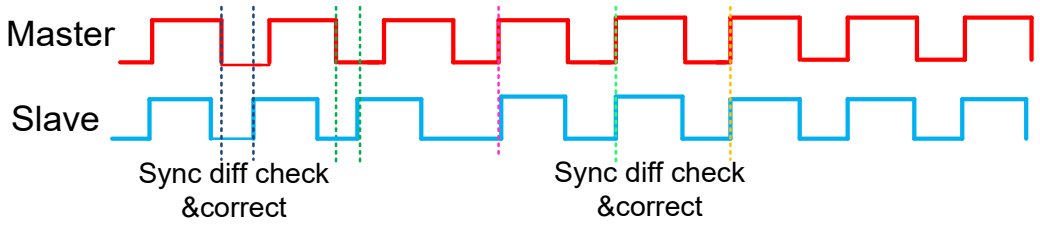


Table 18: FSYNC Relate Register

Addr.	Register name	Description
P0:0x7f	fsync_mode	[7] master clear counter [6] master update flop [5] master clear counter stop [4] fsync_clear_counter [3] clock en [2] lave ready for receive [1] 1:master / 0: slave [0] fsync en
P0:0x83	fsync_mode_new3	[7] fsync_row_force [6:0] fsync out position
P0:0x85	fsync_mode_new4	[7] fsync_vb_gap_mode_tmp [6] fsync_vb_first_mode_tmp [5] fsync_row_diff_mode [4] fsync_vb_mode [3:0] vb_lowbits_disable

7.9 Strobe Timing

The strobe function of GC02M2 is controlled by strobe request (P2:0x84[0]), which is level triggered. The beginning and the end of the request should not within the same frame.

As the strobe request begins, there are two sub-patterns we can use.

The first is row_sel (P2:0x8a[2]), which means we can choose several rows to determine the duration of the request.

Second is frame_sel (P2:0x8a[1]), the meaning of which is similar to the first one.

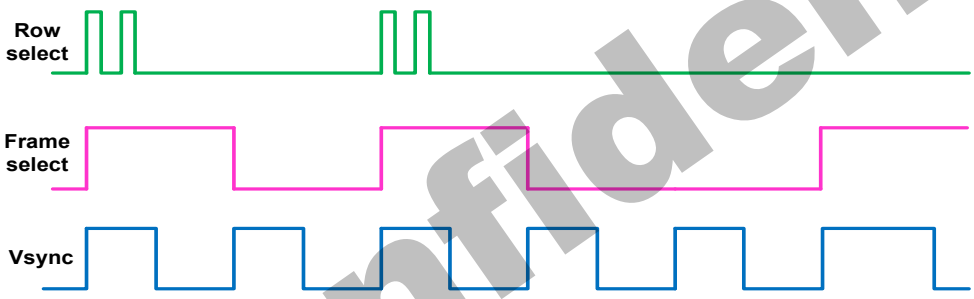


Table 19: Strobe Relate Register

Addr.	Register name	Description
P2:0x84	strobe_request	[0] strobe_request
P2:0x85	strobe_mode2	[2] strobe_frame_times_mode [1] strobe_enlength [0] strobe_short_mode
P2:0x86	strobe_exp_th	[7:0] strobe_exp_th[7:0]
P2:0x87		[5:0] strobe_exp_th[13:8]
P2:0x88	strobe_lasts_th	[7:0] strobe_lasts_th[7:0]
P2:0x89		[5:0] strobe_lasts_th[13:8]
P2:0x8c	strobe_pre_exp_num	[7:0] strobe_pre_exp_num

7.10 OTP Memory

GC02M2 sensor has 256 bits embedded OTP (One Time Programmable) memory, and 136 bits is for customer which use for storing module calibration date.

7.11 Frame Structure

Frame structure is controlled by line length, frame length, out window height and out window width.

Frame length lines control

Frame length is controlled by window height, minimum VB and shutter time.

- Minimum frame length = window height + 32 + min_VB (Reg[P0:0x9d])

  Min_VB should be >16
- If shutter time (Reg[P0:0x03, P0:0x04]) < minimum frame length-16,

  Actual frame length = minimum frame length
- If shutter time > minimum frame length-16,

  Actual frame length = Shutter time + 16

Addr.	Register Name	Description
P0:0x41	Frame length	[5:0] frame length[13:8]
P0:0x42		[7:0] frame length[7:0]
P0:0x9d	min_vb	min_vb[5:0]

Line length control

The typical line length is 1096 (MCLK=24MHz), and it is not recommended to be modified.

Addr.	Register name	Description
P0:0x05	Line length	[3:0] Line length[11:8]
P0:0x06		[7:0] Line length[7:0]

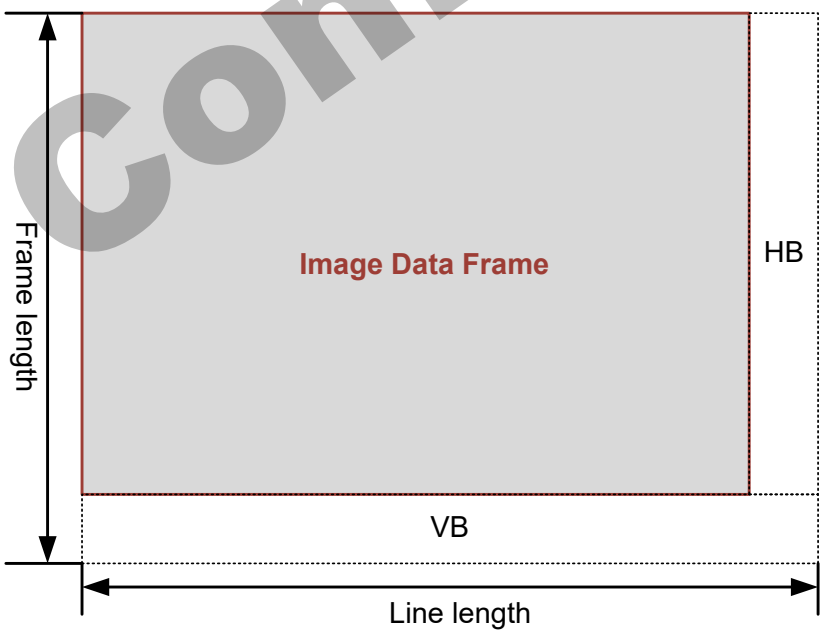
Actual line length = Line length(Reg[P0:0x05,P0: 0x06]) *2

Output window array control

Addr.	Register name	Description
P1:0x91	Out_window_y1	[2:0] Out_window_y1[10:8]
P1:0x92		[7:0] Out_window_y1[7:0]
P1:0x93	Out_window_x1	[3:0] Out_window_x1[11:8]
P1:0x94		[7:0] Out_window_x1[7:0]
P1:0x95	Out window height	[2:0] Out window height[10:8]
P1:0x96		[7:0] Out window height[7:0]
P1:0x97	Out window width	[3:0] Out window width[11:8]
P1:0x98		[7:0] Out window width[7:0]

Blank time control

1. line blank time is controlled by line length
2. frame blank time
   - frame blank time = frame length(Reg[P0:0x41, P0:0x:42]) – out window height



8. Register List

8.1 System Register

Address	Name	Default Value	R/W	Description
0xf0	Sensor_ID_high	0x02	RO	Sensor_ID
0xf1	Sensor_ID_low	0xf0	RO	Sensor_ID
0xf2	Chip_verison	0x00	RO	Chip_verison
0xf3	OTP clk ena	0x00	RW	[7] OTP_finish(RO) [6] OTP_busy(RO) [5] OTP_clk_en [4] OTP_en
0xf4	Group hold	0x01	RW	[4] group hold
0xf5	Pll ldo set	0x80	RW	[6] pll_ldo_en [1] I2C_open_ena
0xf8	PLL_mode2	0x30	RW	[7:0] pllmp_div
0xf9	Analog PWD	0x83	RW	[0] apwdn
0xfb	I2c_device_id	0x6e	RO	[7:1] I2C addr
0xfc	Pll enable	0x00	RW	[0] pll ena
0xfe	System Reset	0x00	RW	[7] soft_reset [6] cm_reset clk manager [5] mipi_reset [4] CISCTL_reset [2:0] page_select

8.2 Shutter & Frame structure

Address	Name	Default Value	R/W	Description
P0:0x03	Shutter H [13:8]	0x00	RW	Shutter H [13:8]
P0:0x04	Shutter L [7:0]	0x10	RW	Shutter L [7:0]
P0:0x05	Line length [11:8]	0x04	RW	Line length
P0:0x06	Line length [7:0]	0x48	RW	
P0:0x07	Vblanking H [13:8]	0x00	RW	Vertical blanking
P0:0x08	Vblanking L [7:0]	0x10	RW	
P0:0x09	row_start [10:8]	0x00	RW	Row Start
P0:0x0a	row_start [7:0]	0x00	RW	
P0:0x0b	col_start [10:8]	0x00	RW	Col start
P0:0x0c	col_start [7:1]	0x00	RW	
P0:0x0d	win_height [10:8]	0x04	RW	[2:0] Window height[10:8]
P0:0x0e	win_height [7:0]	0xbe	RW	[7:0] Window height[7:0]
P0:0x0f	win_width [10:8]	0x06	RW	[2:0] Window width[10:8]
P0:0x10	win_width [7:0]	0x4c	RW	[7:0] window width[7:0]
P0:0x17	Flip&mirror	0x80	RW	[1] updown [0] mirror

8.3 GAIN control

Address	Name	Default Value	R/W	Description
P0:0xb1	Digital gain H	0x04	RW	Digital gain
P0:0xb2	Digital gain L	0x00	RW	
P0:0xb6	Analog gain	0x00	RW	[4:0] Analog gain

8.4 ISP

Address	Name	Default Value	R/W	Description
P1:0x60	Offset level	0x40	RW	[7:0] offset level
P1:0x8c	Test pattern	0x10	RW	[0] test image
P1:0x91	out_win_y1[10:8]	0x00	RW	[2:0] out_win_y1[10:8]
P1:0x92	out_win_y1 [7:0]	0x00	RW	[7:0] out_win_y1 [7:0]
P1:0x93	out_win_x1[11:8]	0x00	RW	[3:0] out_win_x1[11:8]
P1:0x94	out_win_x1 [7:0]	0x00	RW	[7:0] out_win_x1[7:0]
P1:0x95	out_height[10:8]	0x07	RW	[2:0] out_height[10:8]
P1:0x96	out_height[7:0]	0x98	RW	[7:0] out_height[7:0]
P1:0x97	out_width[11:8]	0x0a	RW	[3:0] out_width[11:8]
P1:0x98	out_width[7:0]	0x20	RW	[7:0] out_width[7:0]

8.5 OTP

Address	Name	Default Value	R/W	Description
P2:0x17	otp_addr_low	0x00	RW	[7:0] otp_addr_low
P2:0x18	otp_write_value	0x00	RW	[7:0] otp_write_value
P2:0x19	otp_read_value	--	RO	[7:0] otp_addr_low

8.6 MIPI

Address	Name	Default Value	R/W	Description
P3:0x01	DPHY_enable	0x20	RW	[1] phy_lane0_en [0] phy_clk_en;
P3:0x02	Mipi_diff	0x13	RW	[5:4] data0ctr [3:0] mipi_diff
P3:0x03	Lane mode	0xca	RW	[7] clklane_p2s_sel [6:5] data0hs_ph [4] data0delay1s [3] clkdelay1s [2] mipi_en
P3:0x11	LDI_set	0x2b	RW	RAW8:0x2a RAW10:0x2b
P3:0x12	LWC_set[7:0]	0xd0	RW	LWC set
P3:0x13	LWC_set[15:8]	0x07	RW	
P3:0x14	SYNC_set	0xb8	RW	SYNC_set
P3:0x15	Clk lane mode	0x10	RW	[1:0] clk lane_mode
P3:0x20	init_set	0x80	RW	Timing of initial setting
P3:0x21	LPX_set	0x10	RW	Timing of LP setting
P3:0x22	HS_PREPARE_set	0x05	RW	HS PREPARE setting
P3:0x23	zero_set	0x20	RW	HS zero setting
P3:0x24	PRE_set	0x02	RW	HS PRE of Data setting
P3:0x25	POST_set	0x20	RW	HS Post of Data setting
P3:0x26	TRAIL_set	0x08	RW	Tail timing setting
P3:0x27	HS_exit_set	0x10	RW	HS exit setting