SMARTSENS

SmartSens™
SC230AI Datasheet

V1.7

2023-11-15

■ Applications

- ◆ Industrial surveillance cameras
- ◆ Low light video cameras
- ◆ Home IoT cameras

■ Features

- ◆ HDR
  - ■ Staggered HDR
- ◆ High sensitivity
- ◆ High signal to noise ratio
- ◆ 850nm/940nm NIR
- ◆ Dual conversion gain
- ◆ Low power consumption
- ◆ 99x analog gain, 16x digital gain
- ◆ High speed DPC
- ◆ External control frame rate, multiple sensors synchronization
- ◆ Horizontal/vertical windowing
- ◆ Horizontal/vertical mirror and flip
- ◆ 2 x 2 binning mode
- ◆ Programmable I2C port register

■ Specifications

Parameters	Description
Resolution	2MP
Pixel array	1928H x 1088V
Pixel size	2.9 μm x 2.9 μm
Optical format	1/2.8”
Maximum frame rate	1920H x 1080V@60fps 10bit
Output interface	10/8-bit 1/2Lane MIPI 10-bit DVP
Output format	RAW RGB
CRA	15°
Sensitivity	7341 mV/lux • s
Dynamic range	Linear mode: 86 dB; HDR mode: >100 dB
SNR	42 dB
Operation temperature range	-30°C ~+85°C
Best IQ temperature	-20°C~+60°C
Power supply	AVDD = 2.8V ± 0.1V, DVDD=1.5V ± 0.1V, DOVDD = 1.8V ± 0.1V
Package	CSP, 6.271 mm x 4.107 mm, 41-pin
ESD rank	HBM: Classification 2 CDM: Classification C3

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1. System Description

1.1. General Description

SC230AI is an advanced digital CMOS image sensor for surveillance cameras, supporting a maximum resolution of 1920H × 1080V@60fps. It outputs raw images with an effective pixel array of 1928H × 1088V and supports complex on-chip operations such as windowing, horizontal or vertical mirroring, and so on. It can be configured via the standard I^2C interface. It can achieve external control of frame rate and multiple sensor synchronization via the EFSYNC/FSYNC pin.

1.2. System Framework

Figure 1-1 shows the block diagram of SC230AI. SC230AI supports the Mobile Industry Processor Interface (MIPI) and Digital Video Port (DVP). Figure 1-2 shows a typical configuration example using the MIPI.

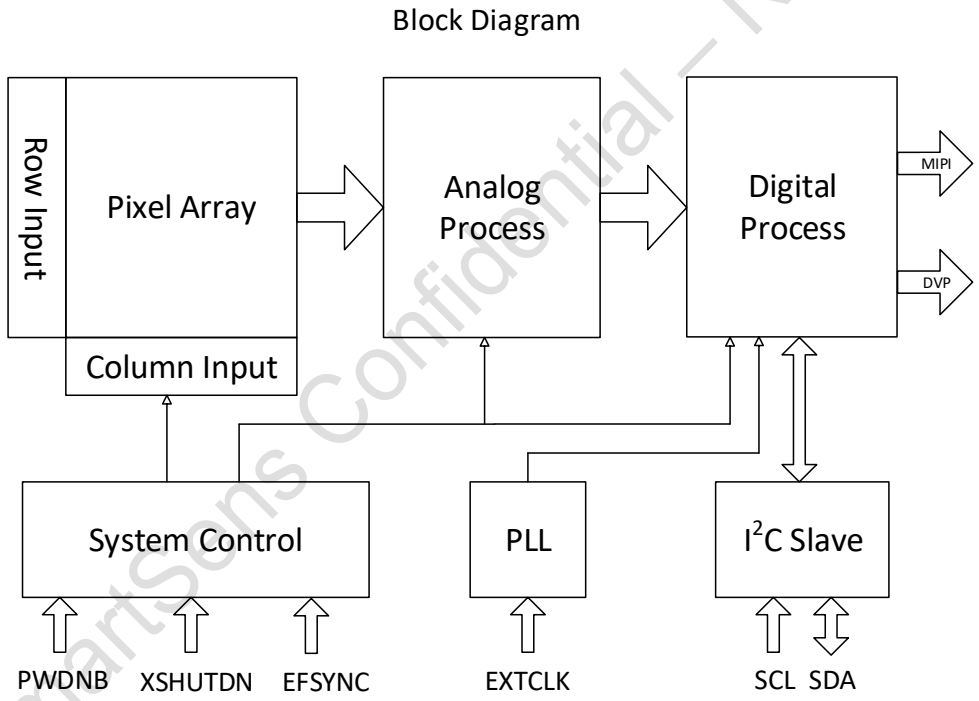

Figure 1-1 Block diagram

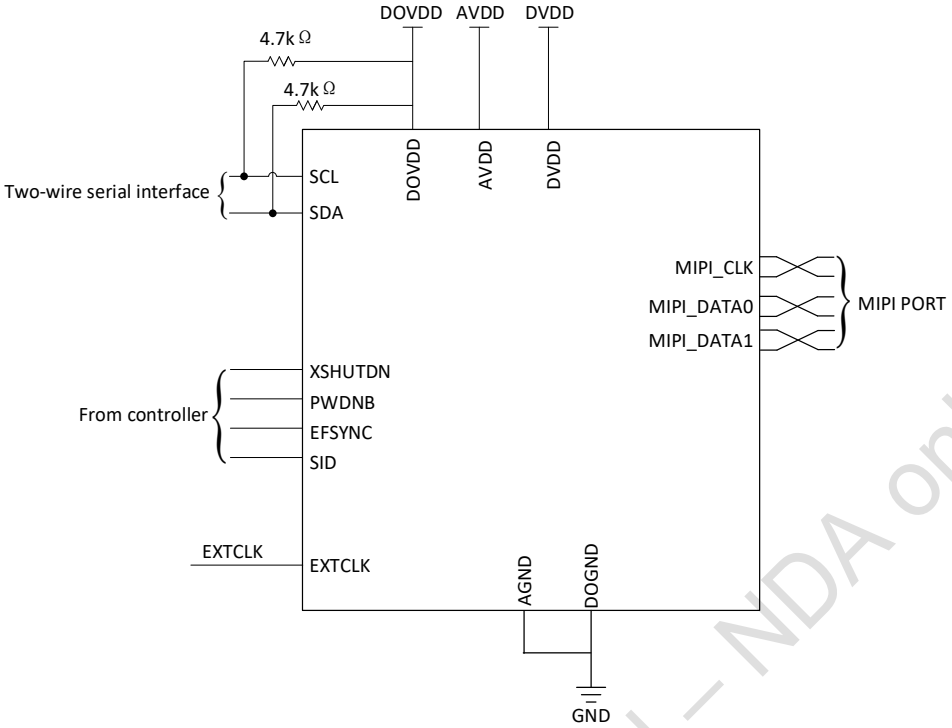

Figure 1-2 Typical configuration diagram

1.3. Pin Description

The table below lists the pin information and related description of SC230AI.

Table 1-1 Pin description

No.	Pin No.	Pin Name	Pin Type	Description
1	A1	AVDD	Power	2.8V Analog Power Supply
2	A2	LREF	Output	DVP Row SYNC
3	A3	SCL	Input	I²C Clock Line
4	A4	PWDNB	Input	Power Down (internal pull-up, active low)
5	A5	SID	Input	I²C Device ID (internal pull-down, device ID = 7'h30)
6	A6	VREF2	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
7	A7	AVDD	Power	2.8V Analog Power Supply
8	B1	AGND	GND	Analog Ground
9	B2	FSYNC	Input / Output	As an external frame synchronization signal when input As a DVP frame synchronization signal when output
10	B3	SDA	Input / Output	I²C Data Line (open drain)
11	B5	DVDD	Power	1.5V Digital Power Supply
12	B6	EFSYNC	Input	External frame synchronization signal
13	B7	AGND	GND	Analog Ground
14	C1	DVDD	Power	1.5V Digital Power Supply
15	C2	EXTCLK	Input	Clock Input
16	C3	DOGND	GND	I/O Ground
17	C4	XSHUTDN	Input	Reset Signal Input (internal pull-up, active low)
18	C5	D<11>	Output	DVP Output Bit [11]
19	C6	NC	-	-
20	C7	AVDD	Power	2.8V Analog Power Supply
21	D1	D<0>	Output	DVP Output Bit [0]
22	D2	DOGND	GND	I/O Ground
23	D3	D<4>	Output	DVP Output Bit [4]
24	D4	DOVDD	Power	1.8V I/O Power Supply
25	D5	D<10>	Output	DVP Output Bit [10]
26	D6	DVDD	Power	1.5V Digital Power Supply
27	D7	NC	-	-
28	E1	D<1>	Output	DVP Output Bit [1]
29	E2	DOVDD	Power	1.8V I/O Power
30	E3	D<5>/MD1N	Output	DVP Output Bit [5]/MIPI Data 1 Negative
31	E4	D<7>/MCN	Output	DVP Output Bit [7]/MIPI Clock Negative
32	E5	D<9>/MD0P	Output	DVP Output Bit [9]/MIPI Data 0 Positive
33	E6	DOGND	GND	I/O Ground
34	E7	VREFH	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
35	F1	D<2>	Output	DVP Output Bit [2]

No.	Pin No.	Pin Name	Pin Type	Description
36	F2	D<3>	Output	DVP Output Bit [3]
37	F3	D<6>/MD1P	Output	DVP Output Bit [6]/MIPI Data 1 Positive
38	F4	PCLK/MCP	Output	DVP Clock/MIPI Clock Positive
39	F5	D<8>/MD0N	Output	DVP Output Bit [8]/MIPI Data 0 Negative
40	F6	DOGND	GND	I/O Ground
41	F7	VREFN	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)

Top View

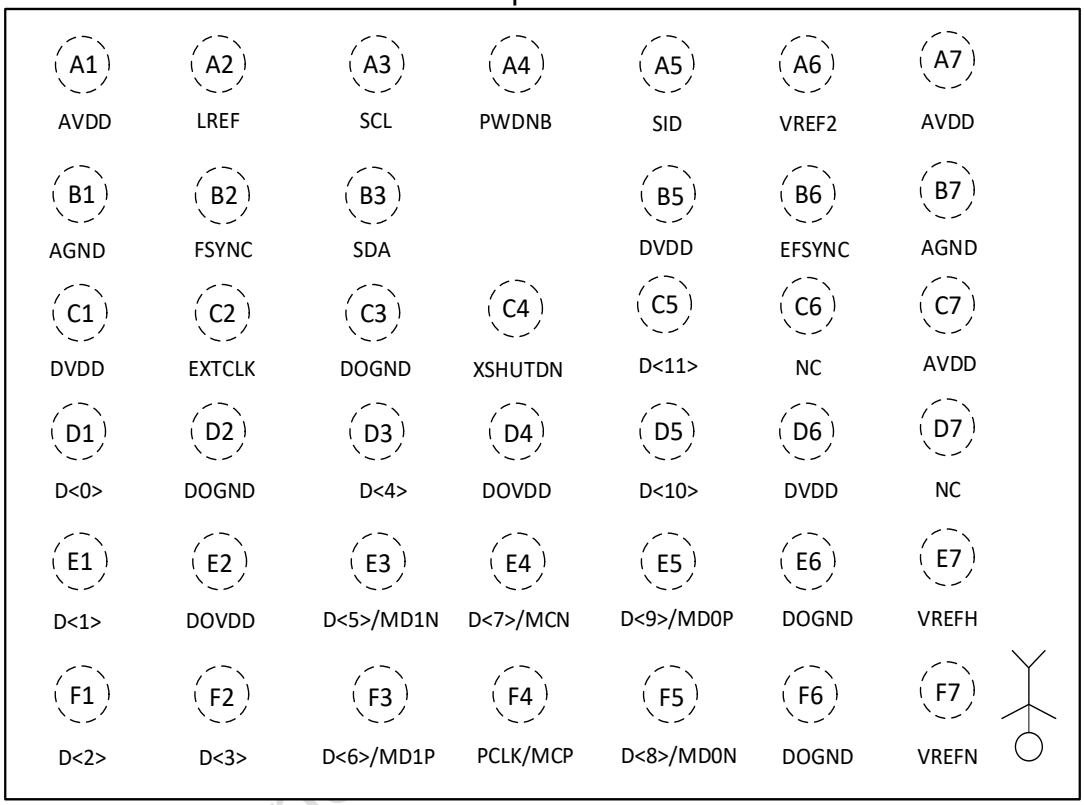

Figure 1-3 Top view of SC230AI package pin assignment

1.4. Chip Initialization

1.4.1. Power-up Timing

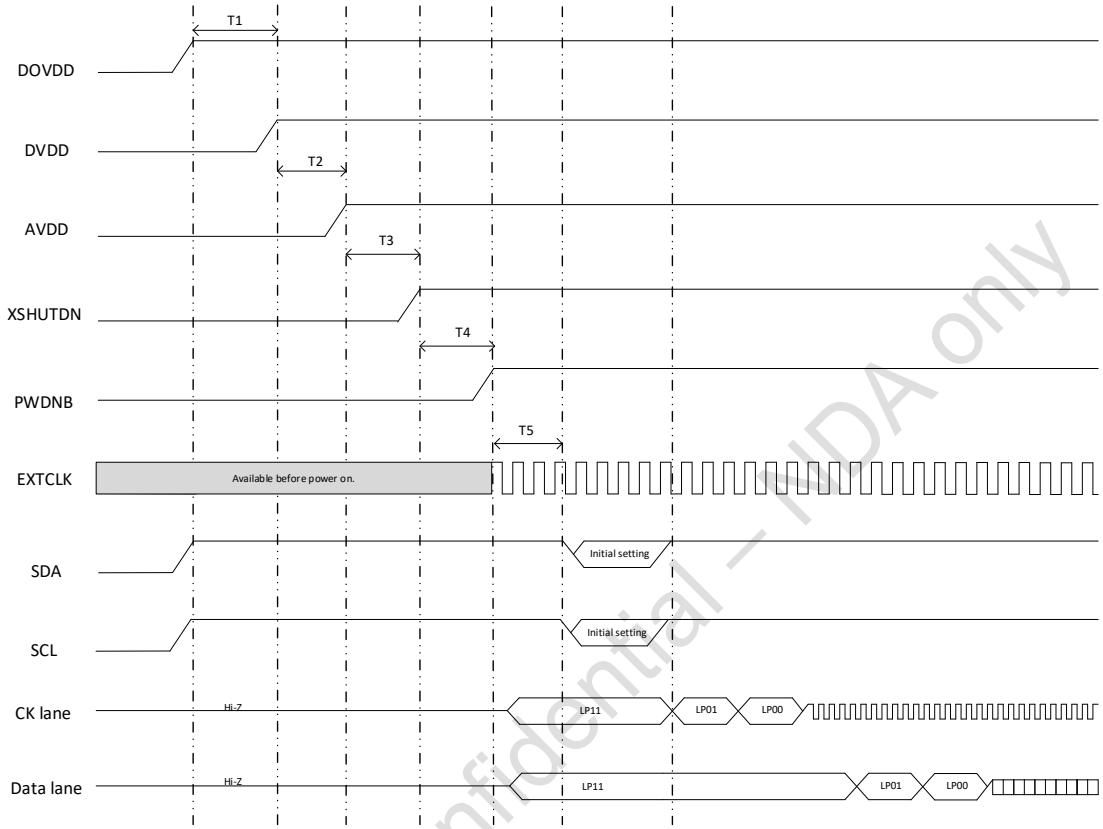

Figure 1-4 Power-up timing

Note: T1≥0ms, T2≥0ms, T3≥0ms, T4≥0ms, T5≥4ms.

1.4.2. Power-down Timing

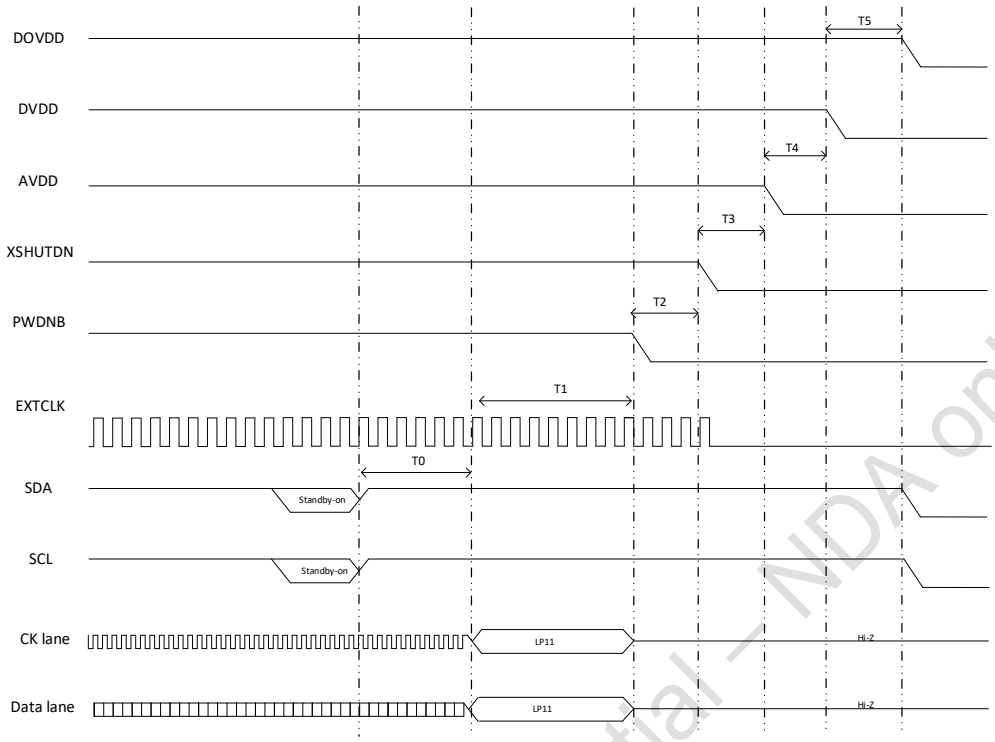

Figure 1-5 Power-down timing

Note: T0≥6EXTCLKs, T1≥0ms, T2≥0ms, T3≥0ms, T4≥0ms, T5≥0ms.

1.4.3. Sleep Mode

Under sleep mode, this chip stops output data, works in a low power status, and keeps registers unchanged. This chip offers two approaches to enter sleep mode:

1. Pull the PWDNB pin low, I²C read and write not supported.
2. Write register 16'h0100 [0] to 0, I²C access remains active.

Table 1-2 Sleep mode control register

Function	Address	Default Value	Description
Sleep mode by the software approach	16'h0100	8'h0	Bit[0]: manual sleep mode control 1: sleep mode disable 0: sleep mode enable

1.4.4. Reset Mode

During reset, this chip stops output data, works in a low power status, and resets its registers to their default values. This chip offers two approaches to reset:

1. Hard reset: pull the XSHUTDN pin low, registers access through I²C is not supported.
2. Soft reset: write 1 to register 16'h0103[0], reset mode lasts for 150 ns.

Table 1-3 Soft reset control register

Function	Address	Default Value	Description
Soft reset	16'h0103	8'h0	Bit[0]: soft reset

1.5. Configuration Interface

Registers of this chip can be read and written via the standard I²C bus. The I²C bus device address of the I²C interface is determined by the SID pin as shown in Table 1-4. The first line of Figure 1-6 shows a standard I²C communication protocol for 7-bit slave address, 16-bit sub address and 8-bit data. The slave address is the I²C bus device address, which is 7-bit. The R/W bit is either 1 for read or 0 for write. The 2 sub address bytes are the high byte and low byte of the 16-bit address of the register to be accessed. The second line of Figure 1-6 shows a write operation. The third line of Figure 1-6 shows a read operation. A dummy write operation is required to set the sub address (i.e. register address) before the read operation. Figure 1-7 shows the I²C timing diagram.

Table 1-4 I²C bus device address control

SID	7-bit I²C bus device address	8-bit I²C write address	8-bit I²C read address
LOW	7'h30	8'h60	8'h61
HIGH	7'h32	8'h64	8'h65

Standard I²C communication protocol

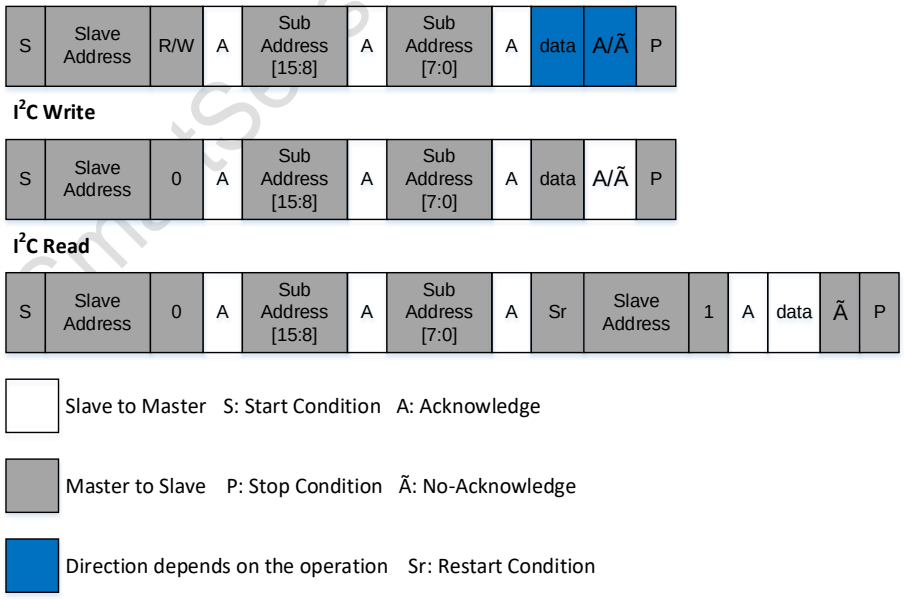

Figure 1-6 I²C standard protocol

I²C interface timing

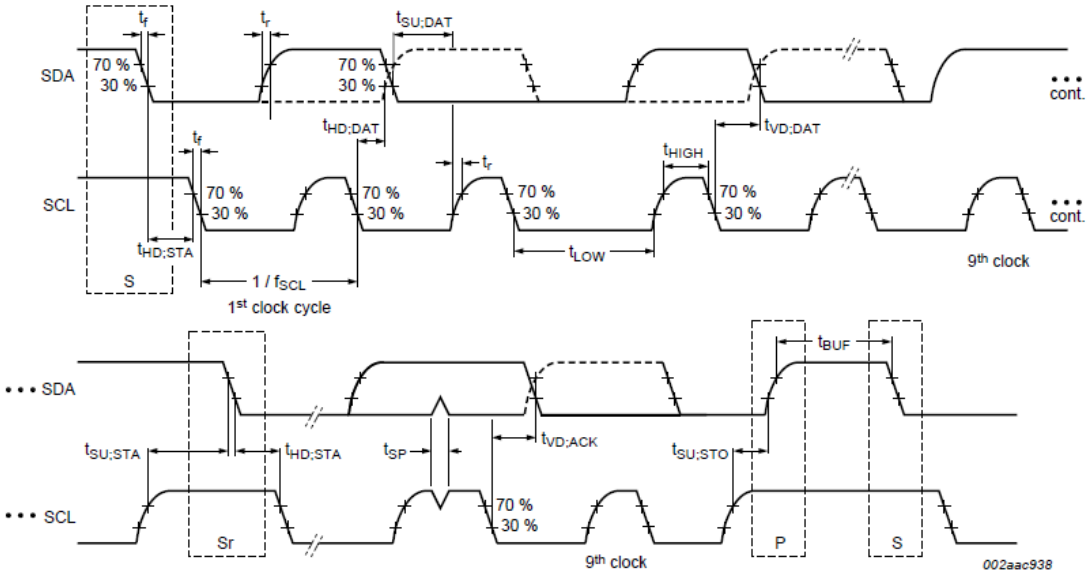

Figure 1-7 I²C interface timing

Table 1-5 I²C interface timing parameter

Symbol	Parameter	Standard-mode		Fast-mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition	4.0	-	0.6	-	μs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	μs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition	4.7	-	0.6	-	μs
$t_{HD;DAT}$	data hold time	0	-	0	-	μs
$t_{SU;DAT}$	data set-up time	250	-	100	-	ns
t_r	rise time of both SDA and SCL signals	-	1000	20	300	ns
t_f	fall time of both SDA and SCL signals	-	300	20	300	ns
$t_{SU;STO}$	set-up time for STOP condition	4.0	-	0.6	-	μs
t_{BUF}	bus free time between a STOP and START condition	4.7	-	1.3	-	μs
$t_{VD;DAT}$	data valid time	-	3.45	-	0.9	μs
$t_{VD;ACK}$	data valid acknowledge time	-	3.45	-	0.9	μs
t_{SP}	pulse width of spikes that must be suppressed by the input filter	-	-	0	50	ns

Note: The beginning of a rising edge and the end of a falling edge are at 30% of the amplitude of the signal. The end of a rising edge and the beginning of a falling edge are at 70% of the amplitude of the signal.

1.6. Sensor ID

Table 1-6 Sensor ID control register

Function	Register	Default Value	Description
SENSOR ID high	16'h3107	8'hcb	SENSOR ID [15:8]
SENSOR ID low	16'h3108	8'h34	SENSOR ID [7:0]

1.7. Data Interface

There are 2 types of data interfaces in this chip: the Digital Video Port (DVP) and the Mobile Industry Processor Interface (MIPI).

1.7.1. Digital Video Port (DVP)

This chip provides a Digital Video Port (DVP) that outputs 10-bit parallel data. A pulse signal indicating the start of data of a new frame is outputted from the FSYNC pin, line synchronization signals are outputted from the LREF pin, and the data clock signal is outputted from the PCLK pin. The period of the data clock signal equals to the period of the pixel clock T_{PCLK} (given by FAEs). Figure 1-8 shows the DVP timing diagram.

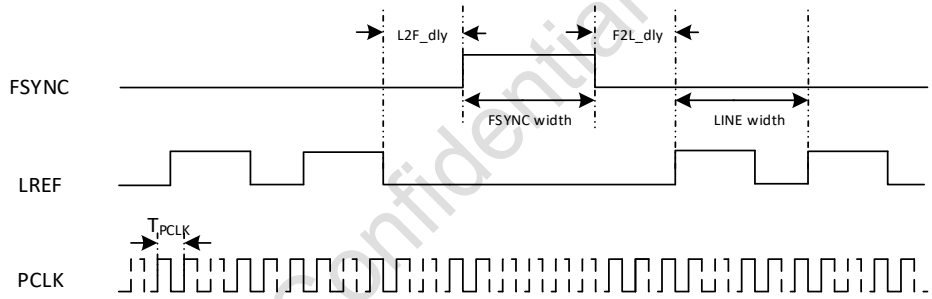

Figure 1-8 DVP timing diagram

Notes:

1) T_{PCLK} is the period of the PCLK signal.
2) L2F_dly is the delay between the falling edge of the last LREF signal and the rising edge of the FSYNC signal.
3) F2L_dly is the delay between the falling edge of the FSYNC signal and the rising edge of the first LREF signal.
4) Line width indicates the line width in the unit of number of T_{PCLK}, which is controlled by register {16'h320c, 16h'320d}.
5) FSYNC width is in the unit of number of lines. It equals to one line by default and is adjusted by register 16'h3d01.

Table 1-7 DVP timing control register

Function	Address	Default Value	Description
FSYNC output enable	16'h300a	8'h20	Bit[2]:FSYNC output enable 1~FSYNC as output PAD 0~FSYNC as input PAD
FSYNC signal width	16'h3d01	8'h01	FSYNC length
DVP signal polarity	16'h3d08	8'h01	Bit[2]: LREF polarity Bit[1]: FSYNC polarity Bit[0]: PCLK polarity
PAD driving capability	16'h3641	8'h00	Bit[1:0]: adjust PAD driver capability
PCLK delay	16'h3640	8'h00	Bit[1:0]: PCLK DLY 2ns/step

1.7.2. Mobile Industry Processor Interface (MIPI)

This chip provides a Mobile Industry Processor Interface (MIPI) which supports 8/10-bit, 1/2-lane data serial output with a speed of lower than 1.0 Gbps on each lane. Figure 1-9 shows the MIPI block diagram.

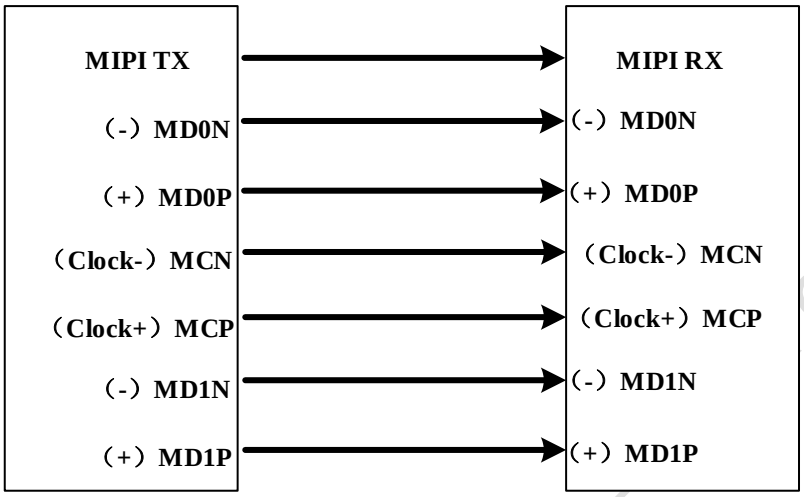

Figure 1-9 MIPI block diagram

Figure 1-10 is a brief diagram of an MIPI low level data packet, showing the transmission process of a short packet and a long packet. Figure 1-11 shows MIPI data packet structure diagrams for long and short packets. The Data Identifier (DI) is used to distinguish different packet types. Figure 1-12 shows the data packet transmission diagram of MIPI working in 1/2-lane. In Figure 1-13, DI consists of two parts, Virtual Channel (VC) and Data Type (DT). By default, the VC value of MIPI data given by this chip is 0, and the DT values are shown in Table 1-8.

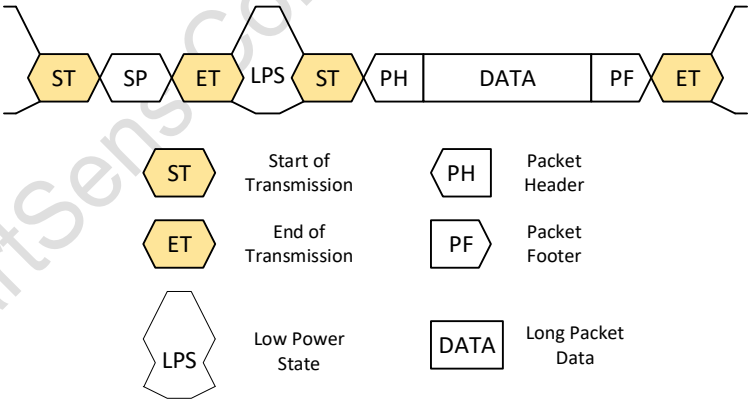

Figure 1-10 MIPI data packet

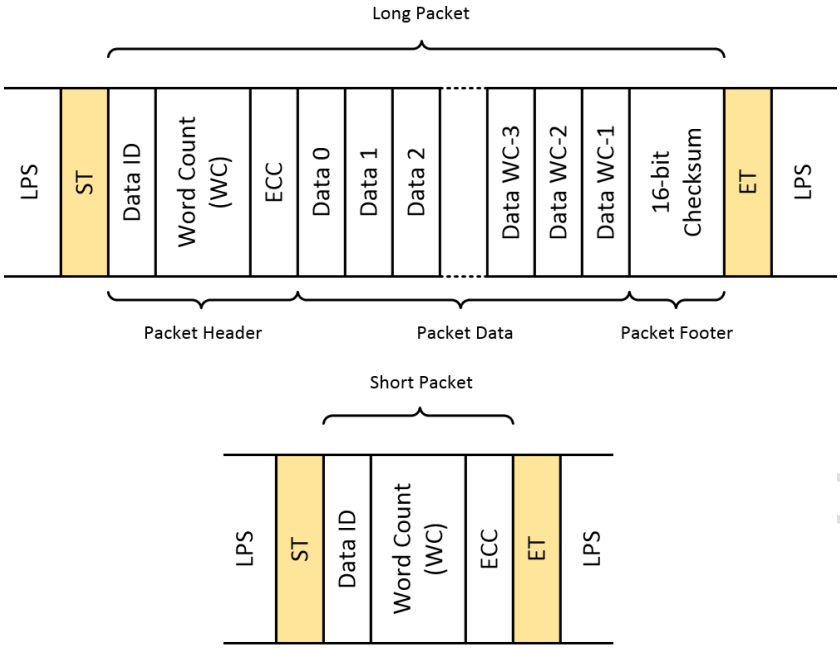

Figure 1-11 MIPI long/short packet structure diagram

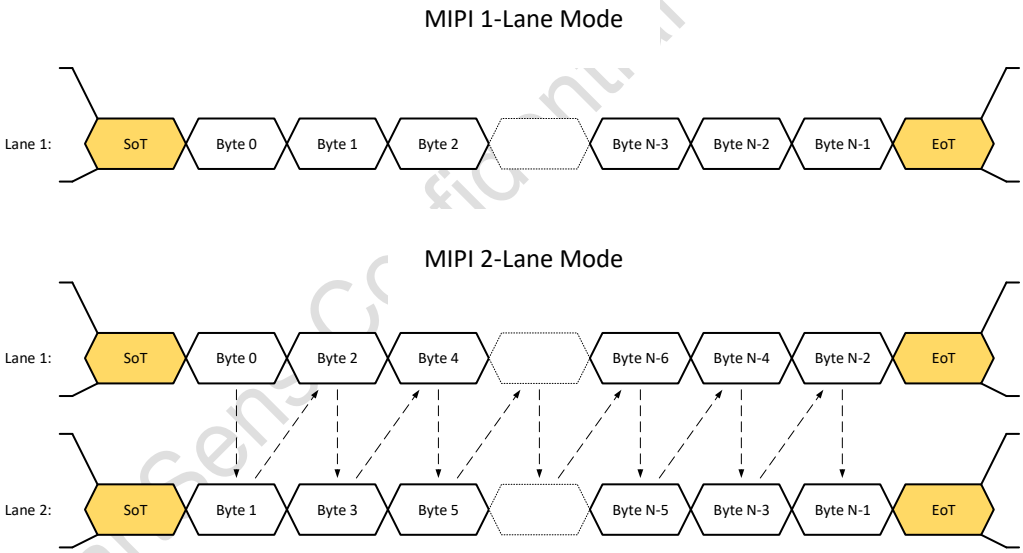

Figure 1-12 MIPI 1/2-lane data package transmission diagram

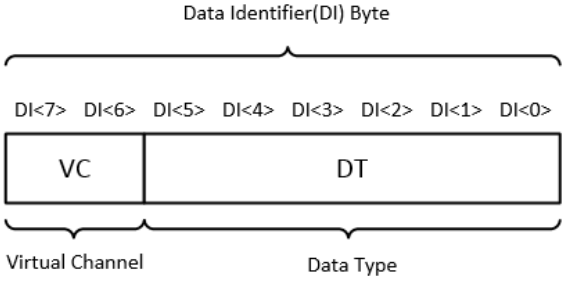

Figure 1-13 MIPI data packet DI structure

Table 1-8 MIPI data type

DT	Description
6'h00	Frame start short packet

6’h01	Frame end short packet
6’h02	Row start short packet
6’h03	Row end short packet
6’h2a	8-bit data long packet
6’h2b	10-bit data long packet

Table 1-9 MIPI control registers

Function	Address	Default Value	Description
MIPI lane number	16’h3018	8’h32	Bit[7:5]: MIPI lane num-1 3’h0 ~ 1 lane mode 3’h1 ~ 2 lane mode
MIPI output data mode	16’h3031	8’h0a	Bit[3:0]: MIPI bit mode 4’h8 ~ raw8 mode 4’ha ~ raw10 mode
PHY data mode	16’h3037	8’h20	Bit[6:5]: phy bit mode 2’h0 ~ 8bit mode 2’h1 ~ 10bit mode
MIPI clock setting	16’h303f	8’h01	Bit[7]: pclk sel 1’h0 ~ sel MIPI_pclk 1’b1 ~ sel DVP_pclk
MIPI data enabling	16’h4603	8’h08	Bit[0]: MIPI read 1’h1 ~ disable 1’h0 ~ enable
MIPI LP driving	16’h3651	8’h7d	Bit[2:1]: MIPI LP driving capability adjustment, the default value is 3’h1
MIPI Lane 0 delay	16’h3652	8’h00	Bit[3]: lane0 invert, the default value is 1’h0 Bit[2:0]: lane0 delay, 40 ps/step, the default value is 3’h0
MIPI Lane 1 delay	16’h3652	8’h00	Bit[7]: lane1 invert, the default value is 1’h0 Bit[6:4]: lane1 delay, 40 ps/step, the default value is 3’h0
MIPI Clock delay	16’h3654	8’h00	Bit[3]: clock invert, the default value is 1’h0 Bit[2:0]: clock delay, 40 ps/step, the default value is 3h0

1.8. Phase Locked Loop (PLL)

The input clock frequency of the PLL module ranges from 6 MHz to 40 MHz, while the VCO output frequency (F_{VCO}) ranges from 400 MHz to 1200 MHz. The PLL block diagram is shown in Figure 1-14.

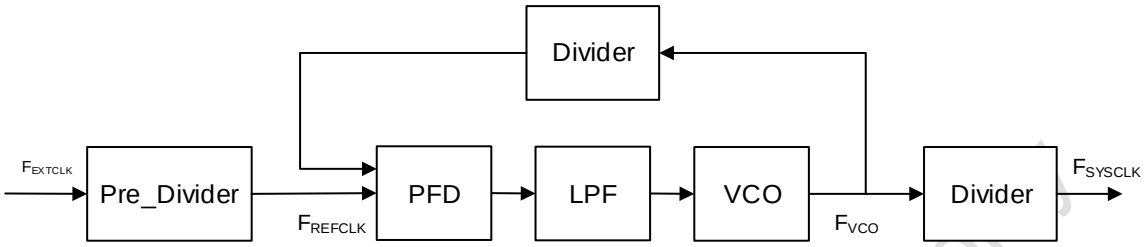

Figure 1-14 PLL control diagram

2. Function Introduction

2.1. Slave Mode

In the slave mode, data output of this chip is triggered by an external signal applied to the EFSYNC pin or FSYNC to achieve synchronization of multiple sensors. The frame rate is determined by the triggering signal. Figure 2-1 shows the timing diagram of the slave mode which consists of the following time intervals: Active State, RB Rows, Active Rows, Blank Rows, and Extra Delays. The exposure implementation in the slave mode is shown in Figure 2-2.

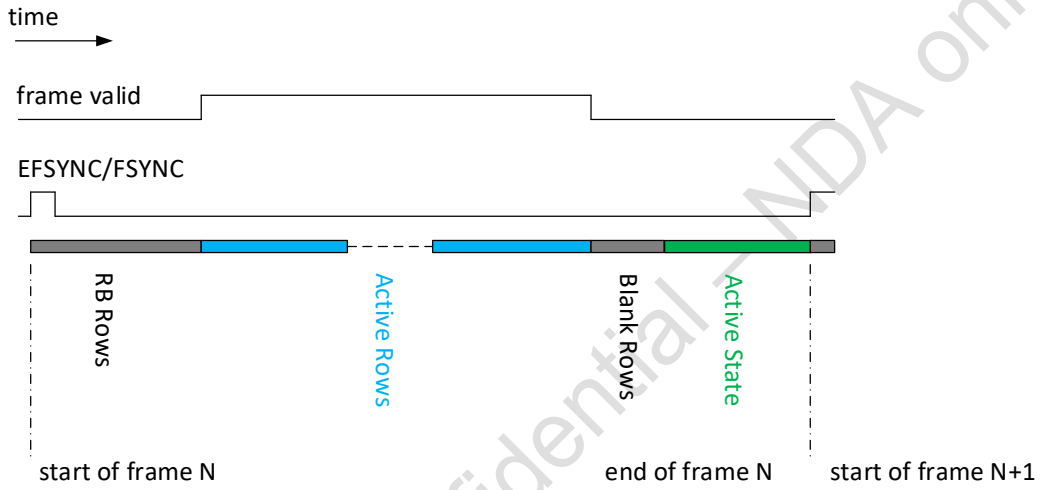

Figure 2-1 Slave mode timing diagram

From Figure 2-1, the slave mode workflow can be detailed as follows:

1) When the chip operates in the slave mode, the chip automatically enters Active State and waits for a trigger from the EFSYNC/FSYNC pin.
2) EFSYNC/FSYNC is active after triggering the rising edge, the duration of EFSYNC high level is not less than 4 EXTCLK cycles.
3) Upon triggering through EFSYNC/FSYNC, the chip enters RB Rows, which is the waiting time before the reading of valid data. The waiting time is controlled by registers. The value of the registers is in the unit of row.
4) During Active Rows, image data can be read. The value of the registers is in the unit of row.
5) During Blank Rows, blanking time after the image data can be read. The first and last rows to be read are controlled by registers. The value of the registers is in the unit of row.
6) During Active State, the chip waits for next triggering through the EFSYNC/FSYNC pin. The Active State should be as minimum as possible, which is proposed to be 0;
7) The rising edge interval of EFSYNC/FSYNC is one frame, and 40 ns deviation is allowed for EFSYNC/FSYNC rising edge interval.

Notes:

1) Triggering through the EFSYNC/FSYNC pin is valid only when the chip enters Active State.

2) The chip will withdraw from Blank Rows 40 ns in advance and enter into Active State

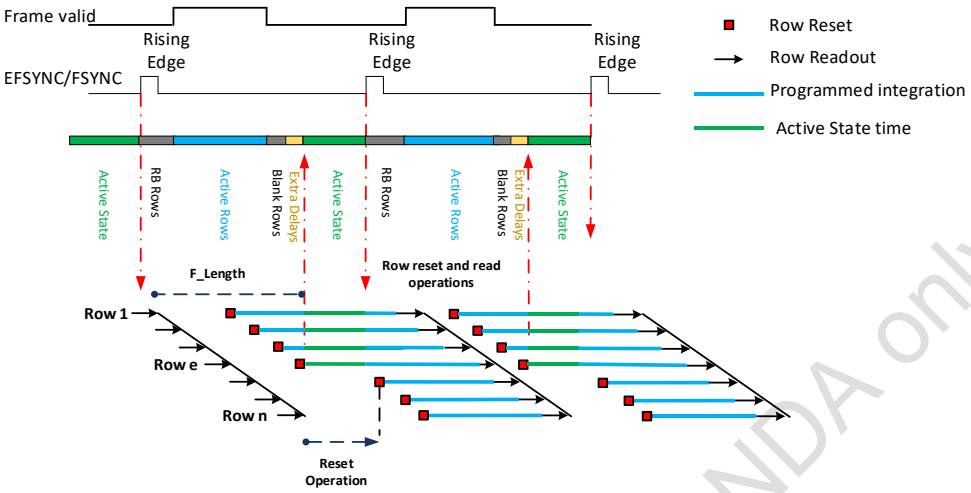

Figure 2-2 Slave mode exposure implementation chart

The exposure in the slave mode is shown in Figure 2-2.

Notes:

1) Row Reset starts exposure operation, ends exposure operation before Row Readout starts, including Active State time;

2) VTS represents frame length, VTS= RB Rows + Active Rows + Blank Rows;

3) During Active State, the chip stops output and stops the Row reset operation, as shown in Figure 2-2. This will result in exposure time being different in a frame image such that the exposure Row1 to Row e and Row (e + 1) to Row n having different integration time, resulting in the exposure time of Row 1 ~ Row e being larger than the Row (e+1) - Row n. The time difference is Active State time as shown as Reset Operation time in the diagram. In order to avoid this exposure difference, the external high precision control EFSYNC/FSYNC is required to keep the Active State within 40ns, ensuring the exposure time of each row in one frame is basically consistent.

4) When RB Rows is greater than the exposure time, the inconsistencies in the in-frame exposure time in Note 3) do not occur, and the exposure time in each row in one frame is the same. At this time, the EFSYNC/FSYNC pin can achieve simultaneous exposure.

Table 2-1 Slave mode control register

Function	Register Address	Default Value	Description
Slave mode enable	16'h3222	8'h00	Bit[1]: Slave mode enable control 1~slave mode 0~master mode
Merge enable	16'h3225	8'h20	Bit[4]: Active Rows Blank Rows merge enable
Trigger Pad sel	16'h3224	8'h82	Bit[4]: trigger pad sel 1 ~ sel FSYNC 0 ~ sel EFSYNC
FSYNC OEN	16'h300a	8'h20	Bit[2]: FSYNC output en 1 ~ FSYNC as output PAD 0 ~ FSYNC as input PAD
RB rows	{16'h3230,16'h3231}	16'h0004	Rows Before Read control register
Active Rows, Blank Rows	-	-	Active Rows + Blank Rows = VTS - RB Rows
VTS	{16'h320e,16'h320f}	16'h0465	Frame length

2.2. High Dynamic Range (HDR)

The SC230AI HDR merges two frames of the same scene with different exposure time into one frame in order to enhance the dynamic range of an image. The SC230AI supports staggered HDR.

2.2.1. Staggered HDR

The SC230AI staggered HDR means that two images with different exposure time are outputted alternately within one frame. The advantage of the SC230AI staggered HDR is the shortening of the gap between the long and short exposure time of the same pixel. As a result, the motion artifact can be reduced during HDR synthesis.

The long and short exposure data can be distinguished through the virtual channel of the SC230AI MIPI. By default, the long exposure data virtual channel is 2'b00, and the short exposure data virtual channel is 2'b01.

The timing diagram of the SC230AI staggered HDR using virtual channel data readout is shown in Figure 2-3.

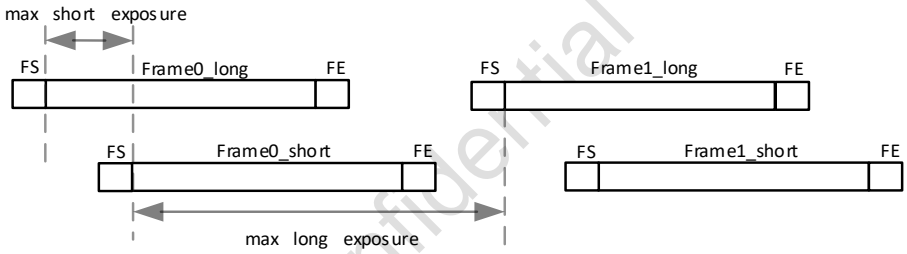

Figure 2-3 Staggered HDR with virtual channel readout timing

The SC230AI can also distinguish the long and short exposure data without using the virtual channel, but by the data readout sequence difference. Two modes are supported: mode a and mode b. When operating in mode a, only valid video data are outputted for the long and short exposures. When operating in mode b, dummy pixels will be inserted for invalid short exposure data when long exposure data is being outputted, and for invalid long exposure data when short exposure data is being outputted.

The timing diagram of the SC230AI staggered HDR without using virtual channel data readout (mode a) and (mode b) are shown in Figure 2-4 and Figure 2-5 respectively.

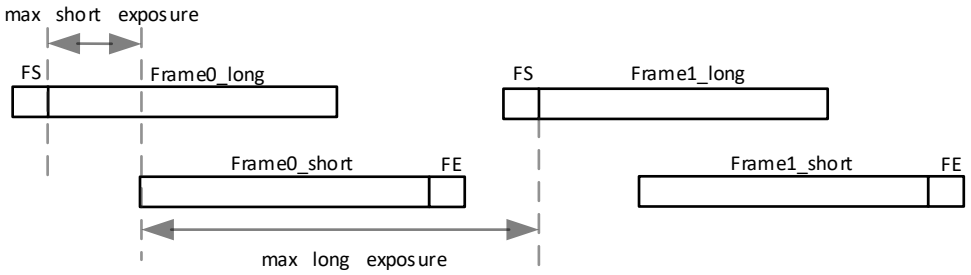

Figure 2-4 Timing diagram for staggered HDR without using virtual channel (mode a)

Notes:

1) Long exposure data and short exposure data are output alternately in rows. max short exposure / 2-row long exposure data is output first, then long exposure data and short exposure data are output alternately in rows, and finally max short exposure / 2-row short exposure data is output.

2) max long exposure = frame length ({16'h320e,16'h320f}) - max short exposure.

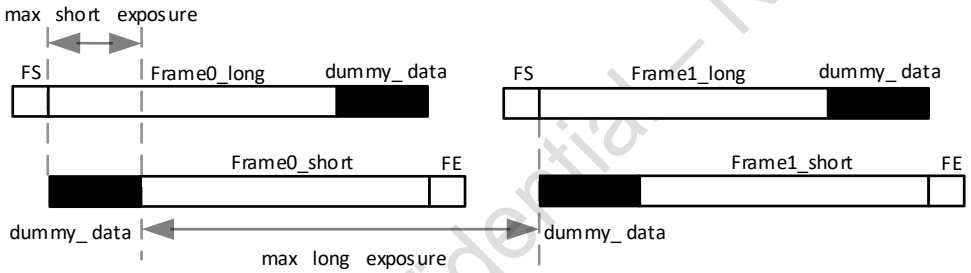

Figure 2-5 Timing diagram for staggered HDR without using virtual channel (mode b)

Table 2-2 HDR control registers

Function	Register address	Default value	Description
HDR mode enable	16'h3281	8'h00	Bit[0]: HDR mode enable control 1~HDR mode enable 0~HDR mode disable
MAX short exposure	{16'h3e23,16'h3e24}	16'h013e	Max short exposure
VC(Virtual Channel)	16'h4816	8'h61	Bit[4]: vc_s_en 1 ~ short frame vc enable 0 ~ short frame vc disable Bit[3:2] :vc_l In HDR mode, vc_l is long frame vc In non-HDR mode, vc_l is normal vc Bit[1:0]:vc_s In HDR mode, vc_s is short frame vc In non-HDR mode, vc_s is reserved
In HDR no virtual channel mode select	16'h4503, 16'h3928, 16'h5002	8'h20 8'hc1 8'h06	16'h4503[6]: sync href always enable 16'h3928[1]: blc keep black href 16'h5002[0]: isp dumy mode

2.3. AEC/AGC

The AEC/AGC adjustment is based on the brightness. AEC adjusts the exposure time while AGC adjusts the gain value so that the image's brightness can fall within the target range of a given brightness threshold.

2.3.1. AEC/AGC adjustment strategy

This chip does not have the AEC/AGC function, so a back-end platform is needed in order to achieve AEC/AGC.

During the AEC/AGC adjustment process, sensor exposure time or gain should not be adjusted independently. A recommended adjustment strategy is as follows: adjust the exposure time first, and then the gain if the exposure time has reached its maximum.

For example, when adjusting a dark scene, the sequence of adjustment is: 1) do not turn on any gain until the exposure time reaches its maximum; 2) when the exposure time reaches its maximum, automatic gain control can be adjusted. It is important to note that when the gain is applied, the average image noise also increases. But when the exposure time increases, the signal-to-noise ratio will improve.

On the other hand, when the image is too bright, the gain should be reduced first. If all gains are disabled and the image is still too bright, the exposure time can be reduced to properly expose the scene.

The exposure time and gain are interrelated. They should be considered at the same time during system adjustment.

2.3.2. AEC control registers

AEC control registers are listed in Table 2-3.

Table 2-3 Manual control registers

Function	Register Address	Description	Adjustment Step	Min	Max
Long exposure time	{16'h3e00[3:0] 16'h3e01[7:0], 16'h3e02[7:4]}	Manual exposure time under linear mode, in the unit of half line	1	2	2*{16'h320e,16'h320f} - 'd9
		Long exposure time under staggered HDR mode, in the unit of half line	4	2	2*{16'h320e,16'h320f} - 2*{16'h3e23,16'h3e24} - 'd17
Short exposure time	{16'h3e22[3:0] 16'h3e04[7:0], 16'h3e05[7:4]}	Short exposure time under staggered HDR mode, in the unit of half line	4	2	2*{16'h3e23,16'h3e24} - 'd15

For AEC control, please refer to the following instructions:

1) The adjustment step of AEC is calculated in the unit of half line, half-line time equals to one-line time divided by 2, and the calculation method of one-line time is referred to Section 2.7;

2) If the exposure time and gain are written in the N^{th} frame, they are effective on the $(N+2)^{th}$ frame.

3) Writing point of exposure time and gain: writing is recommended after the start of the frame in linear mode. Under staggered HDR, writing for long exposure data is recommended after the start of the long exposure data frame, and writing for short exposure data is recommended after the start of the short exposure data frame.

2.3.3. AGC control registers

AGC control registers are listed in Table 2-4.

Table 2-4 Gain control registers

Mode	ANA GAIN register	DIG GAIN register	DIG FINE GAIN register
Long exposure under linear mode/HDR mode	16'h3e09	16'h3e06	16'h3e07
Short exposure under HDR mode	16'h3e13	16'h3e10	16'h3e11

For AGC control, the values of the analog gain and the digital gain are shown in

Table 2-5 and Table 2-6 respectively. In general, the analog gain should be increased first. If the brightness is required to be further increased when the analog gain is increased to the maximum, the digital gain can be increased. The accuracy of the DIG FINE gain of this chip is 1/128. Taking a precision of 1/64 as an example, the digital gain is listed in Table 2-6.

Since the analog gain only has coarse gain, and has no fine gain, so in the adjustment of analog gain, the DIG FINE GAIN (1 ~ 2 times) needs to replace analog fine gain for smooth transition and avoid AGC oscillation.

Table 2-5 Analog gain control registers

ANA GAIN	GAIN Value	dB Value
8'h00	1.000	0.000
8'h01	2.000	6.021
8'h40	3.100	9.827
8'h48	6.200	15.848
8'h49	12.400	21.868
8'h4b	24.800	27.889
8'h4f	49.600	33.910
8'h5f	99.200	39.930

Table 2-6 Digital gain control registers

DIG GAIN	DIG FINE GAIN	GAIN value	dB value	DIG GAIN	DIG FINE GAIN	GAIN value	dB value
8'h00	8'h80	1.000	0.00	8'h00	8'hd2	1.641	4.30
8'h00	8'h82	1.016	0.13	8'h00	8'hd4	1.656	4.38
8'h00	8'h84	1.031	0.27	8'h00	8'hd6	1.672	4.46
8'h00	8'h86	1.047	0.40	8'h00	8'hd8	1.688	4.54
8'h00	8'h88	1.063	0.53	8'h00	8'hda	1.703	4.62
8'h00	8'h8a	1.078	0.65	8'h00	8'hdc	1.719	4.70
8'h00	8'h8c	1.094	0.78	8'h00	8'hde	1.734	4.78
8'h00	8'h8e	1.109	0.90	8'h00	8'he0	1.750	4.86
8'h00	8'h90	1.125	1.02	8'h00	8'he2	1.766	4.94
8'h00	8'h92	1.141	1.14	8'h00	8'he4	1.781	5.01
8'h00	8'h94	1.156	1.26	8'h00	8'he6	1.797	5.09
8'h00	8'h96	1.172	1.38	8'h00	8'he8	1.813	5.17
8'h00	8'h98	1.188	1.49	8'h00	8'hea	1.828	5.24
8'h00	8'h9a	1.203	1.61	8'h00	8'hec	1.844	5.31
8'h00	8'h9c	1.219	1.72	8'h00	8'hee	1.859	5.39
8'h00	8'h9e	1.234	1.83	8'h00	8'hf0	1.875	5.46
8'h00	8'ha0	1.250	1.94	8'h00	8'hf2	1.891	5.53
8'h00	8'ha2	1.266	2.05	8'h00	8'hf4	1.906	5.60
8'h00	8'ha4	1.281	2.15	8'h00	8'hf6	1.922	5.67
8'h00	8'ha6	1.297	2.26	8'h00	8'hf8	1.938	5.74
8'h00	8'ha8	1.313	2.36	8'h00	8'hfa	1.953	5.81
8'h00	8'haa	1.328	2.46	8'h00	8'hfc	1.969	5.88
8'h00	8'hac	1.344	2.57	8'h00	8'hfe	1.984	5.95
8'h00	8'hae	1.359	2.67	8'h01	8'h80	2.000	6.02
8'h00	8'hb0	1.375	2.77	8'h01	8'h82	2.031	6.16
8'h00	8'hb2	1.391	2.86	8'h01	8'h84	2.063	6.29
8'h00	8'hb4	1.406	2.96	8'h01	8'h86	2.094	6.42
8'h00	8'hb6	1.422	3.06	8'h01	8'h88	2.125	6.55
8'h00	8'hb8	1.438	3.15	8'h01	8'h8a	2.156	6.67
8'h00	8'hba	1.453	3.25	8'h01	8'h8c	2.188	6.80
8'h00	8'hbc	1.469	3.34	8'h01	8'h8e	2.219	6.92
8'h00	8'hbe	1.484	3.43	8'h01	8'h90	2.250	7.04
8'h00	8'hc0	1.500	3.52	8'h01	8'h92	2.281	7.16
8'h00	8'hc2	1.516	3.61	8'h01	8'h94	2.313	7.28
8'h00	8'hc4	1.531	3.70	8'h01	8'h96	2.344	7.40
8'h00	8'hc6	1.547	3.79	8'h01	8'h98	2.375	7.51
8'h00	8'hc8	1.563	3.88	8'h01	8'h9a	2.406	7.63
8'h00	8'hca	1.578	3.96	8'h01	8'h9c	2.438	7.74
8'h00	8'hcc	1.594	4.05	8'h01	8'h9e	2.469	7.85
8'h00	8'hce	1.609	4.13	8'h01	8'ha0	2.500	7.96
8'h00	8'hd0	1.625	4.22	8'h01	8'ha2	2.531	8.07

DIG GAIN	DIG FINE GAIN	GAIN value	dB value	DIG GAIN	DIG FINE GAIN	GAIN value	dB value
8'h01	8'ha4	2.563	8.17	8'h01	8'hf6	3.844	11.70
8'h01	8'ha6	2.594	8.28	8'h01	8'hf8	3.875	11.77
8'h01	8'ha8	2.625	8.38	8'h01	8'hfa	3.906	11.84
8'h01	8'haa	2.656	8.49	8'h01	8'hfc	3.938	11.90
8'h01	8'hac	2.688	8.59	8'h01	8'hfe	3.969	11.97
8'h01	8'hae	2.719	8.69	8'h03	8'h80	4.000	12.04
8'h01	8'hb0	2.750	8.79	8'h03	8'h82	4.063	12.18
8'h01	8'hb2	2.781	8.88	8'h03	8'h84	4.125	12.31
8'h01	8'hb4	2.813	8.98	8'h03	8'h86	4.188	12.44
8'h01	8'hb6	2.844	9.08	8'h03	8'h88	4.250	12.57
8'h01	8'hb8	2.875	9.17	8'h03	8'h8a	4.313	12.69
8'h01	8'hba	2.906	9.27	8'h03	8'h8c	4.375	12.82
8'h01	8'hbc	2.938	9.36	8'h03	8'h8e	4.438	12.94
8'h01	8'hbe	2.969	9.45	8'h03	8'h90	4.500	13.06
8'h01	8'hc0	3.000	9.54	8'h03	8'h92	4.563	13.18
8'h01	8'hc2	3.031	9.63	8'h03	8'h94	4.625	13.30
8'h01	8'hc4	3.063	9.72	8'h03	8'h96	4.688	13.42
8'h01	8'hc6	3.094	9.81	8'h03	8'h98	4.750	13.53
8'h01	8'hc8	3.125	9.90	8'h03	8'h9a	4.813	13.65
8'h01	8'hca	3.156	9.98	8'h03	8'h9c	4.875	13.76
8'h01	8'hcc	3.188	10.07	8'h03	8'h9e	4.938	13.87
8'h01	8'hce	3.219	10.15	8'h03	8'ha0	5.000	13.98
8'h01	8'hd0	3.250	10.24	8'h03	8'ha2	5.063	14.09
8'h01	8'hd2	3.281	10.32	8'h03	8'ha4	5.125	14.19
8'h01	8'hd4	3.313	10.40	8'h03	8'ha6	5.188	14.30
8'h01	8'hd6	3.344	10.48	8'h03	8'ha8	5.250	14.40
8'h01	8'hd8	3.375	10.57	8'h03	8'haa	5.313	14.51
8'h01	8'hda	3.406	10.65	8'h03	8'hac	5.375	14.61
8'h01	8'hdc	3.438	10.72	8'h03	8'hae	5.438	14.71
8'h01	8'hde	3.469	10.80	8'h03	8'hb0	5.500	14.81
8'h01	8'he0	3.500	10.88	8'h03	8'hb2	5.563	14.91
8'h01	8'he2	3.531	10.96	8'h03	8'hb4	5.625	15.00
8'h01	8'he4	3.563	11.04	8'h03	8'hb6	5.688	15.10
8'h01	8'he6	3.594	11.11	8'h03	8'hb8	5.750	15.19
8'h01	8'he8	3.625	11.19	8'h03	8'hba	5.813	15.29
8'h01	8'hea	3.656	11.26	8'h03	8'hbc	5.875	15.38
8'h01	8'hec	3.688	11.33	8'h03	8'hbe	5.938	15.47
8'h01	8'hee	3.719	11.41	8'h03	8'hc0	6.000	15.56
8'h01	8'hf0	3.750	11.48	8'h03	8'hc2	6.063	15.65
8'h01	8'hf2	3.781	11.55	8'h03	8'hc4	6.125	15.74
8'h01	8'hf4	3.813	11.62	8'h03	8'hc6	6.188	15.83

DIG GAIN	DIG FINE GAIN	GAIN value	dB value	DIG GAIN	DIG FINE GAIN	GAIN value	dB value
8'h03	8'hc8	6.250	15.92	8'h07	8'h9a	9.625	19.67
8'h03	8'hca	6.313	16.00	8'h07	8'h9c	9.750	19.78
8'h03	8'hcc	6.375	16.09	8'h07	8'h9e	9.875	19.89
8'h03	8'hce	6.438	16.17	8'h07	8'ha0	10.000	20.00
8'h03	8'hd0	6.500	16.26	8'h07	8'ha2	10.125	20.11
8'h03	8'hd2	6.563	16.34	8'h07	8'ha4	10.250	20.21
8'h03	8'hd4	6.625	16.42	8'h07	8'ha6	10.375	20.32
8'h03	8'hd6	6.688	16.51	8'h07	8'ha8	10.500	20.42
8'h03	8'hd8	6.750	16.59	8'h07	8'haa	10.625	20.53
8'h03	8'hda	6.813	16.67	8'h07	8'hac	10.750	20.63
8'h03	8'hdc	6.875	16.75	8'h07	8'hae	10.875	20.73
8'h03	8'hde	6.938	16.82	8'h07	8'hb0	11.000	20.83
8'h03	8'he0	7.000	16.90	8'h07	8'hb2	11.125	20.93
8'h03	8'he2	7.063	16.98	8'h07	8'hb4	11.250	21.02
8'h03	8'he4	7.125	17.06	8'h07	8'hb6	11.375	21.12
8'h03	8'he6	7.188	17.13	8'h07	8'hb8	11.500	21.21
8'h03	8'he8	7.250	17.21	8'h07	8'hba	11.625	21.31
8'h03	8'hea	7.313	17.28	8'h07	8'hbc	11.750	21.40
8'h03	8'hec	7.375	17.36	8'h07	8'hbe	11.875	21.49
8'h03	8'hee	7.438	17.43	8'h07	8'hc0	12.000	21.58
8'h03	8'hf0	7.500	17.50	8'h07	8'hc2	12.125	21.67
8'h03	8'hf2	7.563	17.57	8'h07	8'hc4	12.250	21.76
8'h03	8'hf4	7.625	17.64	8'h07	8'hc6	12.375	21.85
8'h03	8'hf6	7.688	17.72	8'h07	8'hc8	12.500	21.94
8'h03	8'hf8	7.750	17.79	8'h07	8'hca	12.625	22.02
8'h03	8'hfa	7.813	17.86	8'h07	8'hcc	12.750	22.11
8'h03	8'hfc	7.875	17.93	8'h07	8'hce	12.875	22.19
8'h03	8'hfe	7.938	17.99	8'h07	8'hd0	13.000	22.28
8'h07	8'h80	8.000	18.06	8'h07	8'hd2	13.125	22.36
8'h07	8'h82	8.125	18.20	8'h07	8'hd4	13.250	22.44
8'h07	8'h84	8.250	18.33	8'h07	8'hd6	13.375	22.53
8'h07	8'h86	8.375	18.46	8'h07	8'hd8	13.500	22.61
8'h07	8'h88	8.500	18.59	8'h07	8'hda	13.625	22.69
8'h07	8'h8a	8.625	18.72	8'h07	8'hdc	13.750	22.77
8'h07	8'h8c	8.750	18.84	8'h07	8'hde	13.875	22.84
8'h07	8'h8e	8.875	18.96	8'h07	8'he0	14.000	22.92
8'h07	8'h90	9.000	19.08	8'h07	8'he2	14.125	23.00
8'h07	8'h92	9.125	19.20	8'h07	8'he4	14.250	23.08
8'h07	8'h94	9.250	19.32	8'h07	8'he6	14.375	23.15
8'h07	8'h96	9.375	19.44	8'h07	8'he8	14.500	23.23
8'h07	8'h98	9.500	19.55	8'h07	8'hea	14.625	23.30

DIG GAIN	DIG FINE GAIN	GAIN value	dB value	DIG GAIN	DIG FINE GAIN	GAIN value	dB value
8'h07	8'hec	14.750	23.38	8'h07	8'hf6	15.375	23.74
8'h07	8'hee	14.875	23.45	8'h07	8'hf8	15.500	23.81
8'h07	8'hf0	15.000	23.52	8'h07	8'hfa	15.625	23.88
8'h07	8'hf2	15.125	23.59	8'h07	8'hfc	15.750	23.95
8'h07	8'hf4	15.250	23.67	8'h07	8'hfe	15.875	24.01

2.4. Group Hold

Group hold refers to the packing of a group of registers to be effective at a specific time within a frame. In this chip, the maximum number of registers within the group is 10. Frame delay is supported and can be controlled by a register.

The procedure of packing a group is as follows. First, set register 16'h3812 to 8'h00 to start packing the group. Then write the required values to registers of the group. Finally set register 16'h3812 to 8'h30 to end packing the group. Registers in the group are effective with a delay of N frames when setting register 16'h3812 to 8'h30, where N is the value of register 16'h3802. N = 0 means the current frame. N = 1 means the next frame and so on.

Table 2-7 Group hold control registers

Function	Address	Default Value	Description
Frame delay control	16'h3802	8'h00	Bit [3:0]: Determine the number of frames to be delayed before the group of registers is effective. Setting to 0 implies the current frame. Setting to N implies a delay of N frames.

2.5. Defective Pixel Correction (DPC)

This chip supports the Defective Pixel Correction (DPC) feature. A pixel is regarded as defective if the value of the pixel is greater (or smaller) than its surrounding pixels with the same color, and the difference is greater than the set threshold. A defective pixel may be classified as a white pixel or a black pixel. The corresponding control registers are shown in Table 2-8.

Table 2-8 DPC registers

Function	Description	Address	Default Value	Description
White pixel correction	Long/short exposure under linear mode/staggered HDR mode	16'5000[2]	1'b1	white dead pixel cancellation enable 1 ~ enable 0 ~ disable
Black pixel correction	Long/short exposure under linear mode/staggered HDR mode	16'5000[1]	1'b1	black dead pixel cancellation enable 1 ~ enable 0 ~ disable

2.6. Video output Mode

2.6.1. Read Order

Below figure shows the location of the first read pixel as well as the entire array structure. This figure shows the top view when the A1 pin is placed in the upper left corner. The figure below shows the first pixel data color format.

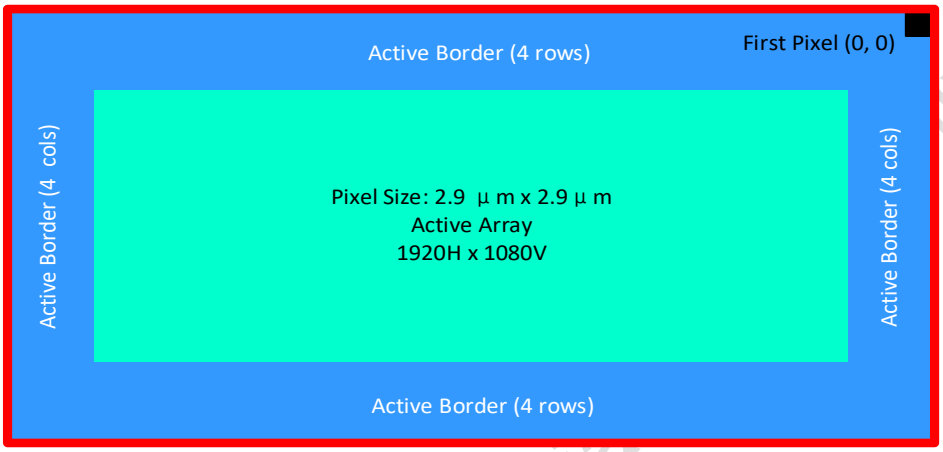

Figure 2-6 Pixel array 1

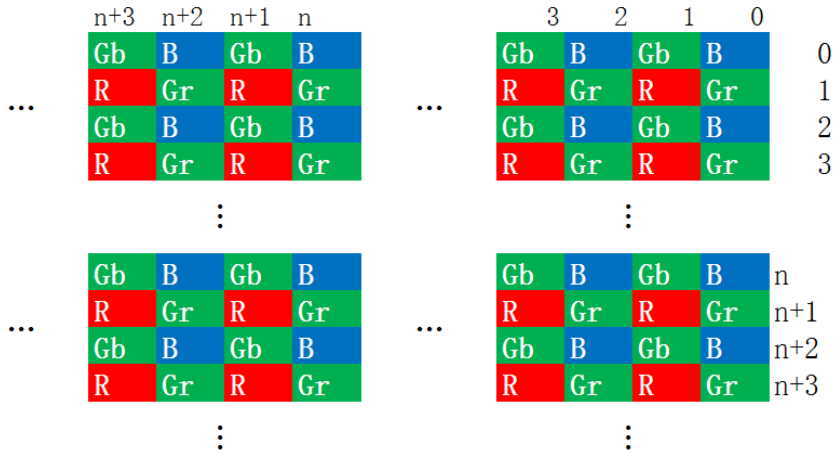

Figure 2-7 Pixel array 2

This chip supports the mirror mode and the flip mode. The mirror mode reverses the sensor data read out order, and the flip mode vertically reverses the sensor readout order, as shown in Figure 2-8.

Figure 2-8 Mirror/flip example

Table 2-9 Mirror and flip control registers

Function	Address	Default Value	Description
Mirror	16'h3221	8'h00	Bit[2:1]: mirror ctrl
			2'b00 ~ mirror off
			2'b11 ~ mirror on
Flip	16'h3221	8'h00	Bit[6:5]: flip ctrl
			2'b00 ~ flip off
			2'b11 ~ flip on

2.6.2. Output Window

Table 2-10 Output window registers

Function	Address	Default Value	Description
Window width	{16'h3208, 16'h3209}	16'h0780	Output window width
Window height	{16'h320a, 16'h320b}	16'h0438	Output window height
Column start	{16'h3210, 16'h3211}	16'h0004	Output window column start
Row start	{16'h3212, 16'h3213}	16'h0004	Output window row start

2.7. Frame Rate Calculator

The frame rate of this chip is provided by FAEs. For simplicity, the duration of one row can be calculated as 1 ÷ (frame rate × frame length).

Table 2-11 Frame rate related registers

Function	Address	Default Value	Description
Frame length	{16'h320e[6:0],16'h320f}	16'h0465	Frame length={16'h320e[6:0],16'h320f}

2.8. Test Mode

For the ease of testing, this chip provides an incremental test mode as shown in Figure 2-9.

Figure 2-9 Test mode

Table 2-12 Test mode control registers

Function	Address	Register value	Default Value	Description
Grey ramp mode	16'h4501	8'hbc	8'hc4	Bit[3]: incremental pattern enable 0 ~ normal image 1 ~ incremental pattern
	16'h3902	8'h85	8'hc5	Bit[6]: BLC auto enable 0 ~ BLC manual enable 1 ~ BLC auto enable

3. Electrical Characteristics

Table 3-1 Absolute maximum ratings (to pad)

Item	Symbol	Absolute Maximum Ratings	Unit
Analog supply voltage	V_{AVDD}	-0.3~3.4	V
I/O supply voltage	V_{DOVDD}	-0.3~2.2	V
Digital supply voltage	V_{DVDD}	-0.3~1.65	V
I/O input voltage	V_I	-0.3 ~ V_{DOVDD} +0.3	V
I/O output voltage	V_O	-0.3 ~ V_{DOVDD} +0.3	V
Operating temperature	T_{OPR}	-30~+85	°C
Functional temperature	T_{SPEC}	-20~+60	°C
Storage temperature	T_{STG}	-40~+85	°C

Table 3-2 DC electrical characteristics (to pad)

Item	Symbol	Min	Typical	Max	Units
Power Supply					
Analog supply voltage	V_{AVDD}	2.7	2.8	2.9	V
I/O supply voltage	V_{DOVDD}	1.7	1.8	1.9	V
Digital supply voltage	V_{DVDD}	1.4	1.5	1.6	V
Supply Current (Operating current *1, linear mode, 60fps, MIPI 2-lane output)					
Analog supply current	I_{AVDD}	-	17.0	20.048	mA
I/O supply current	I_{DOVDD}	-	0.03	0.035	mA
Digital supply current	I_{DVDD}	-	100.6	118.639	mA
Total consumption	Power (*)	-	198.6	234.158	mW
Digital Input					
Input low level	V_{IL}	-	-	0.3 × DOVDD	V
Input high level	V_{IH}	0.7 × DOVDD	-	-	V
Input capacitor	C_{IN}	-	-	10	pF
Digital Output (25 pF standard load)					
Output high level	V_{OH}	0.9 × DOVDD	-	-	V
Output low level	V_{OL}	-	-	0.1 × DOVDD	V
Serial Interface Input (SCL and SDA)					
Input low level	V_{IL}	- 0.5	0	0.3 × DOVDD	V
Input high level	V_{IH}	0.7 × DOVDD	DOVDD	DOVDD + 0.5	V

Note: *1 Operating current: (Typ.) Supply voltage 2.8V/1.8V/1.5V, T_j=25°C; max. analogue gain; test condition: 100 LSB

Table 3-3 AC characteristics (TA = 25°C, AVDD = 2.8V, DOVDD = 1.8V)

Item	Symbol	Min	Typical	Max	Unit
AC Parameters					
DC differential linearity deviation	DLE	-	< 1	-	LSB
DC integral linearity deviation	ILE	-	< 2	-	LSB
Crystal and Clock Input					
Input clock frequency	f_{EXTCLK}	6	-	40	MHz
Input clock high pulse width	t_{WH}	5	-	-	ns
Input clock low pulse width	t_{WL}	5	-	-	ns
Input clock duty cycle	-	45	50	55	%

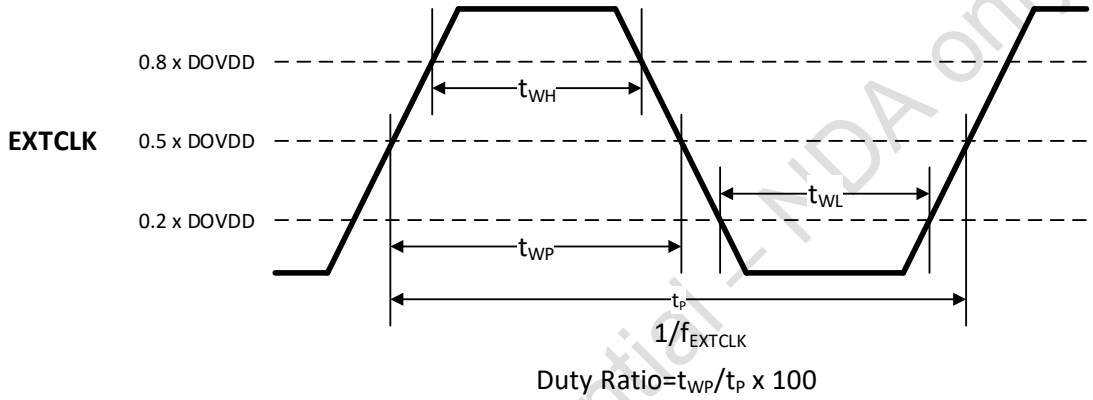

Figure 3-1 Input clock waveform

4. Optical Characteristic

4.1. QE Curve

SC230AI QE curve is shown below.

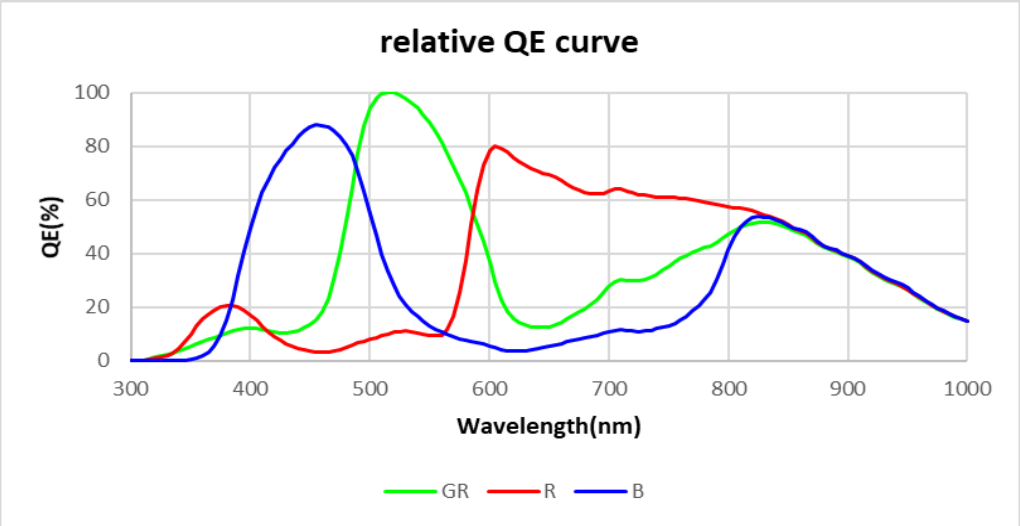

Figure 4-1 QE curve

4.2. Chief Ray Angle (CRA)

SC230AI CRA curve is shown below.

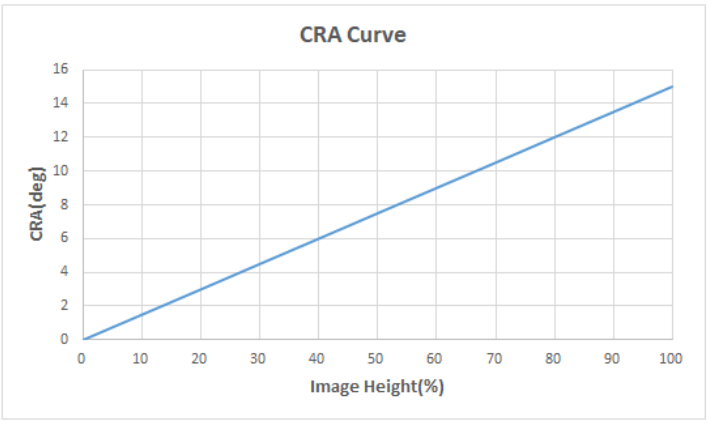

	Image Height		CRA
	%	mm	deg.
	0	0.000	0
	10	0.321	1.5
	20	0.642	3
	30	0.962	4.5
	40	1.283	6
	50	1.604	7.5
	60	1.925	9
	70	2.245	10.5
	80	2.566	12
	90	2.887	13.5
	100	3.208	15

Figure 4-2 CRA curve

5. Packaging Information

SC230AI provides a 41-pin CSP package. The package drawing is shown in Figure 5-1.

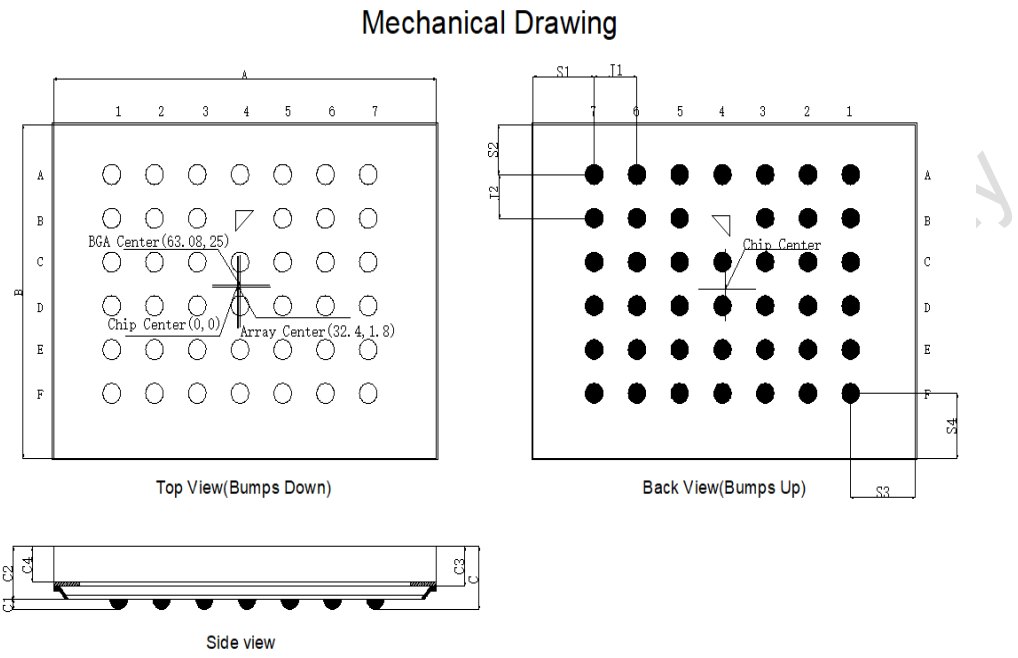

Figure 5-1 Package drawing

Note:

1) Chip Center is not coincident with Array Center (Optical Center), BGA Center is not coincident with Optical Center. Taking BGA Center as the origin, the Optical Center is (-30.68, -23.2), Chip Center is (-63.08, -25), the unit is μm.

2) Distance from the image plane to package bottom: C-C3

Table 5-1 Package dimensions

Parameter	Symbol	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
Package Body Dimension X	A	6.271	6.246	6.296	0.247	0.246	0.248
Package Body Dimension Y	B	4.107	4.082	4.132	0.162	0.161	0.163
Package Height	C	0.680	0.625	0.735	0.027	0.025	0.029
Thickness from top glass surface to wafer	C3	0.345	0.325	0.365	0.014	0.013	0.014
Glass Thickness	C4	0.300	0.290	0.310	0.012	0.011	0.012
Package Body Thickness	C2	0.53	0.495	0.565	0.021	0.019	0.022
Ball Height	C1	0.150	0.120	0.180	0.006	0.005	0.007
Ball Diameter	D	0.300	0.270	0.330	0.012	0.011	0.013
Total Ball Count	N	41	-	-	-	-	-
Ball Count X axis	N1	7	-	-	-	-	-
Ball Count Y axis	N2	6	-	-	-	-	-
Pins Pitch X axis1	J1	0.730	0.720	0.740	0.029	0.028	0.029
Pins Pitch Y axis1	J2	0.650	0.640	0.660	0.026	0.025	0.026

Parameter	Symbol	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
Edge to Ball Center Distance along X	S1	0.882	0.852	0.912	0.035	0.034	0.036
Edge to Ball Center Distance along Y	S2	0.404	0.374	0.434	0.016	0.015	0.017
Edge to Ball Center Distance along X	S3	1.008	0.978	1.038	0.040	0.039	0.041
Edge to Ball Center Distance along Y	S4	0.454	0.424	0.484	0.018	0.017	0.019

6. Order Information

Table 6-1 Order information

Product code	Package	Description
SC230AI-CSBNN00	41-pin CSP	2.0 Megapixel, RAW/RGB, DVP/MIPI output
SC230AI-CSBNF00	41-pin CSP	2.0 Megapixel, RAW/RGB, DVP/MIPI output

7. Revision History

Version	Description	Date
0.3	Initial version	2021-5-6
0.4	Section 2.3.3: Table 2-5: updated ANA gain	2021-7-13
0.5	To unify calculation method, updated sensitivity value	2021-7-21
0.6	■ Section Staggered HDR: Table 2-2: updated the default value of "In HDR no virtual channel mode select" ■ Section AEC control registers: Table 2-3: updated max. and min. exposure values ■ Chapter Order Information: added protective foil part number	2021-12-22
1.0 (Design Release)	Added typical values of operating current and total consumption	2022-01-21
1.1	Table 3-2: updated the typical values of current and total power, and added the max values.	2022-02-25
1.2	Updated the max value of analog gain to 99x Updated the Table 2-5 Analog gain control registers	2022-05-20
1.3	Updated the Figure 1-6 I^2C standard protocol	2022-05-31
1.4	Added Section **1.4.2 Power-down Timing**	2022-06-23
1.5	Table 2-4: corrected the table header	2022-10-24
1.6	Figure 5-1 Package drawing: Added the distance calculation from image plane to package bottom.	2023-09-05
1.7	Table 2-6 Digital gain control registers: updated table layout	2023-11-15

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