datasheet

PRODUCT SPECIFICATION

1/3" color CMOS 4 megapixel (2688x1520) image sensor
with PureCel®Plus and Nyxel® technologies

OS04C10

color CMOS 4 megapixel (2688 x1520) image sensor with PureCel®Plus and Nyxel® technologies

datasheet (CSP)
PRODUCT SPECIFICATION

version 2.01
february 2021

To learn more about OmniVision Technologies, visit www.ovt.com.

applications

- security camera
- action camera
- high resolution consumer camera

ordering information

- **OS04C10-A43A** (color, lead-free)
  43-pin CSP

features

- programmable controls for frame rate, mirror and flip, cropping, and windowing
- supports output formats: 12-bit/10-bit RAW RGB
- supports images sizes: full (2688x1520), 1080p (1920x1080), 720p (1280x720), AO_360p (640x360), and AO_720p (1280x720)
- supports 2x2 binning
- standard serial SCCB interface
- up to 4-lane MIPI serial output interface (supports maximum speed up to 1500 Mbps/lane)
- add staggered HDR RAW data output
- programmable I/O drive capability
- built-in temperature sensor
- MIPI serial output interface (1-lane, 2-lane, or 4-lane)
- image quality controls: defect pixel correction, automatic black level calibration

key specifications (typical)

- **active array size:** 2688 x 1520
- **power supply:**
  core: 1.2V
  analog: 2.8V
  I/O: 1.8V
- **power requirements:**
  active: 155 mW
  XSHUTDOWN: < 10 µA
- **temperature range:**
  operating: -30°C to +85°C junction temperature (see **table 7-2**)
  stable image: -10°C to +60°C junction temperature (see **table 7-2**)
- **output formats:** 10/12-bit RGB RAW
- **lens size:** 1/3"
- **lens chief ray angle:** 12° non-linear (see **figure 9-3**)
- **input clock frequency:** 6~27 MHz
- **maximum image transfer rate:**
  2688x1520: 60 fps (see **table 2-1**)
  1920x1080: 80 fps (see **table 2-1**)
  1280x720: 240 fps
- **sensitivity:** 14,700 e⁻/Lux.sec
- **scan mode:** progressive
- **max S/N ratio:** 37.9 dB
- **dynamic range:** 82.6 dB @ 15.5x gain
- **maximum exposure interval:** VTS-8
- **pixel size:** 1.998 µm x 1.998 µm
- **image area:** 5402.592 µm x 3068.928 µm
- **package dimensions:** 6523.5 µm x 4026 µm

note Power requirements specifications are estimated values and are subject to change when measured data using real silicon is available.

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OS04C10 image sensor. The package information is shown in **section 8**.

figure 1-1 pin diagram

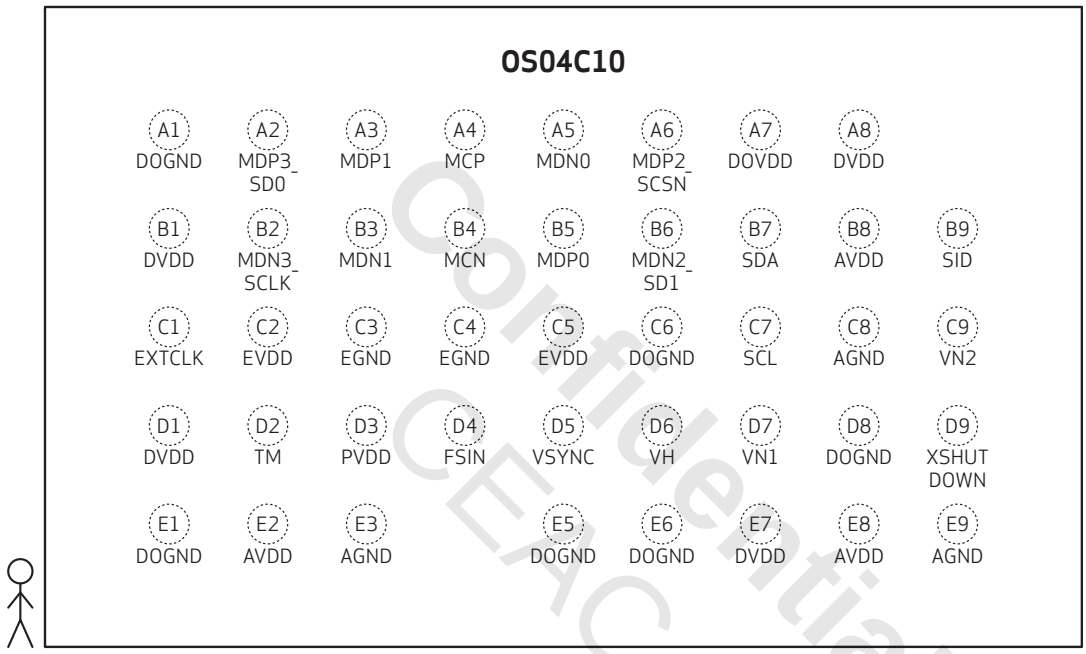


table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description
A1	DOGND	ground	I/O ground
A2	**MDP3_SD0**	output	MIPI data positive output, AO-link D0
A3	**MDP1**	output	MIPI data positive output
A4	**MCP**	output	MIPI clock positive output
A5	**MDN0**	output	MIPI data negative output
A6	**MDP2_SCSN**	output	MIPI data positive output, AO-link CS
A7	DOVDD	power	I/O power
A8	DVDD	power	digital circuit power
B1	DVDD	power	digital circuit power

table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description
B2	**MDN3_SCLK**	output	MIPI data negative output, AO-link CLK
B3	**MDN1**	output	MIPI data negative output
B4	**MCN**	output	MIPI clock negative output
B5	**MDP0**	output	MIPI data positive output
B6	**MDN2_SD1**	output	MIPI data negative output, AO-link D1
B7	**SDA**	I/O	SCCB interface data pin
B8	AVDD	power	analog power
B9	**SID**	input	SCCB last bit ID input 0: SCCB ID address = 0x6C 1: SCCB ID address = 0x20
C1	**EXTCLK**	Input	system clock input
C2	EVDD	power	power for MIPI TX circuit
C3	EGND	ground	ground for MIPI TX circuit
C4	EGND	ground	ground for MIPI TX circuit
C5	EVDD	power	power for MIPI TX circuit
C6	DOGND	ground	I/O ground
C7	**SCL**	input	SCCB interface input clock
C8	AGND	ground	analog ground
C9	VN2	input	reference
D1	DVDD	power	digital circuit power
D2	**TM**	input	test mode (active high with pull down resistor)
D3	PVDD	power	PLL analog power
D4	**FSIN**	I/O	video output frame start signal
D5	**VSYNC**	I/O	frame sync
D6	VH	input	reference
D7	VN1	input	reference
D8	DOGND	ground	I/O ground
D9	**XSHUTDOWN**	input	reset and power down (active low with pull down resistor)
E1	DOGND	ground	I/O ground
E2	AVDD	power	analog power
E3	AGND	ground	analog ground

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description
E5	DOGND	ground	I/O ground
E6	DOGND	ground	I/O ground
E7	DVDD	power	digital circuit power
E8	AVDD	power	analog power
E9	AGND	ground	analog ground

table 1-2 pin states under various conditions

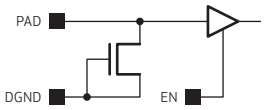
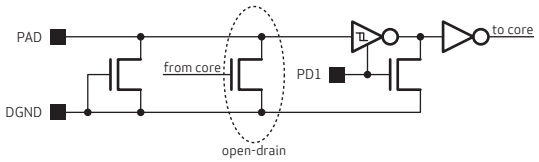
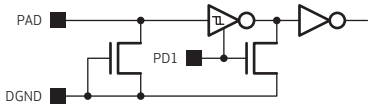
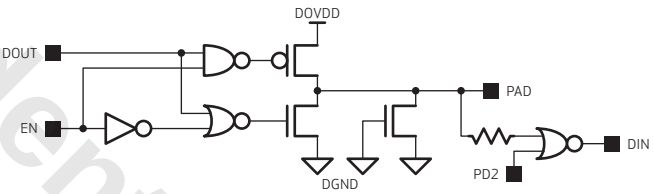
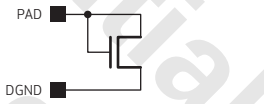
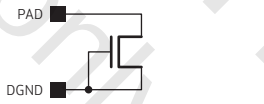
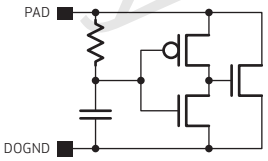
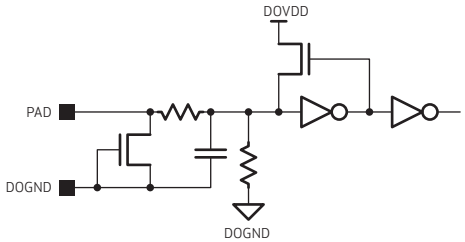
pin number	signal name	RESET[a]	after XSHUTDOWN[b]	software standby[c]
A2	MDP3_SD0	high-z	high	high
A3	MDP1	high-z	high	high
A4	MCP	high-z	high	high
A5	MDN0	high-z	high	high
A6	MDP2_SCSN	high-z	high	high
B2	MDN3_SCLK	high-z	high	high
B3	MDN1	high-z	high	high
B4	MCN	high-z	high	high
B5	MDP0	high-z	high	high
B6	MDN2_SD1	high-z	high	high
B7	SDA	high	high	high
B9	SID	input	input	input
C1	EXTCLK	input	input	input
C7	SCL	high	high	high
D2	TM	input	input	input
D4	FSIN	input	input	input
D5	VSYNC	input	input	input
D9	XSHUTDOWN	input	input	input

a. XSHUTDOWN; chip is in XSHUTDOWN without sending setting

b. XSHUTDOWN from 0t; chip is released from XSHUTDOWN without sending setting

c. sensor set to sleep from streaming; chip is not in XSHUTDOWN and then setting is sent; after, set sensor to sleep mode

table 1-3 pad symbol and equivalent circuit

symbol	equivalent circuit
EXTCLK	
SDA	
SCL	
FSIN, VSYNC	
VN	
MDN3_SCLK, MDP3_SD0, MDN2_SD1, MDP2_SCSN MDP1, MDP0, MDN1, MDN0, MCP, MCN, EGND, AGND, DOGND, VH	
AVDD, DVDD, DOVDD, PVDD	
XSHUTDOWN, SID, TM, XSHUTDOWN2	

2 system level description

2.1 overview

The OS04C10 RAW RGB PureCel®Plus image sensor is a high performance, 1/3-inch, 4 megapixel CMOS image sensor that delivers 2688x1520 at 60 fps. It provides full-frame, sub-sampled, and windowed 10-bit MIPI images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OS04C10 has a 4 megapixel image array capable of operating at up to 60 frames per second (fps) in 10-bit resolution with complete user control over image quality, formatting, and output data transfer. Some image processing functions, such as defective pixel canceling, etc., are programmable through the SCCB interface.

In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

The OS04C10 has a MIPI interface of up to four lanes.

2.2 architecture

The OS04C10 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OS04C10 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, pre-charging and sampling the rows of the array sequentially. In the time between pre-charging and sampling a row, the charge in the pixels decreases with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between pre-charging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs up to 10-bit data for each pixel in the array.

figure 2-1 OS04C10 block diagram

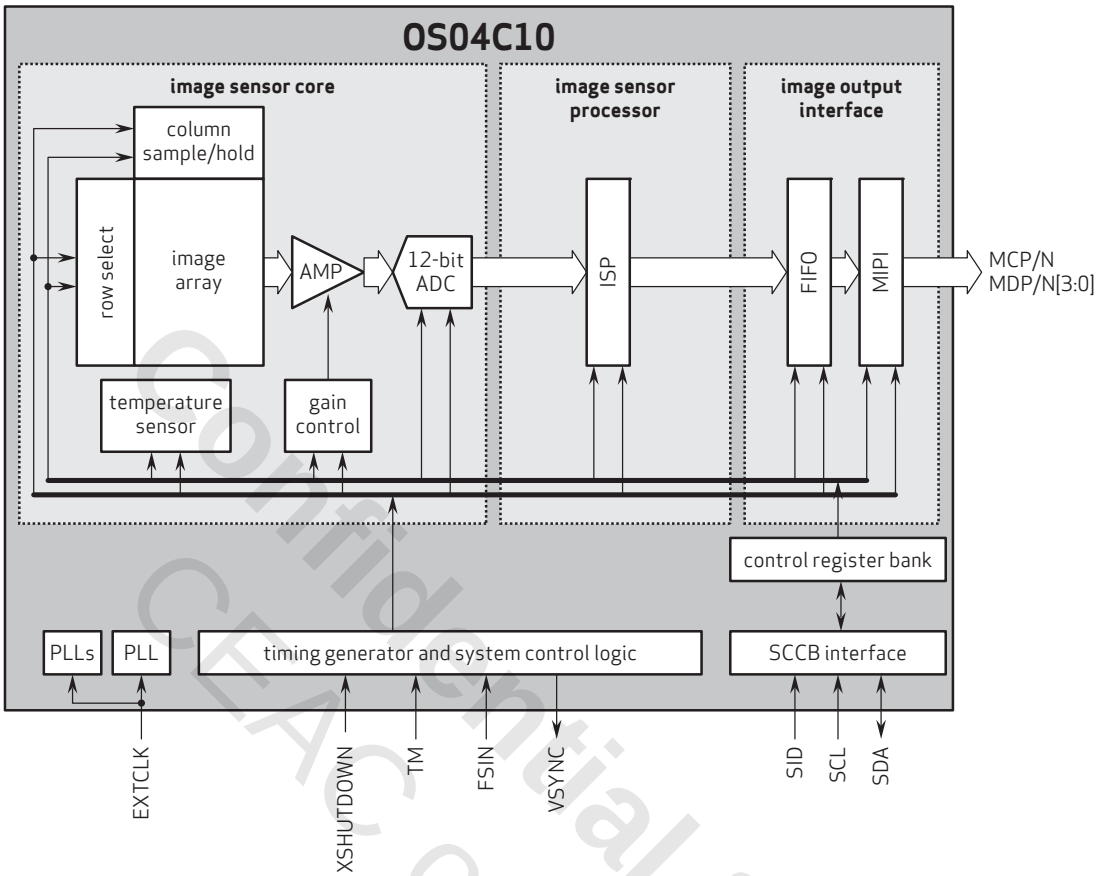
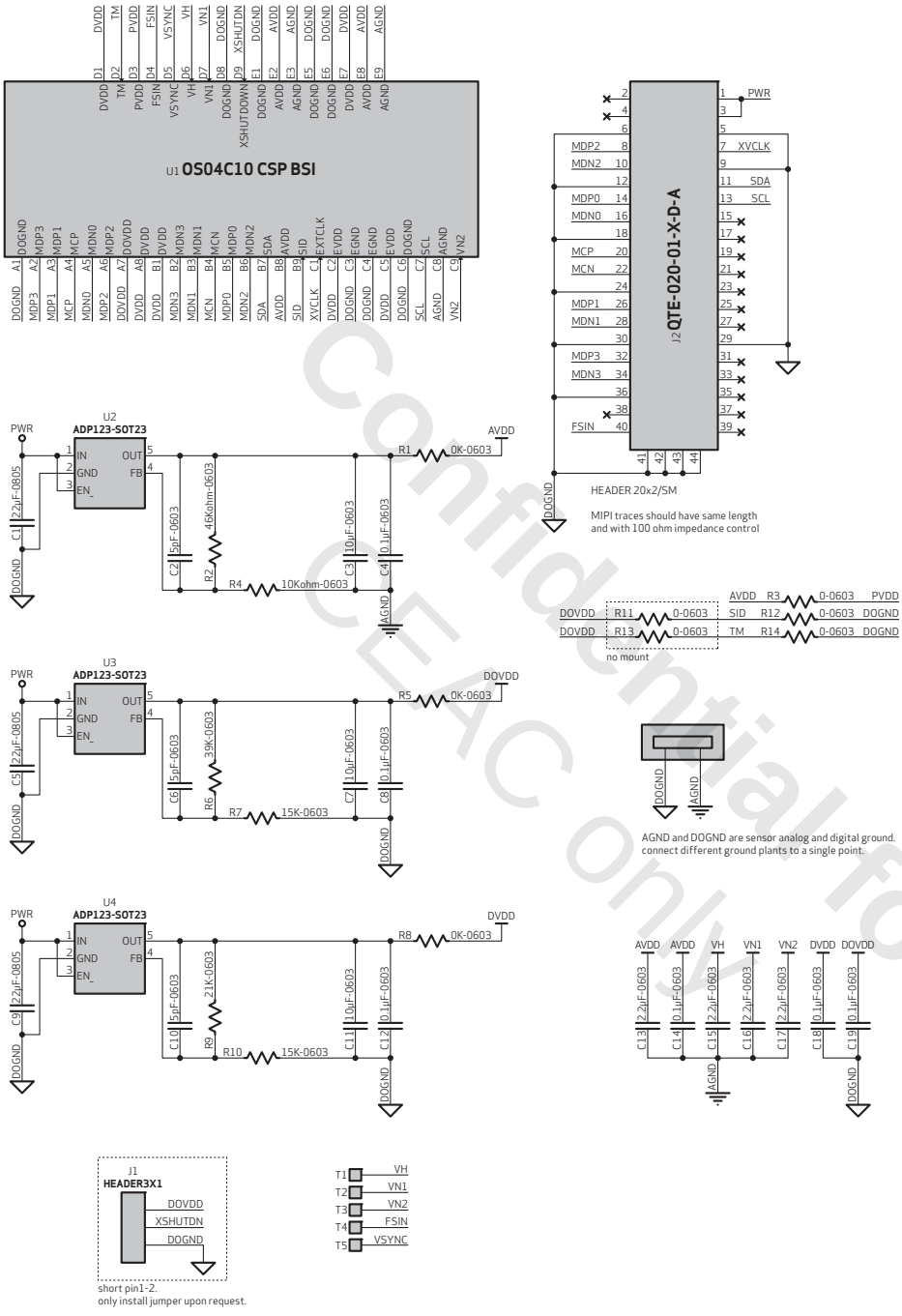


figure 2-2 OS04C10 reference schematic



2.3 format and frame

The OS04C10 supports RAW RGB output with two/four lane MIPI interface.

table 2-1 format and frame rate for two/four lane MIPI

format	resolution	max frame rate	methodology	10-bit output MIPI data rate
full (4 MP)	2688 x 1520	60 fps	linear mode: 60 fps @ 10-bit 30 fps @ 12-bit staggered HDR mode: 30x2 fps @ 10-bit	750 Mbps (4-lane) 1500 Mbps (2-lane)
1080p	1920 x 1080	80 fps	crop from full size staggered HDR mode: 40x2 fps @ 10-bit	750 Mbps (4-lane) 1500 Mbps (2-lane)
720p	1280 x 720	240 fps	2x2 binning and cropping staggered HDR mode: 120x2 fps @ 10-bit	750 Mbps (4-lane) 1500 Mbps (2-lane)

table 2-2 format and frame rate for always-on mode

format	resolution	max frame rate	methodology	10-bit output (AO) data rate
360p	640 x 360	1~10 fps	bin4	20 Mbps (line switching)~140 Mbps (burst)
720p	1280 x 720	<5 fps	bin2	<140 Mbps

2.4 I/O control

The OS04C10 can configure its I/O pins as an input or output. For the output signal, it follows one of two paths: either from the data path or from register control.

table 2-3 I/O control registers

function	register	description
output drive capability control	0x3663	Bit[6:5]: I/O pad drive capability 00: 1x 01: 2x 10: 3x 11: 4x
FSIN I/O control	0x3002	Bit[0]: FSIN output enable 0: Input 1: Output
VSYNC I/O control	0x3002	Bit[1]: VSYNC output enable 0: Input 1: Output
FSIN output select	0x3010	Bit[1]: Enable FSIN as GPIO controlled by register
VSYNC output select	0x3010	Bit[4]: Enable VSYNC as GPIO controlled by register
FSIN output value	0x3008	Bit[1]: Register control FSIN output
VSYNC output value	0x3008	Bit[4]: Register control VSYNC output

2.5 MIPI interface

The OS04C10 supports an MIPI interface of up to four lanes. The MIPI interface can be configured for 1/2/4-lane and each lane is capable of a data transfer rate of up to 1.5 Gbps.

2.6 power management

Based on the system power configuration (XSHUTDOWN), the power up sequence will differ. OmniVision recommends cutting off all power supplies, including the external DVDD, when the sensor is not in use.

2.6.1 power up sequence

To avoid any glitch from a strong external noise source, OmniVision recommends controlling XSHUTDOWN by GPIO. Whether or not XSHUTDOWN is controlled by GPIO, XSHUTDOWN rising cannot occur before AVDD, DVDD, and DOVDD.

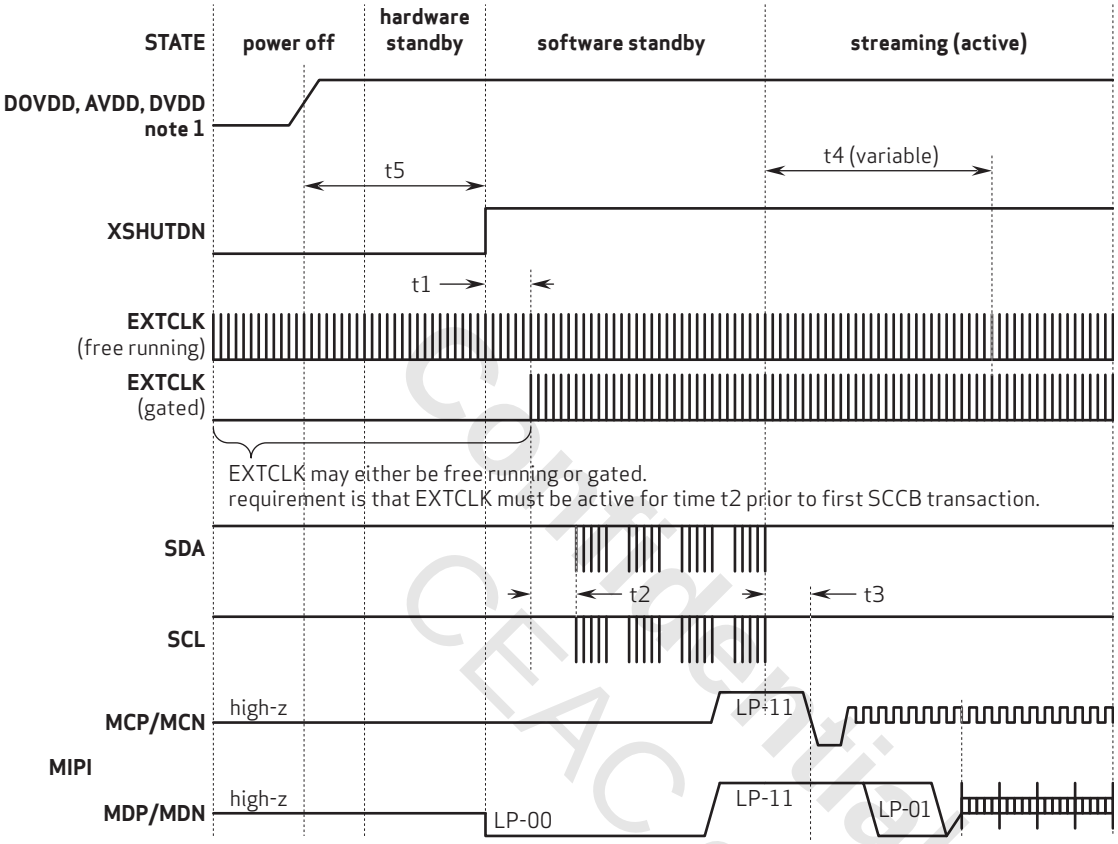
table 2-4 power up sequence

XSHUTDOWN	power up sequence requirement
GPIO	Refer to **figure 2-3** 1. DOVDD, AVDD, and DVDD can rise in any order 2. XSHUTDOWN rising must occur after AVDD, DOVDD, and DVDD are stable

table 2-5 power up sequence timing constraints

constraint	label	min	max	unit
XSHUTDOWN rising – system ready	t1	5		ms
minimum number of EXTCLK cycles prior to first SCCB transaction	t2	8192		EXTCLK cycles
MIPI clock startup time	t3		8192	EXTCLK cycles
entering streaming mode – first frame start sequence (variable)	t4	delay related to output frame rate and line timing		lines
AVDD, DOVDD or DVDD, whichever is last – XSHUTDOWN rising	t5	0	∞	ns

figure 2-3 power up sequence



note 1 DOVDD, AVDD, and DVDD may rise in any order

2.6.2 power down sequence

Pull XSHUTDOWN low to set the sensor into power down mode. The digital and analog supply voltages can be cut off in any order (e.g., DOVDD, DVDD, then AVDD or AVDD, DVDD, then DOVDD). Similar to the power up sequence, the EXTCLK input clock may be either gated or continuous. To avoid bad frames from MIPI, OmniVision recommends setting the sensor into sleep mode in inter frame first before sending the sensor into power down mode by setting register 0x3021[6:5]=2'b00 and register 0x0100 = 0x00.

table 2-6 power down sequence

XSHUTDOWN	power down sequence requirement
GPIO	Refer to **figure 2-5** 1. software standby recommended 2. pull XSHUTDOWN low for minimum power consumption 3. pull AVDD, DVDD, and DOVDD low in any order

table 2-7 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for MIPI end code before entering software for standby; otherwise, enter software standby mode immediately		
minimum of EXTCLK cycles after last SCCB transaction or MIPI frame end	t1	512		EXTCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDOWN falling	t2	512		EXTCLK cycles
XSHUTDOWN falling – AVDD, DVDD or DOVDD falling, whichever is first	t3	0.0		ns

figure 2-4 software standby sequence

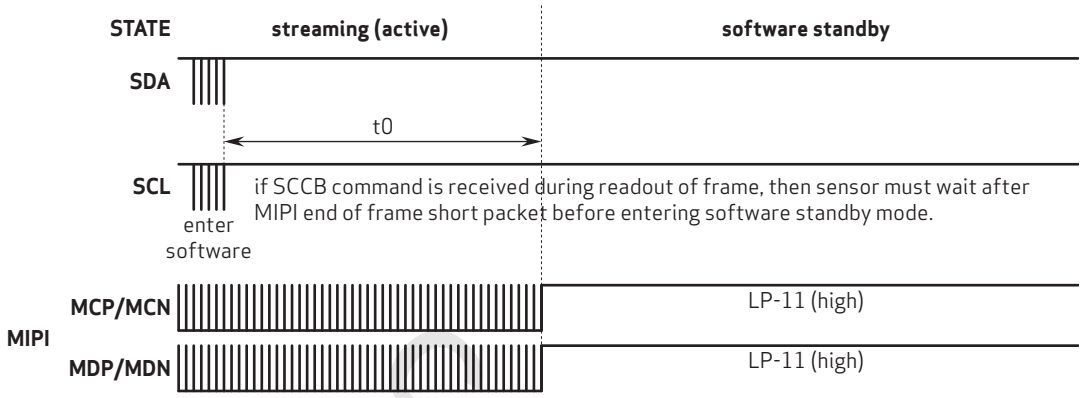
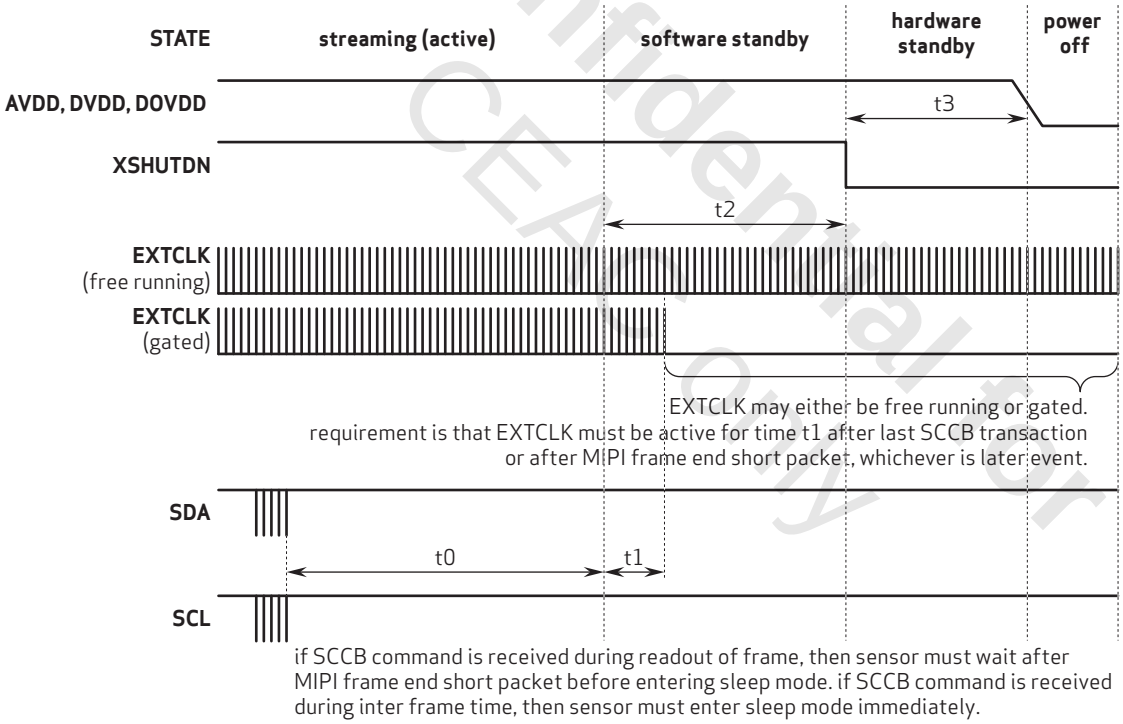


figure 2-5 power down sequence



2.7 reset

The whole chip will be reset during power up. Manually applying a hardware reset (XSHUTDOWN = 0) upon power up is recommended even though the on-chip power up reset is included. The hardware reset is active low with an asynchronized design. The reset pulse width should be greater than or equal to 2 ms.

2.7.1 power ON reset

The power on reset can be controlled from an external pin. Additionally, in this sensor, a power on reset is generated after the core power becomes stable.

2.7.2 software reset

When register 0x0103[0] is configured as 1, all registers are reset to default value.

2.8 standby mode

Two suspend modes are available for the OS04C10:

- hardware standby
- software standby

2.8.1 hardware standby

If XSHUTDOWN is tied to low, it will initiate hardware standby mode. In this mode, the total power consumption will be less than 100 µW.

2.8.2 software standby

Executing a software power down (0x0100[0]) through the SCCB interface suspends internal circuit activity, but does not halt the device clock. All register content is maintained in standby mode. During the resume state, all the registers are restored to their original values.

table 2-8 hardware and standby description

mode	description
hardware standby with XSHUTDOWN	1. enabled by pulling XSHUTDOWN low 2. power down all blocks 3. register values are reset to default values 4. no SCCB communication 5. minimum power consumption
software standby	1. default mode after power on reset 2. power down all blocks except SCCB 3. register values are maintained 4. SCCB communication is available 5. low power consumption 6. GPIO can be configured as high/low/tri-state

2.9 system clock control

PLL settings can only be changed during sensor standby mode (0x0100 = 0).

2.9.1 PLL1

The PLL1 generates a default 180 MHz pixel clock and 1440 MHz MIPI serial clock from a 6~27 MHz input clock. The VCO range is from 500 MHz to 1500 MHz. A programmable clock is provided to generate different frequencies.

2.9.2 PLL2

The PLL2 generates a default 144 MHz system clock from a 6~27 MHz input clock. The VCO range is from 500 MHz to 1500 MHz. A programmable clock divider is provided to generate different frequencies.

figure 2-6 clock scheme

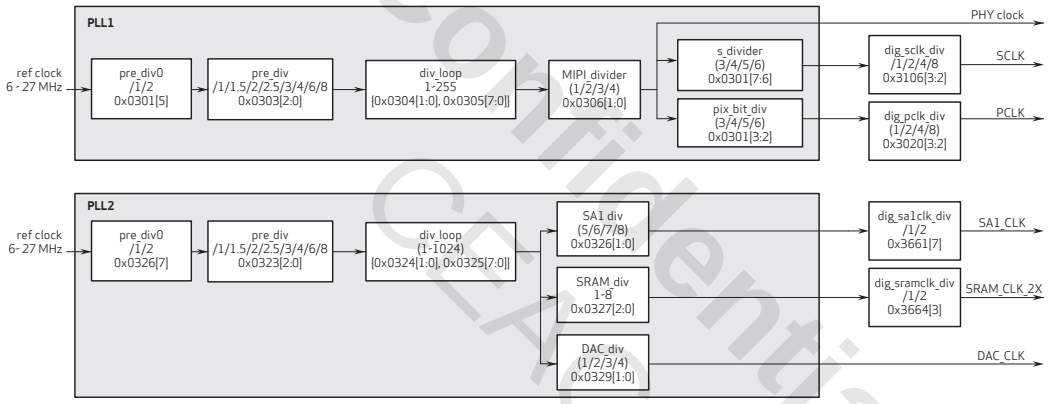


table 2-9 PLL control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x0300	PLL_CTRL_00	0x00	RW	Bit[2]: pll1_rst_0 Bit[0]: r_pll1_bypass_o
0x0301	PLL_CTRL_01	0x84	RW	Bit[7:6]: r_pll1_divsys_o Bit[5]: r_pll1_predivp_o Bit[3:2]: r_pll1_divs_o
0x0302	PLL_CTRL_02	0x01	RW	Bit[5]: r_pll1_div_rst_sync_en_o Bit[2:0]: r_pll1_cp_o
0x0303	PLL_CTRL_03	0x01	RW	Bit[2:0]: r_pll1_prediv_o
0x0304	PLL_CTRL_04	0x00	RW	Bit[1:0]: r_pll1_divp_o[9:8]
0x0305	PLL_CTRL_05	0x5A	RW	Bit[7:0]: r_pll1_divp_o[7:0]
0x0306	PLL_CTRL_06	0x00	RW	Bit[1:0]: r_pll1_divpix_o

table 2-9 PLL control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x0307	PLL_CTRL_07	0x10	RW	Bit[4]: r_pll1_lock_det_en_o Bit[3:2]: r_pll1_precision_o Bit[1:0]: r_pll1_cnt_ref_o
0x0320	PLL_CTRL_20	0x10	RW	Bit[4]: r_pll2_vcoby2_o Bit[3]: r_pll2_band_sel_o Bit[2]: pll2_rst_o Bit[1]: r_pll2_div_rst_sync_en_o Bit[0]: r_pll2_bypass_o
0x0321	PLL_CTRL_21	0x01	RW	Bit[2:0]: r_pll2_cp_o
0x0323	PLL_CTRL_23	0x04	RW	Bit[2:0]: r_pll2_prediv_o
0x0324	PLL_CTRL_24	0x02	RW	Bit[1:0]: r_pll2_divp_o[9:8]
0x0325	PLL_CTRL_25	0xBC	RW	Bit[7:0]: r_pll2_divp_o[7:0]
0x0326	PLL_CTRL_26	0x82	RW	Bit[7]: r_pll2_predivp_o Bit[1:0]: r_pll2_divsa1_o
0x0327	PLL_CTRL_27	0x04	RW	Bit[2:0]: r_pll2_divsram_o
0x0329	PLL_CTRL_29	0x01	RW	Bit[1:0]: r_pll2_divdac_o

2.10 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

In the OS04C10, the SCCB ID is controlled by the SID pin and can be programmed. If SID is low, the sensor's SCCB address comes from register 0x3003 which has a default value of 0x6C for write (0x6D for read). If SID is high, the sensor's SCCB address comes from register 0x3004 which has a default value of 0x20 for write (0x21 for read). There is an alternative ID in register 0x3005, which has a default value of 0x42 The alternative ID works on both SID high or low.

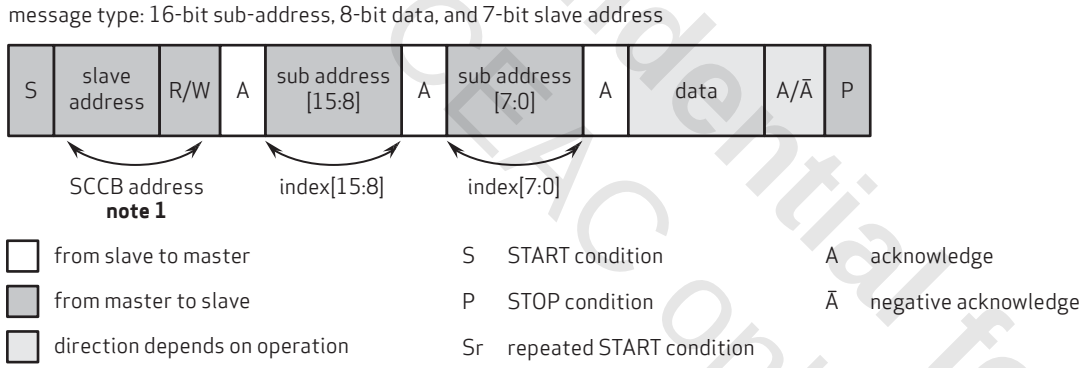
2.10.1 data transfer protocol

The data transfer of the OS04C10 follows the SCCB protocol.

2.10.2 message format

The OS04C10 supports the message format shown in **figure 2-7**. The repeated START (Sr) condition is not shown in **figure 2-8**, but is shown in **figure 2-9** and **figure 2-10**.

figure 2-7 message type



note 1 slave address must be 0x36 for SCCB write address to be 0x6C and for SCCB read address to be 0x6D

2.10.3 read / write operation

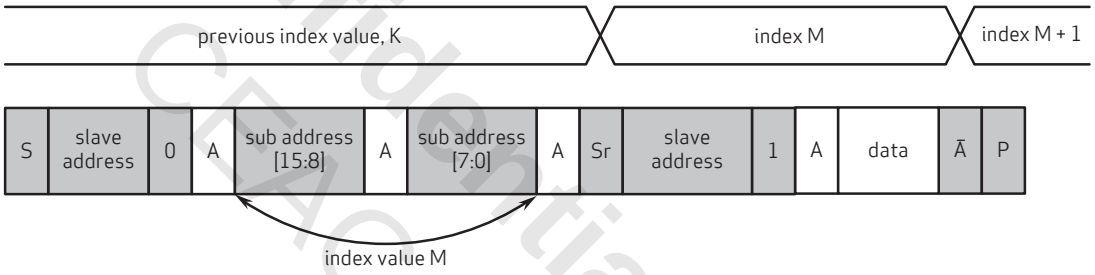
The OS04C10 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

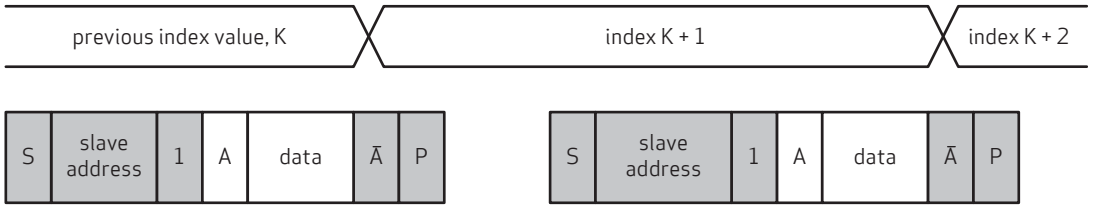
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 2-8**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-8 SCCB single read from random location



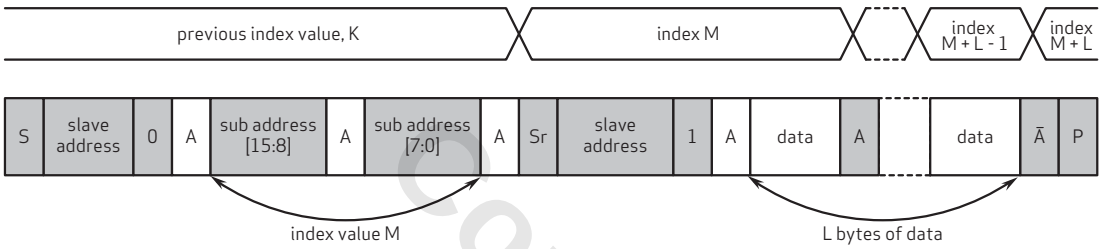
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 2-9**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-9 SCCB single read from current location



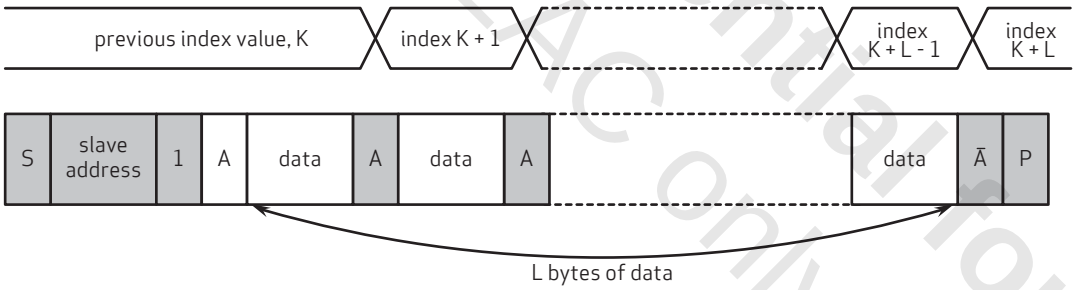
The sequential read from a random location is illustrated in **figure 2-10**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 2-10 SCCB sequential read from random location



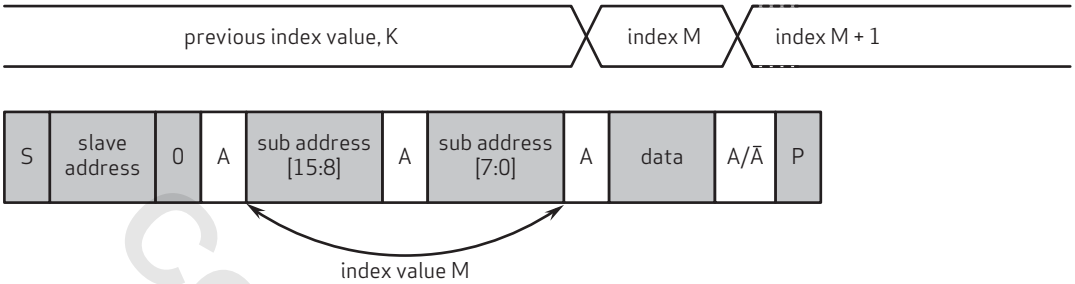
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation as shown in **figure 2-11**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-11 SCCB sequential read from current location



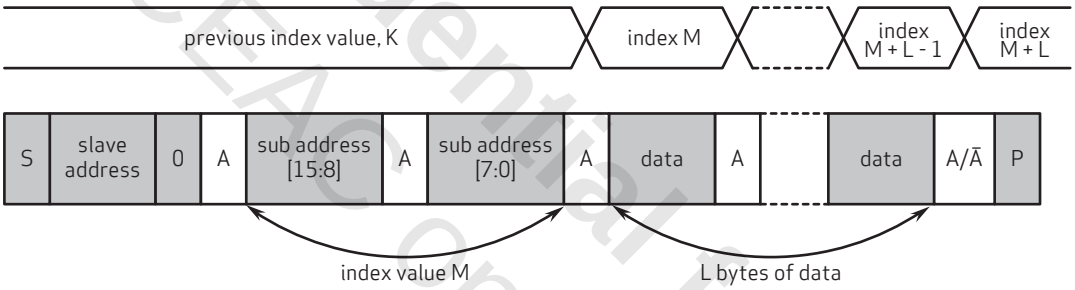
The write operation to a random location is illustrated in **figure 2-12**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 2-12 SCCB single write to random location



The sequential write is illustrated in **figure 2-13**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 2-13 SCCB sequential write to random location



2.10.4 SCCB timing

figure 2-14 SCCB interface timing

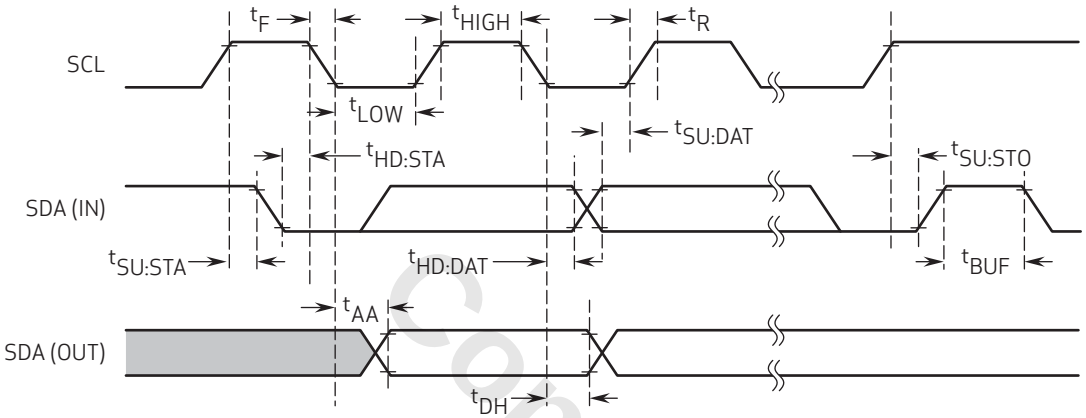


table 2-10 SCCB interface timing specifications[a]

symbol	parameter	400kHz mode		1000kHz mode[b]		unit
		min	max	min	max	
f_{SCL}	clock frequency		400		1000	kHz
t_{LOW}	clock low period	1.3		0.5		µs
t_{HIGH}	clock high period	0.6		0.26		µs
t_{AA}	SCL low to data out valid	0.1	0.9	0.05	0.45	µs
t_{BUF}	bus free time before new start	1.3		0.5		µs
$t_{HD:STA}$	start condition hold time	0.6		0.26		µs
$t_{SU:STA}$	start condition setup time	0.6		0.26		µs
$t_{HD:DAT}$	data in hold time	0		0		µs
$t_{SU:DAT}$	data in setup time	0.1		0.05		µs
$t_{SU:STO}$	stop condition setup time	0.6		0.26		µs
t_R, t_F	SCCB rise/fall times		0.3		0.12	µs
t_{DH}	data out hold time	0.05		0		µs

a. timing measurement shown at beginning of rising edge and/or end of falling edge signifies 30%,
timing measurement shown in middle of rising/falling edge signifies 50%,
timing measurement shown at end of rising edge and/or beginning of falling edge signifies 70%

b. when input clock > 10 MHz

2.11 group write

Group write is supported in order to update a group of registers (except 0x32xx) in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary. If more than one group is going to be launched, the second group cannot be recorded or launched before the first group has effectively been launched.

The OS04C10 supports up to four groups. These groups share 512 bytes of memory and the size of each group is programmable by adjusting the start address.

table 2-11 group hold registers

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch Others: Reserved Bit[3:0]: group ID 0000: Group bank 0 0001: Group bank 1 0010: Group bank 2 0011: Group bank 3 Others: Reserved
0x3209	GRP0_PERIOD	0x00	RW	Number of Frames Staying in Group 0
0x320A	GRP1_PERIOD	0x00	RW	Number of Frames Staying in Group 1
0x320B	GRP2_PERIOD	0x00	RW	Number of Frames Staying in Group 2
0x320C	GRP3_PERIOD	0x00	RW	Number of Frames Staying in Group 3
0x320D	GRP_SWCTRL	0x01	RW	Bit[5]: Repeat switch mode Bit[4]: Context switch enable Bit[1:0]: Switch bank group

2.12 hold

After the groups are configured, users can perform a hold operation to store register settings into the SRAM of each group. The hold of each group starts and ends with the control register 0x3208. The lower 4 bits of register 0x3208 control which group to access, and the upper 4 bits control the start (0x0: hold start) and end (0x1: hold end) of the hold operation.

The example setting below shows the sequence to hold group 0:

```
6C  3208  00    group 0 hold start
6C  3800  11    first register into group 0
6C  3911  22    second register into group 0
6C  3208  10    group 0 hold end
```

2.13 launch

After the contents of each group are defined in the hold operation, all registers belonging to each group are stored in SRAM, and ready to be written into target registers (i.e., the launch of that group).

There are five launch modes as described in sections **section 2.13.1** to **section 2.13.5**.

2.13.1 launch mode 1 - quick manual launch

Manual launch is enabled by setting the register 0x320B to 0.

Quick manual launch is achieved by writing to control register 0x3208. The value written into this register is 0xEX, the upper 4 bits (0xE) are the quick launch command and the lower 4 bits (0xX) are the group number. For example, to launch group 0, write the value 0xE0 to 0x3208, then the contents of group 0 will be written to the target registers immediately after the sensor gets this command through the SCCB. Below is a setting example.

```
6C  320D  00    manual launch on
6C  3208  E0    quick launch group 0
```

2.13.2 launch mode 2 - delay manual launch

Delay manual launch is achieved by writing to the register 0x3208. The value written into this register is 0xAX, where the upper 4 bits (0xA) are the delay launch command and the lower 4 bits (0xX) are the group number. For example, to launch group 1, write the value 0xA1 to 0x3208, then the contents of group 1 will be written to the target registers. The difference with mode 1 is that the writing will wait for some internally defined time spot in vertical blanking, and is thus delayed. Below is a setting example.

```
6C  320D  00    manual launch on
6C  3208  A1    delay launch group 1
```

2.13.3 launch mode 3: quick auto launch

Quick auto launch works like mode 1, the difference is it will return to a specified group automatically. This is controlled by register 0x320D, where Bit[4] is mode enable and Bit[1:0] controls which group to return. 0x3209/320A/320B/320C which is the frame number of group 0/1/2/3, respectively, controls how many frames to stay before returning. The operation can be better understood with an example setting:

```
6C  320D  11    Bit[1:0]: 1, return to group 1, Bit[4}: auto switch enable
6C  3209  04    stay in group 0 for 4 frames
6C  3208  E0    delay launch group 0
```

In this example, the sensor will quick launch group 0, stay at group 0 for 4 frames, then return to group 1.

2.13.4 launch mode 4: delay auto launch

Delay auto launch works like mode 2 during the delay launch operation and like mode 3 during the return operation.

The operation can be better understood with an example setting:

```
6C  320D  11    Bit[1:0]: 1, return to group 1, Bit[4]: auto switch enable
6C  3209  04    stay in group 0 for 4 frames
6C  3208  A0    delay launch group 0
```

In this example, the sensor will delay launch group 0, stay at group 0 for 4 frames, then return to group 1.

2.13.5 launch mode 5: repeat launch

Repeat launch is enabled by register 0x320D[5]. It can support up to 4 groups repeating. 0x3209/320A/320B/320C which is the frame number of group 0/1/2/3, respectively, controls how many frames to stay before jumping to the next one. In this mode, the launch is repeated automatically among group 0, group 1, group 2, and group 3. If any of the group numbers is set to 0, that group is skipped.

The operation can be better understood with an example setting:

```
6C  3209  02    Bit[7:0]: 2, stay 2 frames in group 0
6C  320A  03    Bit[7:0]: 3, stay 3 frames in the group 1
6C  320B  00    Bit[7:0]: 0, do not stay in group 2
6C  320C  08    Bit[7:0]: 8, stay 8 frames in the group 3
6C  320D  30    Bit[5]: repeat switch enable, [4] context switch enable
6C  3208  A0    always use a0 for repeat launch
```

In this example, sensor will delay launch group 0, stay at group 0 for 2 frames, then switch to group 1 for 3 frames, then back to group 3 for 8 frames, then switch back to group 0 for 2 frames, group 1 for 3 frames, group 3 for 8 frames, and so on.

3 block level description

3.1 pixel array structure

The OS04C10 sensor has an image array of 2704 columns by 1536 rows (4,153,344 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 4,153,344 pixels, 4,085,760 (2688x1520) are active pixels and can be output.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

figure 3-1 sensor array region color filter layout

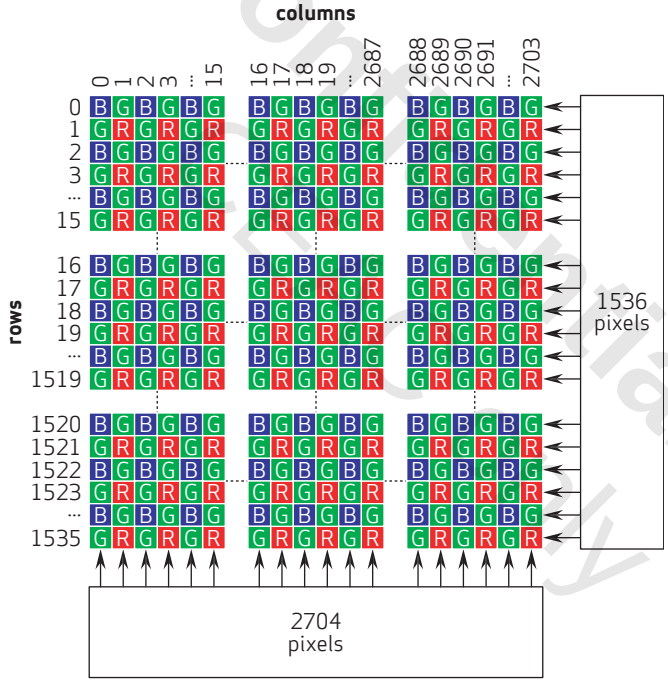


table 3-1 binning-related registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3814	X INC ODD	0x01	RW	Bit[4:0]: x_odd_inc
0x3815	X INC EVEN	0x01	RW	Bit[4:0]: x_even_inc

table 3-1 binning-related registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x382A	Y_INC_ODD	0x01	RW	Bit[4:0]: y_odd_inc
0x382B	Y_INC_EVEN	0x01	RW	Bit[4:0]: y_even_inc
0x3820	FORMAT1	0x80	RW	Bit[5]: Vertical BLC flip Bit[4]: Vertical flip Bit[3]: Horizontal mirror Bit[2]: hbin4_o Bit[1]: hbin2_o Bit[0]: vbinf_o
0x37C2	REGC2	0x04	RW	Bit[3]: vbinf4_rgb
0x4501	R1	0x00	RW	Bit[5:4]: r_hbin4_opt 00: Average of 4 pixels 01: Summary of 4 pixels 10: Select first bin2 pixel 11: Select last bin2 pixel Bit[3:2]: r_hbin2_opt 00: Average 01: Summary 10: Select first pixel 11: Select last pixel

3.2 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

3.3 10-bit A/D converters

The balanced signal is then digitized by the on-chip 10-bit ADC.

4 image sensor core digital functions

4.1 mirror and flip

The OS04C10 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

table 4-1 mirror and flip registers

address	register name	default value	R/W	description
0x3716	REG16	0x04	RW	Bit[5]: Analog flip
0x3820	FORMAT1	0x80	RW	Bit[5]: Vertical BLC flip Bit[4]: Vertical flip Bit[3]: Horizontal mirror Bit[2]: hbin4_o Bit[1]: hbin2_o Bit[0]: vbinf_o

The following are mirror and flip setting examples:

```
@@ NORMAL (linear or cropped)

6C  3820  80

6C  3716  24


@@ MIRROR (linear or cropped)

6C  3820  88

6C  3716  24
```

```
@@ FLIP (linear or cropped)
6C  3820  B0
6C  3716  04

@@ MIRROR&FLIP (linear or cropped)
6C  3820  B8
6C  3716  04

@@ NORMAL (720p digital binning)
6C  3820  83
6C  3716  24

@@ MIRROR (720p digital binning)
6C  3820  8B
6C  3716  24

@@ FLIP (720p digital binning)
6C  3820  B3
6C  3716  04

@@ MIRROR&FLIP (720p digital binning)
6C  3820  BB
6C  3716  04

@@ NORMAL (720p analog binning)
6C  3820  83
6C  3716  24
```

```
@@ MIRROR (720p analog binning)
6C  3820  8B
6C  3716  24

@@ FLIP (720p analog binning)
6C  3820  B3
6C  3716  24

@@ MIRROR&FLIP (720p analog binning)
6C  3820  BB
6C  3716  24
```

4.2 windowing

An image windowing area is defined by four parameters, horizontal start (HS), horizontal end (HE), vertical start (VS), and vertical end (VE). By properly setting the parameters, any portion within the sensor array size can output as a visible area. Windowing is achieved by masking off the pixels outside of the window; thus, the original timing is not affected.

figure 4-2 image windowing

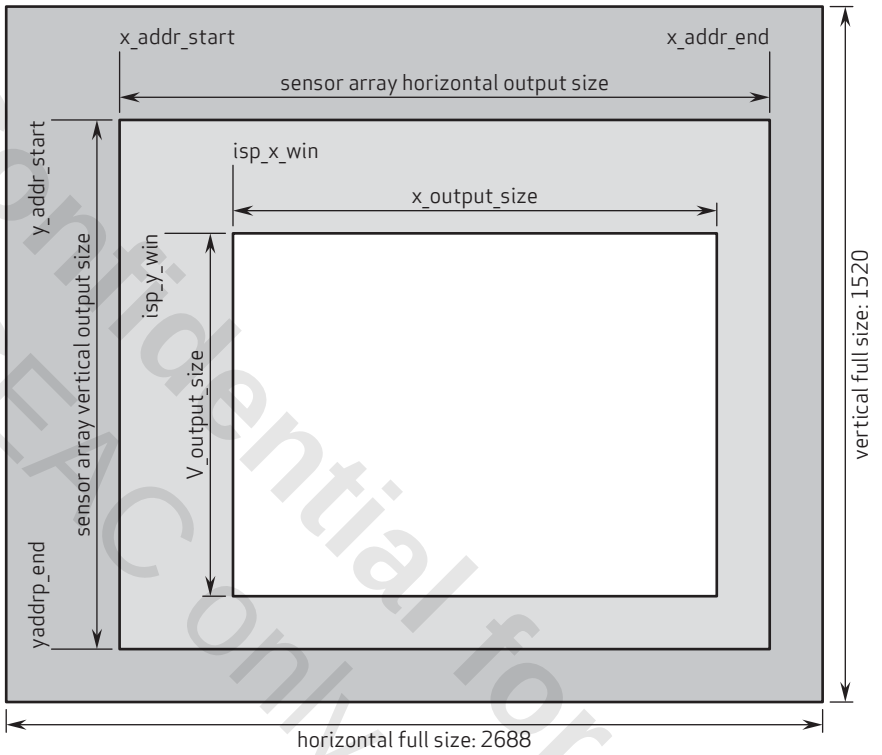


table 4-2 image windowing control functions (sheet 1 of 3)

address	register name	default value	R/W	description
0x3800	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[11:8] Array horizontal start point high byte
0x3801	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[7:0] Array horizontal start point low byte
0x3802	Y ADDR START	0x00	RW	Bit[7:0]: y_addr_start[11:8] Array vertical start point high byte

table 4-2 image windowing control functions (sheet 2 of 3)

address	register name	default value	R/W	description
0x3803	Y ADDR START	0x04	RW	Bit[7:0]: y_addr_start[7:0] Array vertical start point low byte
0x3804	X ADDR END	0x07	RW	Bit[7:0]: x_addr_end[11:8] Array horizontal end point high byte
0x3805	X ADDR END	0x8F	RW	Bit[7:0]: x_addr_end[7:0] Array horizontal end point low byte
0x3806	Y ADDR END	0x04	RW	Bit[7:0]: y_addr_end[11:8] Array vertical end point high byte
0x3807	Y ADDR END	0x43	RW	Bit[7:0]: y_addr_end[7:0] Array vertical end point low byte
0x3808	X OUTPUT SIZE	0x07	RW	Bit[7:0]: x_output_size[11:8] ISP horizontal output width high byte
0x3809	X OUTPUT SIZE	0x80	RW	Bit[7:0]: x_output_size[7:0] ISP horizontal output width low byte
0x380A	Y OUTPUT SIZE	0x04	RW	Bit[7:0]: y_output_size[11:8] ISP vertical output height high byte
0x380B	Y OUTPUT SIZE	0x38	RW	Bit[7:0]: y_output_size[7:0] ISP vertical output height low byte
0x380C	HTS	0x02	RW	Bit[7:0]: HTS[15:8] Total horizontal timing size high byte
0x380D	HTS	0x78	RW	Bit[7:0]: HTS[7:0] Total horizontal timing size low byte
0x380E	VTS	0x04	RW	Bit[7:0]: VTS[15:8] Total vertical timing size high byte
0x380F	VTS	0xA0	RW	Bit[7:0]: VTS[7:0] Total vertical timing size low byte
0x3810	ISP X WIN	0x00	RW	Bit[7:0]: isp_x_win[15:8] ISP horizontal windowing offset high byte
0x3811	ISP X WIN	0x08	RW	Bit[7:0]: isp_x_win[7:0] ISP horizontal windowing offset low byte
0x3812	ISP Y WIN	0x00	RW	Bit[7:0]: isp_y_win[11:8] ISP vertical windowing offset high byte
0x3813	ISP Y WIN	0x04	RW	Bit[7:0]: isp_y_win[7:0] ISP vertical windowing offset low byte
0x3814	X INC ODD	0x01	RW	Bit[4:0]: x_odd_inc
0x3815	X INC EVEN	0x01	RW	Bit[4:0]: x_even_inc
0x3816	Y_INC_ODD	0x01	RW	Bit[4:0]: y_odd_inc

table 4-2 image windowing control functions (sheet 3 of 3)

address	register name	default value	R/W	description
0x3817	Y_INC_EVEN	0x01	RW	Bit[4:0]: y_even_inc

4.3 test pattern

For testing purposes, the OS04C10 offers three types of test patterns: color bar, square, and random data. The OS04C10 also offers two digital effects: transparent effect and rolling bar effect. The output type of digital test pattern is controlled by the test_pattern_type register (0x5080[3:2]). The digital test pattern function is controlled by register 0x5080[7].

4.3.1 color bar

There are four types of color bars which are switched by bar-style in register 0x5040[3:2] (see **figure 4-3**).

figure 4-3 color bar types

4.3.2 square

There are two types of squares: color square and black-white square. The squ_bw register (0x5080[4]) determines which type of square will be output.

figure 4-4 color, black and white square bars

color square

black-white square

4.3.3 random data

There are two types of random data test patterns: frame-changing and frame-fixed random data.

4.3.4 transparent effect

The transparent effect is enabled by transparent_en register (0x5080[5]). If this register is set, the transparent test pattern will be displayed. **figure 4-5** is an example showing a transparent color bar image.

figure 4-5 transparent effect

4.3.5 rolling bar effect

The rolling bar is set by rolling_bar_en register (0x5080[6]). If it is set, an inverted-color rolling bar will roll from up to down. **figure 4-6** is an example showing a rolling bar on a color bar image.

figure 4-6 rolling bar effect

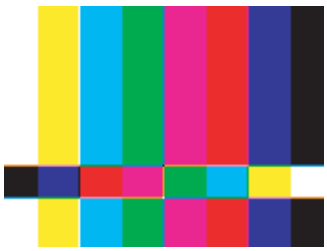


table 4-3 test pattern registers

address	register name	default value	R/W	description
0x5080	ISP_CTRL_0	0x04	RW	Bit[7]: Test enable 0: Disable 1: Enable Bit[6]: Rolling enable (rolling bar in test mode) 0: Disable 1: Enable Bit[5]: Transparent effect enable 0: Disable 1: Enable Bit[4]: Black/white or color square selection 0: Color 1: Black/white Bit[3:2]: Color bar style 0: Disable timing test mode 1: Enable timing test mode Bit[0]: Test mode select
0x5081	ISP_CTRL_1	0x01	RW	Bit[6]: Window cut enable 0: Disable 1: Enable Bit[5]: ISP test Low bits to 0 0: Disable 1: Enable Bit[4]: Random mode frame Fixed seed enable 0: Disable 1: Enable Bit[3:0]: Random seed

4.4 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines and optically shielded (black) pixels on the right side. These lines and columns are used as reference for black level calibration. The main function of the BLC is to adjust all normal pixel values based on the values of the black levels.

table 4-4 BLC registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x4000	BLC_CTRL_00	0xF3	RW	Bit[7]: blk_en Bit[6]: out_range_one_ch_eco Bit[5]: gain_trig_priority Bit[4]: rst_trig_opt Bit[3]: target_adj_dis Bit[2]: cmp_en Bit[1]: dither_en Bit[0]: mf_en
0x4001	BLC_CTRL_01	0x60	RW	Bit[6]: dcblc_en Bit[5]: kcoef_man_en Bit[4]: off_man_en Bit[3]: zero_ln_out_en Bit[2]: blk_ln_out_en Bit[1:0]: byp_mode
0x4002	BLC_CTRL_02	0x00	RW	Bit[1:0]: blk_lvl_target[9:8]
0x4003	BLC_CTRL_03	0x40	RW	Bit[7:0]: blk_lvl_target[7:0]
0x4004	BLC_CTRL_04	0x00	RW	Bit[3:0]: hwin_off[11:8]
0x4005	BLC_CTRL_05	0x08	RW	Bit[7:0]: hwin_off[7:0]
0x4006	BLC_CTRL_06	0x00	RW	Bit[3:0]: hwin_pad[11:8]
0x4007	BLC_CTRL_07	0x08	RW	Bit[7:0]: hwin_pad[7:0]
0x4008	BLC_CTRL_08	0x00	RW	bl_start
0x4009	BLC_CTRL_09	0x0D	RW	bl_end
0x400A	BLC_CTRL_0A	0x02	RW	Bit[7:0]: off_lim_th[15:8]
0x400B	BLC_CTRL_0B	0x00	RW	Bit[7:0]: off_lim_th[7:0]
0x400C	BLC_CTRL_0C	0x00	RW	cvdn_bl_start
0x400D	BLC_CTRL_0D	0x00	RW	cvdn_bl_end
0x400E	BLC_CTRL_0E	0x00	RW	mf_th
0x400F	BLC_CTRL_0F	0x80	RW	Bit[7]: r_exp_chg_trig_en Bit[6]: r_set_zb Bit[5:4]: r_manu_cvdn_out_en Bit[3]: r_v15_one_channel Bit[2]: r_en_adp_k Bit[1]: r_dc_offset_mode Bit[0]: r_compute_offset_v15

table 4-4 BLC registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x4010	BLC_CTRL_10	0xF0	RW	Bit[7]: off_trig_en Bit[6]: gain_chg_trig_en Bit[5]: fmt_chg_trig_en Bit[4]: rst_trig_en Bit[3]: man_avg_en Bit[2]: man_trig Bit[1]: off_frz_en Bit[0]: off_always_up
0x4011	BLC_CTRL_11	0xFF	RW	Bit[7]: r_off_cmp_man_en Bit[6]: off_chg_mf_en Bit[5]: fmt_chg_mf_en Bit[4]: gain_chg_mf_en Bit[3]: rst_mf_mode Bit[2]: off_chg_mf_mode Bit[1]: fmt_chg_mf_mode Bit[0]: gain_chg_mf_mode
0x4012	BLC_CTRL_12	0x08	RW	Bit[7:0]: rst_trig_fn[7:0]
0x4013	BLC_CTRL_13	0x02	RW	Bit[7:0]: fmt_trig_fn[7:0]
0x4014	BLC_CTRL_14	0x02	RW	Bit[7:0]: gain_trig_fn[7:0]
0x4015	BLC_CTRL_15	0x02	RW	Bit[7:0]: off_trig_fn[7:0]
0x4016	BLC_CTRL_16	0x00	RW	Bit[1:0]: off_trig_th[9:8]
0x4017	BLC_CTRL_17	0x04	RW	Bit[7:0]: off_trig_th[7:0]
0x4020	BLC_CTRL_18	0x00	RW	off_cmp_th000
0x4021	BLC_CTRL_19	0x00	RW	off_cmp_k000
0x4022	BLC_CTRL_1A	0x00	RW	off_cmp_th001
0x4023	BLC_CTRL_1B	0x00	RW	off_cmp_k001
0x4024	BLC_CTRL_1C	0x00	RW	off_cmp_th010
0x4025	BLC_CTRL_1D	0x00	RW	off_cmp_k010
0x4026	BLC_CTRL_1E	0x00	RW	off_cmp_th011
0x4027	BLC_CTRL_1F	0x00	RW	off_cmp_k011
0x4030	BLC_CTRL_20	0x00	RW	Bit[1:0]: off_man000[9:8]
0x4031	BLC_CTRL_21	0x00	RW	Bit[7:0]: off_man000[7:0]
0x4032	BLC_CTRL_22	0x00	RW	Bit[1:0]: off_man001[9:8]
0x4033	BLC_CTRL_23	0x00	RW	Bit[7:0]: off_man001[7:0]
0x4034	BLC_CTRL_24	0x00	RW	Bit[1:0]: off_man010[9:8]

table 4-4 BLC registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x4035	BLC_CTRL_25	0x00	RW	Bit[7:0]: off_man010[7:0]
0x4036	BLC_CTRL_26	0x00	RW	Bit[1:0]: off_man011[9:8]
0x4037	BLC_CTRL_27	0x00	RW	Bit[7:0]: off_man011[7:0]
0x4038	BLC_CTRL_28	0x00	RW	Bit[1:0]: off_man100[9:8]
0x4039	BLC_CTRL_29	0x00	RW	Bit[7:0]: off_man100[7:0]
0x403A	BLC_CTRL_2A	0x00	RW	Bit[1:0]: off_man101[9:8]
0x403B	BLC_CTRL_2B	0x00	RW	Bit[7:0]: off_man101[7:0]
0x403C	BLC_CTRL_2C	0x00	RW	Bit[1:0]: off_man110[9:8]
0x403D	BLC_CTRL_2D	0x00	RW	Bit[7:0]: off_man110[7:0]
0x403E	BLC_CTRL_2E	0x00	RW	Bit[1:0]: off_man111[9:8]
0x403F	BLC_CTRL_2F	0x00	RW	Bit[7:0]: off_man111[7:0]
0x4040	ZERO_ADDR_0	0x00	RW	Bit[7:0]: zl_start
0x4041	ZERO_ADDR_1	0x05	RW	Bit[7:0]: zl_end
0x4042	BLC_CTRL_30	0x00	RW	Bit[1:0]: kcoef_b_man[9:8]
0x4043	BLC_CTRL_31	0x80	RW	Bit[7:0]: kcoef_b_man[7:0]
0x4044	BLC_CTRL_32	0x00	RW	Bit[1:0]: kcoef_gb_man[9:8]
0x4045	BLC_CTRL_33	0x80	RW	Bit[7:0]: kcoef_gb_man[7:0]
0x4046	BLC_CTRL_34	0x00	RW	Bit[1:0]: kcoef_gr_man[9:8]
0x4047	BLC_CTRL_35	0x80	RW	Bit[7:0]: kcoef_gr_man[7:0]
0x4048	BLC_CTRL_36	0x00	RW	Bit[1:0]: kcoef_r_man[9:8]
0x4049	BLC_CTRL_37	0x80	RW	Bit[7:0]: kcoef_r_man[7:0]
0x404A	BLC_CTRL_38	0x30	RW	r_dc_th_1
0x404B	BLC_CTRL_39	0x18	RW	r_dc_th_2
0x404C	BLC_CTRL_3A	0x00	RW	Bit[5:0]: avg_weight
0x404D	BLC_CTRL_3B	0x00	RW	Bit[1:0]: rnd_gain_th[9:8]
0x404E	BLC_CTRL_3C	0x00	RW	Bit[7:0]: rnd_gain_th[7:0]
0x404F	BLC_CTRL_3D	0x00	RW	Bit[7:0]: r_dc_th_1_s
0x4050	BLC_CTRL_3E	0x00	RW	Bit[7:0]: r_dc_th_2_s
0x4060	BLC_OFFSET_0	–	R	Bit[1:0]: blc_offset000[9:8]
0x4061	BLC_OFFSET_1	–	R	Bit[7:0]: blc_offset000[7:0]

table 4-4 BLC registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x4062	BLC_OFFSET_2	–	R	Bit[1:0]: blc_offset001[9:8]
0x4063	BLC_OFFSET_3	–	R	Bit[7:0]: blc_offset001[7:0]
0x4064	BLC_OFFSET_4	–	R	Bit[1:0]: blc_offset010[9:8]
0x4065	BLC_OFFSET_5	–	R	Bit[7:0]: blc_offset010[7:0]
0x4066	BLC_OFFSET_6	–	R	Bit[1:0]: blc_offset011[9:8]
0x4067	BLC_OFFSET_7	–	R	Bit[7:0]: blc_offset011[7:0]
0x4068	BLC_OFFSET_8	–	R	Bit[1:0]: blc_offset100[9:8]
0x4069	BLC_OFFSET_9	–	R	Bit[7:0]: blc_offset100[7:0]
0x406A	BLC_OFFSET_10	–	R	Bit[1:0]: blc_offset101[9:8]
0x406B	BLC_OFFSET_11	–	R	Bit[7:0]: blc_offset101[7:0]
0x406C	BLC_OFFSET_12	–	R	Bit[1:0]: blc_offset110[9:8]
0x406D	BLC_OFFSET_13	–	R	Bit[7:0]: blc_offset110[7:0]
0x406E	BLC_OFFSET_14	–	R	Bit[1:0]: blc_offset111[9:8]
0x406F	BLC_OFFSET_15	–	R	Bit[7:0]: blc_offset111[7:0]
0x4070	BLC_CMP_0	–	R	Bit[7:0]: off_cmp_k_00[7:0]
0x4071	BLC_CMP_1	–	R	Bit[7:0]: off_cmp_k_01[7:0]
0x4072	BLC_CMP_2	–	R	Bit[7:0]: off_cmp_k_10[7:0]
0x4073	BLC_CMP_3	–	R	Bit[7:0]: off_cmp_k_11[7:0]
0x4074	REAL_GAIN_L_0	–	R	Bit[1:0]: long ana_real_gain[9:8]
0x4075	REAL_GAIN_L_1	–	R	Bit[7:0]: long ana_real_gain[7:0]
0x4076	REAL_GAIN_S_0	–	R	Bit[1:0]: short ana_real_gain[9:8]
0x4077	REAL_GAIN_S_1	–	R	Bit[7:0]: short ana_real_gain[7:0]
0x4080	CMP_0	–	R	Bit[2:0]: cmp_00[10:8]
0x4081	CMP_1	–	R	Bit[7:0]: cmp_00[7:0]
0x4082	CMP_2	–	R	Bit[2:0]: cmp_01[10:8]
0x4083	CMP_3	–	R	Bit[7:0]: cmp_01[7:0]
0x4084	CMP_4	–	R	Bit[2:0]: cmp_10[10:8]
0x4085	CMP_5	–	R	Bit[7:0]: cmp_10[7:0]
0x4086	CMP_6	–	R	Bit[2:0]: cmp_11[10:8]
0x4087	CMP_7	–	R	Bit[7:0]: cmp_11[7:0]

table 4-4 BLC registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x4088	K_COEF_B_0	–	R	Bit[1:0]: kcoef_b[9:8]
0x4089	K_COEF_B_1	–	R	Bit[7:0]: kcoef_b[7:0]
0x408A	K_COEF_GB_0	–	R	Bit[1:0]: kcoef_gb[9:8]
0x408B	K_COEF_GB_1	–	R	Bit[7:0]: kcoef_gb[7:0]
0x408C	K_COEF_GR_0	–	R	Bit[1:0]: kcoef_gr[9:8]
0x408D	K_COEF_GR_1	–	R	Bit[7:0]: kcoef_gr[7:0]
0x408E	K_COEF_R_0	–	R	Bit[1:0]: kcoef_r[9:8]
0x408F	K_COEF_R_1	–	R	Bit[7:0]: kcoef_r[7:0]
0x4090	BLC_CTRL_3F	0x14	RW	Bit[7]: cmp_flip_auto_old_en Bit[6]: kcoef_flip_auto_old_en Bit[5]: of_read_prec_sel Bit[4]: data_width_mode Bit[3]: cvdnblc_en Bit[2]: hdr_mode Bit[1]: format_trig_beh Bit[0]: gain_trig_beh
0x4091	BLC_CTRL_40	0x00	RW	Bit[7]: cmp_mirror_man Bit[6]: cmp_mirror_man_en Bit[5]: cmp_flip_man Bit[4]: cmp_flip_man_en Bit[3]: kcoef_mirror_man Bit[2]: kcoef_mirror_man_en Bit[1]: kcoef_flip_man Bit[0]: kcoef_flip_man_en
0x4092	BLC_CTRL_41	0x00	RW	Bit[2]: off_man_mirror_man Bit[1]: off_man_mirror_man_en
0x40A0	CMP_S_0	–	R	Bit[2:0]: cmp_00_s_i[10:8]
0x40A1	CMP_S_1	–	R	Bit[7:0]: cmp_00_s_i[7:0]
0x40A2	CMP_S_2	–	R	Bit[2:0]: cmp_01_s_i[10:8]
0x40A3	CMP_S_3	–	R	Bit[7:0]: cmp_01_s_i[7:0]
0x40A4	CMP_S_4	–	R	Bit[2:0]: cmp_10_s_i[10:8]
0x40A5	CMP_S_5	–	R	Bit[7:0]: cmp_10_s_i[7:0]
0x40A6	CMP_S_6	–	R	Bit[2:0]: cmp_11_s_i[10:8]
0x40A7	CMP_S_7	–	R	Bit[7:0]: cmp_11_s_i[7:0]
0x40B0	BLC_CTRL_42	0x00	RW	Bit[0]: thres_en_o

table 4-4 BLC registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x40B1	BLC_CTRL_43	0x00	RW	Bit[4]: hist_win_dis_o Bit[1:0]: thres_stepfine_o
0x40B2	BLC_CTRL_44	0x00	RW	thres_delta_o
0x40B3	BLC_CTRL_45	0x00	RW	Bit[3:0]: thres_hist_cutoff[11:8]
0x40B4	BLC_CTRL_46	0x00	RW	Bit[7:0]: thres_hist_cutoff[7:0]
0x40B5	BLC_CTRL_47	0x00	RW	Bit[4:0]: thres_delta_cutoff
0x40B6	BLC_CTRL_48	0x00	RW	Bit[0]: thres_man_en
0x40B7	BLC_CTRL_49	0x00	RW	Bit[3:0]: thres_man[11:8]
0x40B8	BLC_CTRL_4A	0x00	RW	Bit[7:0]: thres_man[7:0]
0x40B9	BLC_CTRL_4B	0x00	RW	blc_hist_start
0x40BA	BLC_CTRL_4C	0x00	RW	Bit[2]: gate_data_en Bit[1]: gate_clk_en Bit[0]: dummy_out_en

5 image sensor processor digital functions

5.1 ISP top

The main purpose of the ISP top includes:

- integrate all sub-modules
- create necessary control signals

table 5-1 ISP top registers

address	register name	default value	R/W	description
0x5000	ISP_CTRL_0	0x29	RW	Bit[7]: WIN enable Bit[5]: DPC enable Bit[3]: AWB_GAIN enable Bit[0]: ISP enable

5.2 staggered high dynamic range (staggered HDR)

HDR mode increases image dynamic range by capturing multiple exposures of a similar scene and then combining them into one single image. The OS04C10 supports staggered HDR mode.

In staggered HDR mode, long/short exposure frames overlap each other. The overlapping reduces the timing delay between various exposure frames that combine to form one HDR frame. The overlapping also reduces the frame/line buffer needed for backend sensors. The frame timing for staggered HDR is shown in **figure 5-1**.

The OS04C10 uses a MIPI channel to differentiate different exposure frames. Long/short frames use MIPI virtual channel VC0/VC1 respectively, in order for different exposure frames to not mix signals on the MIPI receiver side.

figure 5-1 two set staggered HDR

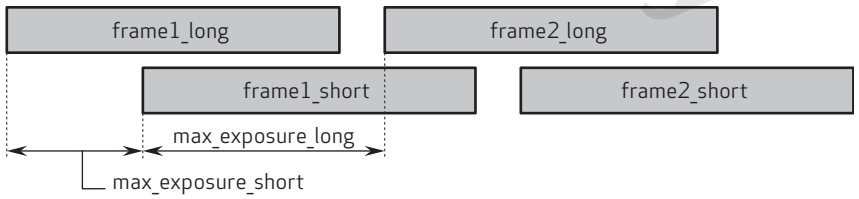


table 5-2 staggered HDR control register

address	register name	default value	R/W	description
0x3821	TIMING_REG_36	0x00	RW	Bit[2]: r_stg_hdr_en

5.3 pre_DSP

The main purposes of the pre_DSP module include:

- adjust HREF, valid, RBlue signals, and data
- create color bar image
- determine the sizes of input images by removing redundant data
- create control signals

table 5-3 pre_DSP registers

address	register name	default value	R/W	description
0x5080	ISP_CTRL_0	0x04	RW	Bit[7]: Test enable 0: Disable 1: Enable Bit[6]: Rolling enable (rolling bar in test mode) 0: Disable 1: Enable Bit[5]: Transparent effect enable 0: Disable 1: Enable Bit[4]: Black/white or color square selection 0: Color 1: Black/white Bit[3:2]: Color bar style Bit[1:0]: Test mode select

5.4 defective pixel cancellation (DPC)

The main purpose of the DPC function is to remove white/black defect pixels. If the pixel is defective, DPC will use a value calculated from the neighboring normal pixels to replace it.

table 5-4 DPC control registers

address	register name	default value	R/W	description
0x5200	ISP_CTRL_0	0x1B	RW	Bit[7]: Enable tail Bit[6]: Enable tailing cluster Bit[5]: Enable 3x3 cluster Bit[4]: Enable saturate cross cluster Bit[3]: Enable cross cluster Bit[2]: Manual mode enable Bit[1]: Black pixel enable Bit[0]: White pixel enable

5.5 window cut (WINC)

The main purpose of the WINC module is to make the image size real size by removing offset.

table 5-5 WINC registers

address	register name	default value	R/W	description
0x5800	ISP_CTRL_0	0x00	RW	Bit[3:0]: Window X start[11:8]
0x5801	ISP_CTRL_1	0x00	RW	Bit[7:0]: Window X start[7:0]
0x5802	ISP_CTRL_2	0x00	RW	Bit[3:0]: Window Y start[11:8]
0x5803	ISP_CTRL_3	0x00	RW	Bit[7:0]: Window Y start[7:0]
0x5804	ISP_CTRL_4	0x02	RW	Bit[3:0]: Window width[11:8]
0x5805	ISP_CTRL_5	0x80	RW	Bit[7:0]: Window width[7:0]
0x5806	ISP_CTRL_6	0x01	RW	Bit[3:0]: Window height[11:8]
0x5807	ISP_CTRL_7	0xE0	RW	Bit[7:0]: Window height[7:0]
0x5808	ISP_CTRL_8	0x00	RW	Bit[7:3]: emb_num Bit[2]: emb_flag_sel 0: Start line 1: End line Bit[0]: win_man_en 0: Window size from window top 1: Window size from register

5.6 exposure and gain control

Manual exposure and gain provide controls to change sensor exposure and gain. The OS04C10 has linear mode and 2-exposure staggered HDR mode. In HDR mode, there are two sets of exposure and gain control registers.

In rolling shutter sensor, exposure always takes effect at N+2 frame. The exposure control registers in linear and HDR mode are as follows:

In linear mode:

- Exp_0 = (0x3501, 0x3502[7:0]) x time_of_1line, exposure range from 2 line up to VTS - 8

In 2-exposure staggered HDR mode:

- Exp_0 = (0x3501, 0x3502[7:0]) x time_of_1line, exposure range from 2 line up to VTS - 8
- Exp_1 = (0x3511, 0x3512[7:0]) x time_of_1line, exposure range from 2 line up to VTS - Exp_0 - 12

Analog gain range is from 1x to 15.5 x, and can be set manually in the registers shown below. By default, analog gain takes effect at the same frame (N+2) as exposure frame takes effect.

- 0x3508[5:0], 0x3509[7:0] for linear, long channel (staggered), 0x0080 is 1x gain
- 0x350C[5:0], 0x350D[7:0] for short channel (staggered), 0x0080 is 1x gain.

table 5-6 AEC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3501	LONG EXPO	0x00	RW	Bit[7:0]: Long exposure[15:8]
0x3502	LONG EXPO	0x40	RW	Bit[7:0]: Long exposure[7:0]

table 5-6 AEC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3503	AEC MANUAL	0x88	RW	Bit[7]: AGC select 0: Real gain auto 1: Real gain manual Bit[6]: Digital fraction gain delay option 0: Delay 1 frame 1: Do not delay 1 frame Bit[5]: Gain change delay option 0: Delay 1 frame 1: Do not delay 1 frame Bit[4]: Gain delay option 0: Delay 1 frame 1: Do not delay 1 frame Bit[3]: AEC select 0: Exposure auto 1: Exposure manual Bit[2]: Gain manual as sensor gain 0: Input gain as real gain format 1: Input gain as sensor gain format Bit[1]: Exposure delay option (must be 0) 0: Delay 1 frame Bit[0]: Exposure change delay option (must be 0) 0: Delay 1 frame
0x3505	GCVT OPTION	0x83	RW	Gain Conversion Option Bit[7]: DAC fixed gain bit Bit[6:4]: Sensor gain fixed bit Bit[3:2]: Sensor gain pregain option (debug only, always set to 0) Bit[1:0]: Sensor gain option for transferring real gain to sensor gain format
0x3507	GAIN SHIFT	0x00	RW	Bit[3]: fine_snr_gain_16_en Back gain enable Bit[2]: priority_6: switch_snr_gain_en 0: dac[2:0]_comp[1:0] 1: comp[1:0]_dac[2:0] Bit[1:0]: Gain shift option 00: No shift 01: Left shift 1 bit 10: Left shift 2 bits 11: Left shift 3 bits
0x3508	LONG GAIN	0x00	RW	Bit[5:0]: Long gain[13:8]

table 5-6 AEC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3509	LONG GAIN	0x80	RW	Bit[7:0]: Long gain[7:0] 0x3503[2] = 0, gain[12:0] is real gain format, where low 7 bits are fraction bits, real_gain = gain[12:0]/128; for example: 0x080 is 1x gain, 0x100 is 2x gain; if 0x3503[2] = 1, gain[12:0] is sensor gain format, gain[12:8] is coarse gain, 00000: 1x, 00001: 2x, 00011: 4x, 00111: 8x, gain[7] is 1, gain[6:3] is fine gain, gain[2:0] is always 0; for example: 0x080 is 1x gain, 0x180 is 2x gain, 0x380 is 4x gain
0x350A	LONG DIGIGAIN	0x04	RW	Bit[5:0]: Long digital gain[13:8] 4.10 format
0x350B	LONG DIGIGAIN	0x00	RW	Bit[7:0]: Long Digital gain[7:0] 4.10 format
0x350C	SHORT GAIN	0x00	RW	Bit[5:0]: Short gain[13:8]
0x350D	SHORT GAIN	0x80	RW	Bit[7:0]: Short gain[7:0]
0x350E	SHORT DIGIGAIN	0x04	RW	Bit[5:0]: Short digital gain[13:8]
0x350F	SHORT DIGIGAIN	0x00	RW	Bit[7:0]: Short digital gain[7:0]
0x3511	SHORT EXPO	0x00	RW	Bit[7:0]: Short exposure[15:8]
0x3512	SHORT EXPO	0x20	RW	Bit[7:0]: Short exposure[7:0]
0x3513	SNR_GAIN_L	–	R	Bit[5:0]: Long sensor gain[13:8]
0x3514	SNR_GAIN_L	–	R	Bit[7:0]: Long sensor gain[7:0]
0x3515	FINE_SNR_GAIN_L	–	R	Bit[5:0]: Long fine sensor gain
0x3516	SNR_GAIN_S	–	R	Bit[5:0]: Short sensor gain[13:8]
0x3517	SNR_GAIN_S	–	R	Bit[7:0]: Short sensor gain[7:0]
0x3518	FINE_SNR_GAIN_S	–	R	Bit[5:0]: Short fine sensor gain

table 5-6 AEC control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3519	GAIN_DELAY_SWAP_OPTION	0x00	RW	Bit[1]: digital_gain apply select 0: Digital gain apply in BLC 1: Digital gain apply in MAWB Bit[0]: Auto gain delay option 0: Real gain and digital gain delay manual mode 1: Real gain and digital gain delay will auto sync with expo; when expo and gain change at same time, both gains will delay 1 frame to sync with expo; otherwise, gain will have no frame delay
0x351A	GAIN_CUR_L	–	R	Bit[7:0]: Current long gain[7:0]
0x351B	GAIN_CUR_L	–	R	Bit[7:0]: Current long gain[13:8]
0x351C	GAIN_CUR_S	–	R	Bit[7:0]: Current short gain[7:0]
0x351D	GAIN_CUR_S	–	R	Bit[7:0]: Current short gain[13:8]
0x351E	EXPO_CUR_L	–	R	Bit[7:0]: Current long expo[11:4]
0x351F	EXPO_CUR_L	–	R	Bit[7:0]: Current long expo[19:12]
0x3520	EXPO_CUR_S	–	R	Bit[7:0]: Current short expo[11:4]
0x3521	EXPO_CUR_S	–	R	Bit[7:0]: Current short expo[19:12]
0x3522	DIGI_CUR_L	–	R	Bit[7:0]: Current long digital gain[7:0]
0x3523	DIGI_CUR_L	–	R	Bit[7:0]: Current long digital gain[13:8]
0x3524	DIGI_CUR_S	–	R	Bit[7:0]: Current short digital gain[7:0]
0x3525	DIGI_CUR_S	–	R	Bit[7:0]: Current short digital gain[13:8]
0x3526	EXPO_CUR_L	–	R	Bit[7:0]: expo_cur_l_i[23:16]
0x3527	EXPO_CUR_S	–	R	Bit[7:0]: expo_cur_s_i[23:16]

5.7 MAWB gain

The RAW R/G/B values of a gray object vary with the spectrum of the illumination and the sensor spectral response. The illumination spectrum is usually described by "color temperature", which is the surface temperature of a black body radiating equivalent spectrum. In the real world, light color temperature ranges from very low (reddish) to very high (bluish) value. For example, the color temperature of an incandescent lamp is around 2850K, while the color temperature of an overcast day is around 6500K.

To make sure that a gray image is truly gray, the sensor needs to adjust the gain for each color channel according to the color temperature. This process is called white balance (WB).

White balanced gain is enabled by default and can be disabled by register 0x5000[3]. The manual white balance (MWB), controlled by registers 0x5100~0x5105 and 0x5140~0x5145, provides gain for R, G, and B channels. Each channel gain is 12-bit. 0x400 is 1x gain. Maximum 4x gain is 0xFFF.

White balance gain does not have an internal latch function. Once it is set, it will take effect immediately.

table 5-7 frame_length and row_length registers

address	register name	default value	R/W	description
0x5100	ISP_CTRL_0_L	0x04	RW	Bit[3:0]: awb_gain_B_L[11:8]
0x5101	ISP_CTRL_1_L	0x00	RW	Bit[7:0]: awb_gain_B_L[7:0]
0x5102	ISP_CTRL_2_L	0x04	RW	Bit[3:0]: awb_gain_G_L[11:8]
0x5103	ISP_CTRL_3_L	0x00	RW	Bit[7:0]: awb_gain_G_L[7:0]
0x5104	ISP_CTRL_4_L	0x04	RW	Bit[3:0]: awb_gain_R_L[11:8]
0x5105	ISP_CTRL_5_L	0x00	RW	Bit[7:0]: awb_gain_R_L[7:0]
0x5106	ISP_CTRL_6_L	0x02	RW	Bit[5:0]: digigain_L[13:8]
0x5107	ISP_CTRL_7_L	0x00	RW	Bit[7:0]: digigain_L[7:0]
0x5140	ISP_CTRL_0_S	0x04	RW	Bit[3:0]: awb_gain_B_S[11:8]
0x5141	ISP_CTRL_1_S	0x00	RW	Bit[7:0]: awb_gain_B_S[7:0]
0x5142	ISP_CTRL_2_S	0x04	RW	Bit[3:0]: awb_gain_G_S[11:8]
0x5143	ISP_CTRL_3_S	0x00	RW	Bit[7:0]: awb_gain_G_S[7:0]
0x5144	ISP_CTRL_4_S	0x04	RW	Bit[3:0]: awb_gain_R_S[11:8]
0x5145	ISP_CTRL_5_S	0x00	RW	Bit[7:0]: awb_gain_R_S[7:0]
0x5146	ISP_CTRL_6_S	0x02	RW	Bit[5:0]: digigain_S[13:8]
0x5147	ISP_CTRL_7_S	0x00	RW	Bit[7:0]: digigain_S[7:0]

6 register tables

The following tables provide descriptions of the device control registers contained in the OS04C10. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x6C for write and 0x6D for read (when SID=1, 0x20 for write and 0x21 for read).

6.1 PLL control [0x0100, 0x0103, 0x0300 - 0x0307, 0x0320 - 0x0329]

table 6-1 PLL control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x0100	SC_CTRL0100	0x00	RW	Bit[7:1]: Debug mode Bit[0]: software_standby 0: software_standby 1: Streaming
0x0103	SC_CTRL0103	–	W	Bit[7:1]: Debug mode Bit[0]: software_reset
0x0300	RSVD	–	–	Reserved
0x0301	PLL_CTRL_01	0x84	RW	Bit[7:6]: r_pll1_divsys_o Bit[5]: r_pll1_predivp_o Bit[4]: Reserved Bit[3:2]: r_pll1_divs_o Bit[1:0]: Reserved
0x0302	RSVD	–	–	Reserved
0x0303	PLL_CTRL_03	0x10	RW	Bit[7:3]: Reserved Bit[2:0]: r_pll1_prediv_o
0x0304	PLL_CTRL_04	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: r_pll1_divp_o[9:8]
0x0305	PLL_CTRL_05	0x5A	RW	Bit[7:0]: r_pll1_divp_o[7:0]
0x0306	PLL_CTRL_06	0xH0	RW	Bit[7:2]: Reserved Bit[1:0]: r_pll1_divpix_o
0x0307	PLL_CTRL_07	0x10	RW	Bit[7:5]: Reserved Bit[4]: r_pll1_lock_det_en_o Bit[3:2]: r_pll1_precision_o Bit[1:0]: r_pll1_cnt_ref_o
0x0320	PLL_CTRL_20	0x10	RW	Bit[7:5]: Reserved Bit[4]: r_pll2_vcoby2_o Bit[3]: r_pll2_band_sel_o Bit[2]: pll2_rst_o Bit[1]: r_pll2_div_rst_sync_en_o Bit[0]: r_pll2_bypass_o

table 6-1 PLL control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x0321~ 0x0322	RSVD	–	–	Reserved
0x0323	PLL_CTRL_23	0x04	RW	Bit[7:3]: Reserved Bit[2:0]: r_pll2_prediv_o
0x0324	PLL_CTRL_24	0x02	RW	Bit[7:2]: Reserved Bit[1:0]: r_pll2_divp_o[9:8]
0x0325	PLL_CTRL_25	0xBC	RW	Bit[7:0]: r_pll2_divp_o[7:0]
0x0326	PLL_CTRL_26	0x82	RW	Bit[7]: r_pll2_predivp_o Bit[6:2]: Reserved Bit[1:0]: r_pll2_divsa1_o
0x0327	PLL_CTRL_27	0x04	RW	Bit[7:3]: Reserved Bit[2:0]: r_pll2_divsram_o
0x0328	NOT USED	–	–	Not Used
0x0329	PLL_CTRL_29	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: r_pll2_divdac_o

6.2 AEC control [0x3500 - 0x3503, 0x3505, 0x3507 - 0x3527]

table 6-2 AEC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3500	LONG EXPO	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Long exposure[23:16]
0x3501	LONG EXPO	0x00	RW	Bit[7:0]: Long exposure[15:8]
0x3502	LONG EXPO	0x40	RW	Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits

table 6-2 AEC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3503	AEC MANUAL	0x88	RW	Bit[7]: AGC select 0: Real gain auto 1: Real gain manual Bit[6]: Digital fraction gain delay option 0: Delay 1 frame 1: Not delay 1 frame Bit[5]: Reserved Bit[4]: Gain delay option 0: Delay 1 frame 1: Not delay 1 frame Bit[3]: AEC select 0: Exposure auto 1: Exposure manual Bit[2]: Gain manual as sensor gain 0: Input gain as real gain format 1: Input gain as sensor gain format Bit[1]: Exposure delay option (must be 0) 0: Delay 1 frame 1: Not used Bit[0]: Digital fraction gain delay option 0: Delay 1 frame 1: Not used
0x3505	GCVT OPTION	0x83	RW	Gain Conversation Option Bit[7]: DAC fixed gain bit Bit[6:4]: Sensor gain fixed bit Bit[3:2]: Sensor gain pregain option (debug only, always set it to 0) Bit[1:0]: Sensor gain option for transferring real gain to sensor gain format
0x3507	GAIN SHIFT	0x00	RW	Bit[7:4]: Reserved Bit[3]: fine_snr_gain_16_en Back gain enable Bit[2]: priority_6 switch_snr_gain_en 0: DAC[2:0]_comp[1:0] 1: Comp[1:0]_dac[2:0] Bit[1:0]: Gain shift option 00: No shift 01: Left shift 1 bit 10: Left shift 2 bits 11: Left shift 3 bits
0x3508	LONG GAIN	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Long gain[13:8]

table 6-2 AEC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3509	LONG GAIN	0x80	RW	Bit[7:0]: Long gain[7:0] If 0x3503[2] = 0, gain[12:0] is real gain format, where low 7 bits are fraction bits, real_gain = gain[12:0]/128, for example: 0x080 is 1x gain, 0x100 is 2x gain If 0x3503[2] = 1, gain[12:0] is sensor gain format, gain[12:8] is coarse gain, 00000: 1x, 00001: 2x, 00011: 4x, 00111: 8x, gain[7] is 1, gain[6:3] is fine gain, gain[2:0] is always 0 For example: 0x080 is 1x gain, 0x180 is 2x gain, 0x380 is 4x gain
0x350A	LONG DIGIGAIN	0x04	RW	Bit[7:6]: Reserved Bit[5:0]: Long digital gain[13:8] 4.10 format
0x350B	LONG DIGIGAIN	0x00	RW	Bit[7:0]: Long digital gain[7:0] 4.10 format
0x350C	SHORT GAIN	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Short gain[13:8]
0x350D	SHORT GAIN	0x80	RW	Bit[7:0]: Short gain[7:0]
0x350E	SHORT DIGIGAIN	0x04	RW	Bit[7:6]: Reserved Bit[5:0]: Short digital gain[13:8]
0x350F	SHORT DIGIGAIN	0x00	RW	Bit[7:0]: Short digital gain[7:0]
0x3510	SHORT EXPO	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Short exposure[19:16]
0x3511	SHORT EXPO	0x00	RW	Bit[7:0]: Short exposure[15:8]
0x3512	SHORT EXPO	0x20	RW	Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits
0x3513	SNR_GAIN_L	–	R	Bit[7:6]: Reserved Bit[5:0]: Long sensor gain[13:8]
0x3514	SNR_GAIN_L	–	R	Bit[7:0]: Long sensor gain7:0]
0x3515	FINE_SNR_GAIN_L	–	R	Bit[7:6]: Reserved Bit[5:0]: Long fine sensor gain
0x3516	SNR_GAIN_S	–	R	Bit[7:6]: Reserved Bit[5:0]: Short sensor gain[13:8]
0x3517	SNR_GAIN_S	–	R	Bit[7:0]: Short sensor gain[7:0]
0x3518	FINE_SNR_GAIN_S	–	R	Bit[7:6]: Reserved Bit[5:0]: Short fine sensor gain

table 6-2 AEC control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3519	GAIN_DELAY_SWAP_OPTION	0x00	RW	Bit[7:3]: Reserved Bit[2]: Debug mode No need to change Bit[1]: digital_gain apply select 0: Digital gain apply in BLC 1: Digital gain apply in MAWB Bit[0]: Auto gain delay option 0: Real gain and digital gain delay manual mode 1: Real gain and digital gain delay will auto sync with expo; when expo and gain change at same time, both gain will delay 1 frame to sync with expo; otherwise, gain will have no frame delay
0x351A	GAIN_CUR_L	–	R	Bit[7:0]: Current long gain[7:0]
0x351B	GAIN_CUR_L	–	R	Bit[7:0]: Current long gain[15:8]
0x351C	GAIN_CUR_S	–	R	Bit[7:0]: Current short gain[7:0]
0x351D	GAIN_CUR_S	–	R	Bit[7:0]: Current short gain[15:8]
0x351E	EXPO_CUR_L	–	R	Bit[7:0]: Current long expo[11:4]
0x351F	EXPO_CUR_L	–	R	Bit[7:0]: Current long expo[19:12]
0x3520	EXPO_CUR_S	–	R	Bit[7:0]: Current short expo[11:4]
0x3521	EXPO_CUR_S	–	R	Bit[7:0]: Current short expo[19:12]
0x3522	DIGI_CUR_L	–	R	Bit[7:0]: Current long digital gain[7:0]
0x3523	DIGI_CUR_L	–	R	Bit[7:0]: Current long digital gain[15:8]
0x3524	DIGI_CUR_S	–	R	Bit[7:0]: Current short digital gain[7:0]
0x3525	DIGI_CUR_S	–	R	Bit[7:0]: Current short digital gain[15:8]
0x3526	EXPO_CUR_L	–	R	Bit[7:0]: expo_cur_l_i[23:16]
0x3527	EXPO_CUR_S	–	R	Bit[7:0]: expo_cur_s_i[23:16]

6.3 system control [0x3000 - 0x3008, 0x300A - 0x300C, 0x300E - 0x3026, 0x302A]

table 6-3 system control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3000	PAD OEN0	0xH0	RW	Bit[7:4]: Reserved Bit[3:0]: p_y_oen[11:8]
0x3001	PAD OEN1	0x00	RW	Bit[7:0]: p_y_oen[7:0]
0x3002	PAD OEN2	0x21	RW	Bit[7:6]: Reserved Bit[5]: p_gpio_oen Bit[4]: Reserved Bit[3]: p_pclk_oen Bit[2]: p_href_oen Bit[1]: p_vsync_oen Bit[0]: p_fsin_oen
0x3003	SCCB_ID	0x6C	RW	Bit[7:0]: SCCB programmable ID
0x3004	SCCB ID	0x20	RW	Bit[7:0]: sccb_id SCCB backup programed ID
0x3005	SCCB_ID_2	0x42	RW	Bit[7:0]: sccb_id2
0x3006	PAD_OUT0	0xH0	RW	Bit[7:4]: Reserved Bit[3:0]: io_y[11:8]
0x3007	PAD_OUT1	0x00	RW	Bit[7:0]: io_y[7:0]
0x3008	PAD_OUT2	0x00	RW	Bit[7:6]: Reserved Bit[5]: io_gpio (select this one as output of GPIO) Bit[4]: io_vsync Bit[3]: io_href Bit[2]: io_pclk Bit[1]: io_fsin Bit[0]: io_sda
0x300A	CHIP ID	–	R	Bit[7:0]: chip_id[23:16]
0x300B	CHIP ID	–	R	Bit[7:0]: chip_id[15:8]
0x300C	CHIP ID	–	R	Bit[7:0]: chip_id[7:0]
0x300E	PAD SEL0	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: io_y_sel[11:8]
0x300F	PAD SEL1	0x00	RW	Bit[7:0]: io_y_sel[7:0]

table 6-3 system control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3010	PAD SEL2	0x00	RW	Bit[7:6]: Reserved Bit[5]: io_gpio_sel Bit[4]: io_vsync_sel Bit[3]: io_href_sel Bit[2]: io_pclk_sel Bit[1]: io_fsin_sel Bit[0]: io_sda_sel
0x3011	RSVD	–	–	Reserved
0x3012	CLK_GATE_MASK	0x04	RW	Bit[7]: pclk_dvp_gate_mask Bit[6]: pclk_mipi_gate_mask Bit[5]: pclk_vfifo_gate_mask Bit[4:1]: Reserved Bit[0]: sclk_aec_gate_mask
0x3013	CLK_GATE_MASK	0x00	RW	Bit[7:0]: clk_gate_mask[7:0]
0x3014	RSVD	–	–	Reserved
0x3015	PUMP CLK DIV	0x00	RW	Bit[7]: Reserved Bit[6:4]: Npump clock div Bit[3]: pd_mipi auto signal selection 0: Use original rst as pd_mipi_auto (faster) 1: Use synchronous rst as pd_mipi_auto Bit[2:0]: sclk_aec_gate_mask
0x3016	MIPI SC CTRL	0x32	RW	Bit[7:5]: mipi_lane_mode n+1 lanes Bit[4]: mipi_en 0: MIPI disable, DVP output 1: MIPI enable Bit[3:2]: r_phy_pd_mipi Bit[1]: phy_rst option 0: rst_sync cannot reset PHY 1: Reset PHY when rst_sync Bit[0]: lane_dis option 1: Disable lanes when pd_mipi
0x3017	MIPI SC CTRL	0x00	RW	Bit[7:0]: MIPI lane disable
0x3018	CLK_CTRL	0xF0	RW	Bit[7]: tclk_tc enable Bit[6]: tclk_snr_ctrl enable Bit[5]: srmclk_psram enable Bit[4]: srmclk_syncfifo and sclk_sync_fifo enable Bit[3]: rst_tc Bit[2]: rst_snr_ctrl and psram_ctrl Bit[1]: rst_sync_srmclk Bit[0]: rst_syncfifo

table 6-3 system control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3019	CTRL_R19	0xF0	RW	Bit[7]: Reserved Bit[6]: tclk_strobe Bit[5]: tclk_psv_ctrl Bit[4:3]: Reserved Bit[2]: rst_strobe Bit[1]: rst_psv Bit[0]: Reserved
0x301A	CLKRST0	0xF0	RW	Bit[7]: sclk_gt Bit[6]: sclk_ao Bit[5:4]: Reserved Bit[3]: mipi_phy_rst_o Bit[2:0]: Reserved
0x301B	CLKRST1	0xD0	RW	Bit[7]: sclk_blc enable Bit[6]: sclk_isp enable Bit[5]: sclk_tpm enable Bit[4]: sclk_vfifo Bit[3]: rst_blc Bit[2]: rst_isp Bit[1]: rst_tpm Bit[0]: rst_vfifo
0x301C	CLKRST2	0xF0	RW	Bit[7]: pclk_dvp_enable Bit[6]: sclk_mipi enable Bit[5]: ser_clk enable Bit[4]: sclk_efuse enable Bit[3]: rst_dvp Bit[2]: rst_mipi Bit[1]: Reserved Bit[0]: rst_efuse
0x301D	CLKRST3	0x58	RW	Bit[7]: sclk_asram_tst enable Bit[6]: grp_clk_en Bit[5]: sclk_bist enable Bit[4]: sclk_aec_pk enable Bit[3]: rst_asram_tst Bit[2]: rst_grp Bit[1]: rst_bist Bit[0]: rst_aec_pk
0x301E	CLKRST4	0xB4	RW	Bit[7]: Reserved Bit[6]: pclk_lvds enable Bit[5]: pclk_vfifo_enable Bit[4]: pclk_mipi enable Bit[3]: rst_sd Bit[2]: rst_lvds Bit[1]: rst_gt Bit[0]: rst_ao

table 6-3 system control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x301F	CLKRST5	0xD0	RW	Bit[7]: sclk_fc enable Bit[6]: sclk_isp_fc enable Bit[5]: sclk_dpcm enable Bit[4]: sclk_clip enable Bit[3]: rst_fc Bit[2]: rst_isp_fc Bit[1]: rst_dpcm Bit[0]: rst_clip
0x3020	CLOCK SEL	0x17	RW	Bit[7]: r_spi_ser_clk_sel_o Bit[6]: r_spi_ser_clk_inv Bit[5]: sccb_pgm_id_en Bit[4]: sccb_id2_nack 0: SCCB slave will return normal ACK 1: SCCB slave will not return ACK Bit[3:2]: pclk_sel Bit[1]: pclk_inv Reverse PCLK Bit[0]: sclk2x_sel 0: Choose pll_sclk_i 1: Choose pll_sclk_d2
0x3021	MISC CTRL	0x23	RW	Bit[7:1]: Reserved Bit[0]: cen_global_o
0x3022	MIPI SC CTRL	0x01	RW	Bit[7:4]: mipi_bit_sel 0100: 8-bit mode 0110: 12-bit mode 1000: 16-bit mode Others:Reserved Bit[3]: mipi_lvds_mode_o Bit[2]: Ck lane disable Bit[1]: Ck lane disable 0 Bit[0]: pd_mipi enable when rst_sync
0x3023	RSVD	–	–	Reserved
0x3024	SC CTRL24	0x08	RW	Bit[7]: Reserved Bit[6:0]: s2p_start_size_o
0x3025	SC CTRL25	0xF0	RW	Bit[7]: sclk_skip2 enable Bit[6]: sclk_dither enable Bit[5]: sclk_noise enable Bit[4]: sclk_vap enable Bit[3]: rst_skip2 Bit[2]: rst_dither Bit[1]: rst_noise Bit[0]: rst_vap
0x3026	SC CTRL26	0x00	RW	Bit[7:0]: clk_gate_mask[23:16]
0x302A	CHIP REVISION	–	R	Bit[7:0]: chip_revision

6.4 SCCB control [0x3100 - 0x3109]

table 6-4 SCCB control registers

address	register name	default value	R/W	description
0x3100	SCCB CTRL	0x00	RW	Bit[7:4]: Reserved Bit[3]: r_sda_dly_en Bit[2:0]: r_sda_dly
0x3101	SCCB OPT	0x12	RW	Bit[7:5]: Reserved Bit[4]: en_sccb_adro_inc Bit[3]: r_sda_byp 0: Two CLK stage sync for sda_ 1: No sync for sda_i Bit[2]: r_scl_byp 0: two CLK stage sync for scl_i 1: no sync for scl_i Bit[1]: r_msk_glitch Bit[0]: r_msk_stop
0x3102	SCCB FILTER	0x05	RW	Bit[7:4]: Reserved Bit[3]: scl_chk_en Bit[2:0]: scl_pulse_num_min
0x3103	SCCB SYSREG	0x00	RW	pll_clk_sel
0x3104	PWUP DIS	0x00	RW	pll_byp_rst Bit[7]: pll4_byp Bit[6]: pll4_rst Bit[5]: pll3_rst Bit[4]: pll2_byp Bit[3]: pll2_byp Bit[2]: pll2_rst Bit[1]: pll1_byp Bit[0]: pll1_rst
0x3105	PADCLK DIV	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: padclk_div
0x3106	SRB_CTRL0	0x25	RW	Bit[7:0]: srb_ctrl_o[7:0]
0x3107	SRB_CTRL1	0x81	RW	Bit[7:0]: srb_ctrl_o[15:8]
0x3108	SRB_CTRL2	0xFD	RW	Bit[7:0]: srb_ctrl_o[23:16]
0x3109	SRB_CTRL3	0xE7	RW	Bit[7:0]: srb_ctrl_o[31:24]

6.5 group hold [0x3200 - 0x3206, 0x3208 - 0x320D, 0x3210 - 0x321F]

table 6-5 group hold registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Group0 Start Address in SRAM, Actual Address is {0x3200[5:0], 4'h0}
0x3201	GROUP ADR1	0x80	RW	Group1 Start Address in SRAM, Actual Address is {0x3201[5:0], 4'h0}
0x3202	GROUP ADR2	0x10	RW	Group2 Start Address in SRAM, Actual Address is {0x3202[5:0], 4'h0}
0x3203	GROUP ADR3	0x18	RW	Group3 Start Address in SRAM, Actual Address is {0x3203[5:0], 4'h0}
0x3204	GROUP ADR4	0x20	RW	Group4 Start Address in SRAM, Actual Address is {0x3204[5:0], 4'h0}
0x3205	GROUP ADR5	0x30	RW	Group5 Start Address in SRAM, Actual Address is {0x3205[5:0], 4'h0}
0x3206	FSIN_GRP	0x10	RW	Bit[7:5]: Reserved Bit[4]: fsin_en Bit[3:2]: Reserved Bit[1:0]: Start group in FSIN mode
0x3208	GROUP ACCESS	–	W	Bit[7:5]: Reserved 0000: Group hold start 0001: Group hold end 1010: Group launch Others:Reserved Bit[3:0]: Group ID 0000: Group bank 0 0000: Group bank 1 0000: Group bank 2 0000: Group bank 3 Others:Reserved
0x3209	GRP0_PERIOD	0x00	RW	Number of Frames Staying in Group 0
0x320A	GRP1_PERIOD	0x00	RW	Number of Frames Staying in Group 1
0x320B	GRP2_PERIOD	0x00	RW	Number of Frames Staying in Group 2
0x320C	GRP3_PERIOD	0x00	RW	Number of Frames Staying in Group 3
0x320D	GRP_SWCTRL	0x01	RW	Bit[7:6]: Reserved Bit[5]: Repeat switch mode Bit[4]: Context switch enable Bit[3:2]: Reserved Bit[1:0]: Switch bank group
0x3210	GROUP LEN0	–	W	Length of Group0

table 6-5 group hold registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3211	GROUP LEN1	–	W	Length of Group1
0x3212	GROUP LEN2	–	W	Length of Group2
0x3213	GROUP LEN3	–	W	Length of Group3
0x3214	GROUP LEN4	–	W	Length of Group4
0x3215	GROUP LEN5	–	W	Length of Group5
0x3216	EMB_LINE_NUM	0x10	RW	Bit[7:4]: Reserved Bit[3:0]: emb_line_num
0x3217	EMB_LINE_PADDING_DATA	0x00	RW	Bit[7:0]: emb_line padding data
0x3218	EMB_LINE_SEL_CONTROL	0x00	RW	Bit[7:6]: emb_line blanking select 00: 32 SCLK 01: 64 SCLK 10: 128 SCLK 11: Wait for next trigger signal Bit[5]: emb_line address enable Bit[4]: r_padding_md2 0: No dummy data mixing with valid data 1: Dummy data output with valid data every cycle Bit[3]: frame_trigger_sel 0: tc_grp_wr 1: EOG Bit[2]: emb_line_eof_enable Bit[1]: emb_line_sof_enable Bit[0]: mb_line_tag_enable
0x3219	EMB_LINE_TAG_DATA	0x55	RW	Bit[7:0]: emb_line tag data
0x321A	GRP_ACT	–	R	Indicate Which Group is Active
0x321B	GRP_HOLD_SRAM_TEST	0x00	RW	Bit[7:5]: Reserved Bit[4]: TEST_srm Bit[3:0]: sram_RM
0x321C	GRP_FRAME_CNT_GRP0	–	R	Indicate Frame Counter for Group 0
0x321D	GRP_FRAME_CNT_GRP1	–	R	Indicate Frame Counter for Group 1
0x321E	GRP_FRAME_CNT_GRP2	–	R	Indicate Frame Counter for Group 2
0x321F	GRP_FRAME_CNT_GRP3	–	R	Indicate Frame Counter for Group 3

6.6 analog control [0x3600 - 0x36F2]

table 6-6 analog control and system control registers

Address	register name	default value	R/W	description
0x3600~ 0x36F2	ANA_CTRL	–	–	Analog Control Registers

6.7 sensor timing control [0x3700 - 0x37FF]

table 6-7 sensor timing control registers

address	register name	default value	R/W	description
0x3700~ 0x37FF	SNR CTRL	–	–	Sensor Timing Control Registers

6.8 timing control [0x3800 - 0x381D, 0x3820 - 0x3828, 0x3833]

table 6-8 timing control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3800	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[11:8] Array horizontal start point
0x3801	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[7:0] Array horizontal start point
0x3802	Y ADDR START	0x00	RW	Bit[7:0]: y_addr_start[11:8] Array vertical start point
0x3803	Y ADDR START	0x00	RW	Bit[7:0]: y_addr_start[7:0] Array vertical start point
0x3804	X ADDR END	0xA0	RW	Bit[7:0]: x_addr_end[11:8] Array horizontal end point
0x3805	X ADDR END	0x8F	RW	Bit[7:0]: x_addr_end[7:0] Array horizontal end point
0x3806	Y ADDR END	0x50	RW	Bit[7:0]: y_addr_end[11:8] Array vertical end point

table 6-8 timing control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3807	Y ADDR END	0xFF	RW	Bit[7:0]: y_addr_end[7:0] Array vertical end point
0x3808	X OUTPUT SIZE	0xA0	RW	Bit[7:0]: x_output_size[11:8] ISP horizontal output width
0x3809	X OUTPUT SIZE	0x80	RW	Bit[7:0]: x_output_size[7:0] ISP horizontal output width
0x380A	Y OUTPUT SIZE	0x50	RW	Bit[7:0]: y_output_size[11:8] ISP vertical output height
0x380B	Y OUTPUT SIZE	0xF0	RW	Bit[7:0]: y_output_size[7:0] ISP vertical output height
0x380C	HTS	0x04	RW	Bit[7:0]: HTS[15:8] Total horizontal timing size
0x380D	HTS	0x4C	RW	Bit[7:0]: HTS[7:0] Total horizontal timing size
0x380E	VTS	0x06	RW	Bit[7:0]: VTS[15:8] Total vertical timing size[15:8]
0x380F	VTS	0x30	RW	Bit[7:0]: VTS[7:0] Total vertical timing size
0x3810	ISP X WIN	0x00	RW	Bit[7:0]: isp_x_win[15:8] ISP horizontal windowing offset
0x3811	ISP X WIN	0x08	RW	Bit[7:0]: isp_x_win[7:0] ISP horizontal windowing offset
0x3812	ISP Y WIN	0x00	RW	Bit[7:0]: isp_y_win[11:8] ISP vertical windowing offset
0x3813	ISP Y WIN	0x08	RW	Bit[7:0]: isp_y_win[7:0] ISP vertical windowing offset
0x3814	X INC ODD	0x01	RW	Bit[7:5]: Not used Bit[4:0]: x_odd_inc
0x3815	X INC EVEN	0x01	RW	Bit[7:4]: Not used Bit[4:0]: x_even_inc
0x3816	Y_INC_ODD	0x01	RW	Bit[7:5]: Not used Bit[4:0]: y_odd_inc
0x3817	Y_INC_EVEN	0x01	RW	Bit[7:5]: Not used Bit[4:0]: y_even_inc
0x3818	VSYNC START	0x00	RW	Bit[7:0]: vsync_start[15:8] VSYNC start point
0x3819	VSYNC START	0x00	RW	Bit[7:0]: vsync_start[7:0] VSYNC start point

table 6-8 timing control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x381A	VSYNC END	0x00	RW	Bit[7:0]: vsync_end[15:8] VSYNC end point
0x381B	VSYNC END	0x01	RW	Bit[7:0]: vsync_end[7:0] VSYNC end point
0x381C	BLC_NUM_OPTION	0x0E	RW	Bit[7:5]: ablc_adj Bit[4:0]: ablc_use_num [5:1]
0x381D	BLC_OPTION	0x40	RW	Bit[7]: Reserved Bit[6]: r_tc_sof_dly Bit[5]: r_man_blc_num_sel Bit[4:0]: r_man_blc_num[5:1] r_man_blc_num[0] = 1'b0
0x3820	FORMAT1	0x80	RW	Bit[7:6]: Reserved Bit[5]: vflip_blc_o 0: Always 0 1: vflip_blc_o = vflip_o Bit[4]: vflip_o Bit[3]: hmirror_o Bit[2]: hbin4_o Bit[1]: hbin2_o Bit[0]: vbinf_o
0x3821	FORMAT2	0x00	RW	Bit[7:3]: Reserved Bit[2]: r_new_stg_hdr_en Bit[1]: hdr_en_o Bit[0]: vsub48_blc
0x3822	TC_CTRL 22	0x04	RW	Bit[7:6]: Reserved Bit[5]: r_fix_cnt_en Bit[4]: vts_add_dis Bit[3:0]: r_grp_adj
0x3823	TC_CTRL 23	0x08	RW	Bit[7]: ext_vs_re Bit[6]: ext_vs_en Bit[5]: vts_no_latch Bit[4]: init_man Bit[3:0]: r_grp_adj
0x3824	CS RST FSIN	0x00	RW	Bit[7:0]: cs_rst_fsin[15:8] CS reset value high byte at vs_ext
0x3825	CS RST FSIN	0x20	RW	Bit[7:0]: cs_rst_fsin[7:0] CS reset value low byte at vs_ext
0x3826	R RST FSIN	0x00	RW	Bit[7:0]: r_rst_fsin[15:8] R reset value high byte at vs_ext
0x3827	R RST FSIN	0x08	RW	Bit[7:0]: r_rst_fsin[7:0] R reset value low byte at vs_ext

table 6-8 timing control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3828	TC_CTRL 28	0x38	RW	Bit[7]: Reserved Bit[6:0]: r_ablc_num_o
0x3833	TC_CTRL 33	0x05	RW	Bit[7:3]: Reserved Bit[2]: r_stg_grphold_nomask Bit[1]: r_stg_sleep_nomask Bit[0]: r_stg_hdr_grp_wr_opt

6.9 sensor control [0x3700 - 0x37FF]

table 6-9 sensor control registers

address	register name	default value	R/W	description
0x3700~ 0x37FF	SNR CTRL	–	–	Sensor Timing Control Registers

6.10 column ADC sync and sync FIFO control [0x4500 - 0x4502, 0x4507]

table 6-10 column ADC sync and sync FIFO control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4500	SYNC_FIFO00	0x22	RW	Bit[7:6]: rblue_option Bit[3:0]: r_sync_fifo_sram_tst
0x4501	SYNC_FIFO01	0x00	RW	Bit[7]: r_skip_man_ctl Bit[6]: rd_mem_ah Bit[5:4]: r_hbin4_opt 00: Average of 4 pixels 01: Summary of 4 pixels 10: Select first bin2 pixel 11: Select last bin2 pixel Bit[3:2]: r_hbin2_opt 00: Average 01: Summary 10: Select first pixel 11: Select last pixel Bit[1]: r_dat_swap Bit[0]: r_srclk_inv

table 6-10 column ADC sync and sync FIFO control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4502	SYNC_FIFO02	0x00	RW	Bit[7:0]: r_data_offset
0x4507	SYNC_FIFO07	0x64	RW	Bit[7]: r_sync_ln_cnt_rst_en Bit[6]: r_waddr_dummy_en Bit[5]: r_sof_reset_en Bit[4]: r_new_stg_hdr_en Bit[3]: r_clip_opt Bit[2]: r_dig_gray2bin_en Bit[1]: r_dummy_line_en Bit[0]: r_stg_hdr_en

6.11 BLC control [0x4000 - 0x4017, 0x4020 - 0x4027, 0x4030 - 0x40BA]

table 6-11 BLC control registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x4000	BLC00	0xF3	RW	Bit[7]: blk_en Bit[6]: out_range_one_ch_eco Bit[5]: gain_trig_priority Bit[4]: rst_trig_opt Bit[3]: target_adj_dis Bit[2]: cmp_en Bit[1]: dither_en Bit[0]: mf_en
0x4001	BLC01	0x60	RW	Bit[7]: Reserved Bit[6]: dcblc_en Bit[5]: kcoef_man_en Bit[4]: off_man_en Bit[3]: zero_ln_out_en Bit[2]: blk_ln_out_en Bit[1:0]: byp_mode
0x4001	BLC01	0x60	RW	Bit[7]: Reserved Bit[6]: dcblc_en Bit[5]: kcoef_man_en Bit[4]: off_man_en Bit[3]: zero_ln_out_en Bit[2]: blk_ln_out_en Bit[1:0]: byp_mode
0x4002	BLC02	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: blk_lvl_target[9:8]
0x4003	BLC03	0x40	RW	Bit[7:0]: blk_lvl_target[7:0]

table 6-11 BLC control registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x4004	BLC04	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: hwin_off[11:8]
0x4005	BLC05	0x08	RW	Bit[7:0]: hwin_off[7:0]
0x4006	BLC06	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: hwin_pad[11:8]
0x4007	BLC07	0x08	RW	Bit[7:0]: hwin_pad[7:0]
0x4008	BLC08	0x00	RW	bl_start
0x4009	BLC09	0x0D	RW	bl_end
0x400A	BLC0A	0x02	RW	Bit[7:0]: off_lim_th[15:8]
0x400B	BLC0B	0x00	RW	Bit[7:0]: off_lim_th[7:0]
0x400C	BLC0C	0x00	RW	cvdn_bl_start
0x400D	BLC0D	0x00	RW	cvdn_bl_end
0x400E	BLC0E	0x00	RW	mf_th
0x400F	BLC0F	0x80	RW	Bit[7]: r_exp_chg_trig_en Bit[6]: r_set_zb Bit[5:4]: r_manu_cvdn_out_en Bit[3]: r_v15_one_channel Bit[2]: r_en_adp_k Bit[1]: r_dc_offset_mode Bit[0]: r_compute_offset_v15
0x4010	BLC10	0xF0	RW	Bit[7]: off_trig_en Bit[6]: gain_chg_trig_en Bit[5]: fmt_chg_trig_en Bit[4]: rst_trig_en Bit[3]: man_avg_en Bit[2]: man_trig Bit[1]: off_frz_en Bit[0]: off_always_up
0x4011	BLC11	0xFF	RW	Bit[7]: r_off_cmp_man_en Bit[6]: off_chg_mf_en Bit[5]: fmt_chg_mf_en Bit[4]: gain_chg_mf_en Bit[3]: rst_mf_mode Bit[2]: off_chg_mf_mode Bit[1]: fmt_chg_mf_mode Bit[0]: gain_chg_mf_mode
0x4012	BLC12	0x08	RW	Bit[7:0]: rst_trig_fn[7:0]
0x4013	BLC13	0x02	RW	Bit[7:0]: fmt_trig_fn[7:0]
0x4014	BLC14	0x02	RW	Bit[7:0]: gain_trig_fn[7:0]

table 6-11 BLC control registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x4015	BLC15	0x02	RW	Bit[7:0]: off_trig_fn[7:0]
0x4016	BLC16	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: off_trig_th[9:8]
0x4017	BLC17	0x04	RW	Bit[7:0]: off_trig_th[7:0]
0x4020	BLC20	0x00	RW	off_cmp_th000
0x4021	BLC21	0x00	RW	off_cmp_k000
0x4022	BLC22	0x00	RW	off_cmp_th001
0x4023	BLC23	0x00	RW	off_cmp_k001
0x4024	BLC24	0x00	RW	off_cmp_th010
0x4025	BLC25	0x00	RW	off_cmp_k010
0x4026	BLC26	0x00	RW	off_cmp_th011
0x4027	BLC27	0x00	RW	off_cmp_k011
0x4030	BLC30	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: off_man000[9:8]
0x4031	BLC31	0x00	RW	Bit[7:0]: off_man000[7:0]
0x4032	BLC32	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: off_man001[9:8]
0x4033	BLC33	0x00	RW	Bit[7:0]: off_man001[7:0]
0x4034	BLC34	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: off_man010[9:8]
0x4035	BLC35	0x00	RW	Bit[7:0]: off_man010[7:0]
0x4036	BLC36	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: off_man011[9:8]
0x4037	BLC37	0x00	RW	Bit[7:0]: off_man011[7:0]
0x4038	BLC38	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: off_man100[9:8]
0x4039	BLC39	0x00	RW	Bit[7:0]: off_man100[7:0]
0x403A	BLC3A	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: off_man101[9:8]
0x403B	BLC3B	0x00	RW	Bit[7:0]: off_man101[7:0]
0x403C	BLC3C	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: off_man110[9:8]
0x403D	BLC3D	0x00	RW	Bit[7:0]: off_man110[7:0]

table 6-11 BLC control registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x403E	BLC3E	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: off_man111[9:8]
0x403F	BLC3F	0x00	RW	Bit[7:0]: off_man111[7:0]
0x4040	BLC40	0x00	RW	Bit[7:0]: zl_start
0x4041	BLC41	0x05	RW	Bit[7:0]: zl_end
0x4042	BLC42	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: kcoef_b_man[9:8]
0x4043	BLC43	0x80	RW	Bit[7:0]: kcoef_b_man[7:0]
0x4044	BLC44	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: kcoef_gb_man[9:8]
0x4045	BLC45	0x80	RW	Bit[7:0]: kcoef_gb_man[7:0]
0x4046	BLC46	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: kcoef_gr_man[9:8]
0x4047	BLC47	0x80	RW	Bit[7:0]: kcoef_gr_man[7:0]
0x4048	BLC48	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: kcoef_r_man[9:8]
0x4049	BLC49	0x80	RW	Bit[7:0]: kcoef_r_man[7:0]
0x404A	BLC4A	0x30	RW	r_dc_th_1
0x404B	BLC4B	0x18	RW	r_dc_th_2
0x404C	BLC4C	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: avg_weight
0x404D	BLC4D	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: rnd_gain_th [9:8]
0x404E	BLC4E	0x00	RW	Bit[7:0]: rnd_gain_th [7:0]
0x404F	BLC4F	0x00	RW	Bit[7:0]: r_dc_th_1_s
0x4050	BLC50	0x00	RW	Bit[7:0]: r_dc_th_2_s
0x4051~ 0x405F	NOT USED	–	–	Not Used
0x4060	BLC60	–	R	Bit[7:2]: Reserved Bit[1:0]: blc_offset000[9:8]
0x4061	BLC61	–	R	Bit[7:0]: blc_offset000[7:0]
0x4062	BLC62	–	R	Bit[7:2]: Reserved Bit[1:0]: blc_offset001[9:8]
0x4063	BLC63	–	R	Bit[7:0]: blc_offset001[7:0]

table 6-11 BLC control registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x4064	BLC64	–	R	Bit[7:2]: Reserved Bit[1:0]: blc_offset010[9:8]
0x4065	BLC65	–	R	Bit[7:0]: blc_offset010[7:0]
0x4066	BLC66	–	R	Bit[7:2]: Reserved Bit[1:0]: blc_offset011[9:8]
0x4067	BLC67	–	R	Bit[7:0]: blc_offset011[7:0]
0x4068	BLC68	–	R	Bit[7:2]: Reserved Bit[1:0]: blc_offset100[9:8]
0x4069	BLC69	–	R	Bit[7:0]: blc_offset100[7:0]
0x406A	BLC6A	–	R	Bit[7:2]: Reserved Bit[1:0]: blc_offset101[9:8]
0x406B	BLC6B	–	R	Bit[7:0]: blc_offset101[7:0]
0x406C	BLC6C	–	R	Bit[7:2]: Reserved Bit[1:0]: blc_offset110[9:8]
0x406D	BLC6D	–	R	Bit[7:0]: blc_offset110[7:0]
0x406E	BLC6E	–	R	Bit[7:2]: Reserved Bit[1:0]: blc_offset111[9:8]
0x406F	BLC6F	–	R	Bit[7:0]: blc_offset111[7:0]
0x4070	BLC70	–	R	Bit[7:0]: off_cmp_k_00[7:0]
0x4071	BLC71	–	R	Bit[7:0]: off_cmp_k_01[7:0]
0x4072	BLC72	–	R	Bit[7:0]: off_cmp_k_10[7:0]
0x4073	BLC73	–	R	Bit[7:0]: off_cmp_k_11[7:0]
0x4074	BLC74	–	R	Bit[7:2]: Reserved Bit[1:0]: Long ana_real_gain[9:8]
0x4075	BLC75	–	R	Bit[7:0]: Long ana_real_gain[7:0]
0x4076	BLC76	–	R	Bit[7:2]: Reserved Bit[1:0]: Short ana_real_gain[9:8]
0x4077	BLC77	–	R	Bit[7:0]: Short ana_real_gain[7:0]
0x4078~ 0x407F	NOT USED	–	–	Not Used
0x4080	BLC80	–	R	Bit[7:3]: Reserved Bit[2:0]: cmp_00[10:8]
0x4081	BLC	–	R	Bit[7:0]: cmp_00[7:0]

table 6-11 BLC control registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x4082	BLC	–	R	Bit[7:3]: Reserved Bit[2:0]: cmp_01[10:8]
0x4083	BLC	–	R	Bit[7:0]: cmp_01[7:0]
0x4084	BLC	–	R	Bit[7:3]: Reserved Bit[2:0]: cmp_10[10:8]
0x4085	BLC	–	R	Bit[7:0]: cmp_10[7:0]
0x4086	BLC	–	R	Bit[7:3]: Reserved Bit[2:0]: cmp_11[10:8]
0x4087	BLC	–	R	Bit[7:0]: cmp_11[7:0]
0x4088	BLC	–	R	Bit[7:3]: Reserved Bit[2:0]: kcoef_b[9:8]
0x4089	BLC	–	R	Bit[7:0]: kcoef_b[7:0]
0x408A	BLC	–	R	Bit[7:3]: Reserved Bit[2:0]: kcoef_gb[9:8]
0x408B	BLC	–	R	Bit[7:0]: kcoef_gb[7:0]
0x408C	BLC	–	R	Bit[7:3]: Reserved Bit[2:0]: kcoef_gr[9:8]
0x408D	BLC	–	R	Bit[7:0]: kcoef_gr[7:0]
0x408E	BLC	–	R	Bit[7:3]: Reserved Bit[2:0]: kcoef_r[9:8]
0x408F	BLC	–	R	Bit[7:0]: kcoef_r[7:0]
0x4090	BLC	0x14	RW	Bit[7]: cmp_flip_auto_old_en Bit[6]: kcoef_flip_auto_old_en Bit[5]: of_read_prec_sel Bit[4]: data_width_mode Bit[3]: cvdnblc_en Bit[2]: hdr_mode Bit[1]: format_trig_beh Bit[0]: gain_trig_beh
0x4091	BLC	0x00	RW	Bit[7]: cmp_mirror_man Bit[6]: cmp_mirror_man_en Bit[5]: cmp_flip_man Bit[4]: cmp_flip_man_en Bit[3]: kcoef_mirror_man Bit[2]: kcoef_mirror_man_en Bit[1]: kcoef_flip_man Bit[0]: kcoef_flip_man_en

table 6-11 BLC control registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x4092	BLC	0x00	RW	Bit[7:2]: Reserved Bit[1]: off_man_mirror_man_en Bit[0]: off_man_mirror_man
0x4093~ 0x409F	NOT USED	–	–	Not Used
0x40A0	BLC	–	R	Bit[7:3]: Reserved Bit[2:0]: cmp_00_s_i[10:8]
0x40A1	BLC	–	R	Bit[7:0]: cmp_00_s_i[7:0]
0x40A2	BLC	–	R	Bit[7:3]: Reserved Bit[2:0]: cmp_01_s_i[10:8]
0x40A3	BLC	–	R	Bit[7:0]: cmp_01_s_i[7:0]
0x40A4	BLC	–	R	Bit[7:3]: Reserved Bit[2:0]: cmp_10_s_i[10:8]
0x40A5	BLC	–	R	Bit[7:0]: cmp_10_s_i[7:0]
0x40A6	BLC	–	R	Bit[7:3]: Reserved Bit[2:0]: cmp_11_s_i[10:8]
0x40A7	BLC	–	R	Bit[7:0]: cmp_11_s_i[7:0]
0x40A8~ 0x40AF	NOT USED	–	–	Not Used
0x40B0	BLC	0x00	RW	Bit[7:1]: Reserved Bit[0]: thres_en_o
0x40B1	BLC	0x00	RW	Bit[7:5]: Reserved Bit[4]: hist_win_dis_o Bit[3:2]: Reserved Bit[1:0]: thres_stepfine_o
0x40B2	BLC	0x00	RW	thres_delta_o
0x40B3	BLC	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: thres_hist_cutoff[11:8]
0x40B4	BLC	0x00	RW	Bit[7:0]: thres_hist_cutoff[7:0]
0x40B5	BLC	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: thres_delta_cutoff
0x40B6	BLC	0x00	RW	Bit[7:1]: Reserved Bit[0]: thres_man_en
0x40B7	BLC	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: thres_man[11:8]
0x40B8	BLC	0x00	RW	Bit[7:0]: thres_man[7:0]

table 6-11 BLC control registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x40B9	BLC	0x00	RW	blc_hist_start
0x40BA	BLC	0x00	RW	Bit[7:3]: Reserved Bit[2]: gate_data_en Bit[1]: gate_clk_en Bit[0]: dummy_out_en

6.12 MIPI control [0x4800, 0x4802 - 0x4839, 0x483C - 0x488B]

table 6-12 MIPI control registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x4800	MIPI_CORE_0	0x04	RW	Bit[7]: Select sc_valid Bit[6]: Enable vertical clock gating Bit[5]: Enable clock gating Bit[4]: Enable line sync Bit[3]: Reserved Bit[2]: Invert output PCLK Bit[1]: First bit is 1 Bit[0]: Select manual parameter or auto parameter
0x4802	MIPI_CORE_2	0x00	RW	Bit[7]: hs_prepare_man_o Bit[6]: clk_prepare_man_o Bit[5]: clk_post_sel_o Bit[4]: clk_trail_sel_o Bit[3]: hs_exit_sel_o Bit[2]: hs_zero_sel_o Bit[1]: hs_trail_sel_o Bit[0]: clk_zero_sel_o
0x4803	MIPI_CORE_3	0x10	RW	Bit[7]: High speed mode only enable Bit[6]: PRBS test enable Bit[5]: prbs_rp_ph_en 1: PRBS pattern replace packet header Bit[4]: FIFO read speed Bit[3:0]: Reserved
0x4804	MIPI_CORE_4	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: Select height for each virtual channel
0x4805	MIPI_CORE_5	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Retiming

table 6-12 MIPI control registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x4806	MIPI_CORE_6	0x00	RW	Bit[7:5]: Reserved Bit[4]: Enable power up mark Bit[3]: Remote reset Bit[2]: Suspend Bit[1]: Enable SMIA lane Bit[0]: Output TXLSB first
0x4807	MIPI_CORE_7	0x03	RW	Bit[7:4]: Reserved Bit[3:0]: Ultra low power mode state delay[3:0]
0x4808	MIPI_CORE_8	0x18	RW	Bit[7:0]: Wakeup delay[7:0]
0x4809-0x480D	RSVD	–	–	Reserved
0x480E	MIPI_CORE_E	0x00	RW	Bit[7:4]: Reserved Bit[3]: Enable data type2 Bit[2]: Enable img2 Bit[1:0]: Reserved
0x480F	MIPI_CORE_F	0x00	RW	Bit[7:0]: hcnt_end_man_o[15:8]
0x4810	MIPI_CORE_10	0xFF	RW	Bit[7:0]: Max frame count value[15:8]
0x4811	MIPI_CORE_11	0xFF	RW	Bit[7:0]: Max frame count value[7:0]
0x4812	RSVD	–	–	Reserved
0x4813	MIPI_CORE_13	0x00	RW	Bit[7:6]: Virtual channel ID Bit[5:4]: Virtual channel ID Bit[3:2]: Virtual channel ID Bit[1:0]: Virtual channel ID
0x4814	MIPI_CORE_14	0x2A	RW	Bit[7]: Reserved Bit[6]: Data type select Bit[5:0]: Data type[5:0]
0x4815	MIPI_CORE_15	0x2B	RW	Bit[7:6]: Reserved Bit[5:0]: Datatype[5:0]
0x4816	MIPI_CORE_16	0x2B	RW	Bit[7:6]: Reserved Bit[5:0]: Data type[5:0]
0x4817	NOT USED	–	–	Not Used
0x4818	MIPI_CORE_18	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: MIPI parameter value[9:8] hs_zero_min_o
0x4819	MIPI_CORE_19	0x70	RW	Bit[7:0]: MIPI parameter value[7:0] hs_zero_min_o
0x481A	MIPI_CORE_1A	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: MIPI parameter value[9:8] hs_trail_min_o

table 6-12 MIPI control registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x481B	MIPI_CORE_1B	0x3C	RW	Bit[7:0]: MIPI parameter value[7:0] hs_trail_min_o
0x481C	MIPI_CORE_1C	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: MIPI parameter value[9:8] clk_zero_min_o
0x481D	MIPI_CORE_1D	0x2C	RW	Bit[7:0]: MIPI parameter value[7:0] clk_zero_min_o
0x481E	MIPI_CORE_1E	0x5F	RW	Bit[7:0]: MIPI parameter value[7:0] clk_prepare_max_o
0x481F	MIPI_CORE_1F	0x26	RW	Bit[7:0]: MIPI parameter value[7:0] clk_prepare_min_o
0x4820	MIPI_CORE_20	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: MIPI parameter value[9:8] clk_post_min_o
0x4821	MIPI_CORE_21	0x3C	RW	Bit[7:0]: MIPI parameter value[7:0] clk_post_min_o
0x4822	MIPI_CORE_22	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: MIPI parameter value[9:8] clk_trail_min_o
0x4823	MIPI_CORE_23	0x3C	RW	Bit[7:0]: MIPI parameter value[7:0] clk_trail_min_o
0x4824	MIPI_CORE_24	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: MIPI parameter value[9:8] lpx_p_min_o
0x4825	MIPI_CORE_25	0x32	RW	Bit[7:0]: MIPI parameter value[7:0] lpx_p_min_o
0x4826	MIPI_CORE_26	0x32	RW	Bit[7:0]: MIPI parameter value[7:0] hs_prepare_min_o
0x4827	MIPI_CORE_27	0x55	RW	Bit[7:0]: MIPI parameter value, [7:0]hs_prepare_max_o
0x4828	MIPI_CORE_28	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: MIPI parameter value[9:8] hs_exit_min_o
0x4829	MIPI_CORE_29	0x64	RW	Bit[7:0]: MIPI parameter value[7:0] hs_exit_min_o
0x482A	MIPI_CORE_2A	0x06	RW	Bit[7:6]: Reserved Bit[5:0]: MIPI parameter value[5:0] ui_hs_zero_min_o

table 6-12 MIPI control registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x482B	MIPI_CORE_2B	0x04	RW	Bit[7:6]: Reserved Bit[5:0]: MIPI parameter value[5:0] ui_hs_trail_min_o
0x482C	MIPI_CORE_2C	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: MIPI parameter value[5:0] ui_clk_zero_min_o
0x482D	MIPI_CORE_2D	0x00	RW	Bit[7:4]: MIPI parameter value[3:0] ui_clk_prepare_max_o Bit[3:0]: MIPI parameter value[3:0] ui_clk_prepare_min_o
0x482E	MIPI_CORE_2E	0x34	RW	Bit[7:6]: Reserved Bit[5:0]: MIPI parameter value[5:0] ui_clk_post_min_o
0x482F	MIPI_CORE_2F	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: MIPI parameter value[5:0] ui_clk_trail_min_o
0x4830	MIPI_CORE_30	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: MIPI parameter value[5:0] ui_lpx_p_min_o
0x4831	MIPI_CORE_31	0x64	RW	Bit[7:4]: MIPI parameter value[3:0] ui_hs_prepare_max_o Bit[3:0]: MIPI parameter value[3:0] ui_hs_prepare_min_o
0x4832	MIPI_CORE_32	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: MIPI parameter value[5:0] ui_hs_exit_min_o
0x4833	MIPI_CORE_33	0x10	RW	Bit[7:6]: Reserved Bit[5:0]: Pkt FIFO ready mark[5:0]
0x4834~ 0x4836	NOT USED	–	–	Not Used
0x4837	MIPI_CORE_37	0x0E	RW	Bit[7:0]: MIPI PCLK period Should be changed when PCLK frequency changes[7:0]
0x4838	MIPI_CORE_38	0x00	RW	Bit[7]: Low power select for lane0 Bit[6]: Low power direction for lane0 Bit[5]: Lp p0 for lane0 Bit[4]: Lp n0 for lane0 Bit[3]: Low power select for lane1 Bit[2]: Low power direction for lane1 Bit[1]: Lp p0 for lane1 Bit[0]: Lp n0 for lane1

table 6-12 MIPI control registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x4839	MIPI_CORE_39	0x00	RW	Bit[7]: Low power select for lane2 Bit[6]: Low power direction for lane2 Bit[5]: Lp p0 for lane2 Bit[4]: Lp n0 for lane2 Bit[3]: Low power select for lane3 Bit[2]: Low power direction for lane3 Bit[1]: Lp p0 for lane3 Bit[0]: Lp n0 for lane0
0x483C	MIPI_CORE_3C	0x10	RW	Bit[7:0]: MIPI parameter value[7:0] t_clk_pre_o
0x483D	MIPI_CORE_3D	0x00	RW	Bit[7:4]: Reserved Bit[3]: Low power select for clock lane Bit[2]: Reserved Bit[1]: Lp clock lane p Bit[0]: Lp clock lane n
0x483E	MIPI_CORE_3E	–	R	Bit[7:0]: Frame count value[15:8]
0x483F	MIPI_CORE_3F	–	R	Bit[7:0]: Frame count value[7:0]
0x4840~ 0x4849	NOT USED	–	–	Not Used
0x484A	MIPI_CORE_4A	0x3F	RW	Bit[7:6]: Reserved Bit[5]: Sleep power down select Bit[4]: lp_pon data Bit[3]: lp_pon clock lane data Bit[2]: Manual sleep state Bit[1]: Clock lane sleep state Bit[0]: Data lane sleep state
0x484B	MIPI_CORE_4B	0x07	RW	Bit[7]: Reserved Bit[6]: pa_cal_1time 0: Global timing calculation every frame 1: Global timing calculation only at wakeup Bit[5]: EOF select Bit[4]: Virtual channel select Bit[3]: Data scramble enable Bit[2]: EOF busy select Bit[1]: Clock start select Bit[0]: SOF select
0x484C	MIPI_CORE_4C	0x00	RW	Bit[7:1]: Reserved Bit[0]: Disable frame count
0x484E	MIPI_CORE_4E	0x10	RW	Bit[7:0]: Frame end delay
0x484F	NOT USED	–	–	Not Used

table 6-12 MIPI control registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x4850	MIPI_CORE_50	0x40	RW	Bit[7]: Reserved Bit[6]: DPHY1.2 frame blank select 0: Skew end 1: Frame end Bit[5]: Deskew output enable Bit[4]: Frame deskew disable Bit[3]: Initial deskew disable Bit[2]: Deskew tradata Bit[1]: Perform deskew one lane at a time Bit[0]: DPHY1, 2 enable
0x4851	MIPI_CORE_51	0xAA	RW	Bit[7:0]: Deskew data[7:0]
0x4852	MIPI_CORE_52	0xFF	RW	Bit[7:0]: Deskew sync data[7:0]
0x4853	MIPI_CORE_53	0x8A	RW	Bit[7:0]: Deskew start delay[7:0]
0x4854	MIPI_CORE_54	0x08	RW	Bit[7:0]: Frame deskew width[7:0]
0x4855	MIPI_CORE_55	0x30	RW	Bit[7:0]: Initial deskew width[7:0]
0x4856	MIPI_CORE_56	0x01	RW	Bit[7:0]: Frame deskew interval[7:0]
0x4857~ 0x485F	NOT USED	–	–	Not Used
0x4860	MIPI_CORE_60	0x00	RW	Bit[7:6]: CPHY disable[1:0] Bit[5:1]: Reserved Bit[0]: CPHY enable
0x4861	MIPI_CORE_61	0xA0	RW	Bit[7]: CPHY escape flag Bit[6]: CPHY escape flag Bit[5]: CPHY trdata Bit[4]: Select CPHY CRC head 1: Low byte first Bit[3:0]: Reserved
0x4862	MIPI_CORE_62	0x01	RW	Bit[7:0]: CPHY parameter[7:0]
0x4863	MIPI_CORE_63	0x01	RW	Bit[7:0]: CPHY parameter[7:0]
0x4864	MIPI_CORE_64	0x02	RW	Bit[7:0]: CPHY programmable sequence[7:0]
0x4865	MIPI_CORE_65	0x66	RW	Bit[7:0]: CPHY programmable data1[7:0]
0x4866	MIPI_CORE_66	0x99	RW	Bit[7:0]: CPHY programmable data2[7:0]
0x4867	MIPI_CORE_67	0x88	RW	Bit[7:0]: CPHY programmable data3[7:0]
0x4868	MIPI_CORE_68	0xAA	RW	Bit[7:0]: CPHY programmable data4[7:0]
0x4869	MIPI_CORE_69	0xFF	RW	Bit[7:0]: CPHY preamble data1[7:0]
0x486A	MIPI_CORE_6A	0x3F	RW	Bit[7:0]: CPHY preamble data2[7:0]
0x486B	MIPI_CORE_6B	0x84	RW	Bit[7:0]: CPHY sync data1[7:0]

table 6-12 MIPI control registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x486C	MIPI_CORE_6C	0x36	RW	Bit[7:0]: CPHY sync data2[7:0]
0x486D	MIPI_CORE_6D	0x00	RW	Bit[7:0]: Reverse data for CPHY[7:0]
0x486E	MIPI_CORE_6E	0x84	RW	Bit[7:0]: CPHY escape data1[7:0]
0x486F	MIPI_CORE_6F	0x36	RW	Bit[7:0]: CPHY escape data2[7:0]
0x4870~ 0x487F	RSVD	–	–	Reserved
0x4880	MIPI_PHY_0	0x00	RW	Bit[7]: Enable pll2 debug output Bit[6]: Enable PCLK debug output Bit[5]: Reserved Bit[4:3]: CLK lane skew adjustment Bit[2]: Disable CLK lane Bit[1]: Test mode to force HS0 on clock/data lane Bit[0]: Enable PLL1 debug clock output
0x4881	MIPI_PHY_1	0x00	RW	Bit[7]: Reserved Bit[6:5]: Data lane0 skew adjustment Bit[4]: Disable data lane0 Bit[3]: Reserved Bit[2:1]: Data lane1 skew adjustment Bit[0]: Disable data lane1
0x4882	MIPI_PHY_2	0x00	RW	Bit[7]: Reserved Bit[6:5]: Data lane2 skew adjustment Bit[4]: Disable data lane2 Bit[3]: Reserved Bit[2:1]: Data lane3 skew adjustment Bit[0]: Disable data lane3
0x4883	MIPI_PHY_3	0x00	RW	Bit[7]: pll2_dac clock to MIPI PHY enable Bit[6]: Reserved Bit[5:4]: Coarse tuning register for high speed output voltage Bit[3]: Reserved Bit[2:0]: Fine tuning register for high speed output voltage
0x4884	MIPI_PHY_4	0x08	RW	Bit[7:6]: Reserved Bit[5]: Bypass HS TX enable retiming Bit[4:3]: LP TX driving strength adjustment Bit[2:1]: Reserved Bit[0]: Enable MIPI self bias circuit
0x4885	MIPI_PHY_5	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: MIPI HS TX driving strength adjustment
0x4886	RSVD	–	–	Reserved

table 6-12 MIPI control registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x4887	MIPI_PHY_7	0x51	RW	Bit[7]: HS enable signal delay option Bit[6]: Select LPTX driver 0: Regulator mode 1: EVDD mode Bit[5]: MIPI D-PHY+ in-phase calibration 0: D-PHY 1.2 calibration mode 1: D-PHY+ in-phase calibration mode Bit[4]: De-emphasis mode selection 0: 7 dB 1: 3.5 dB Bit[3]: Enable de-emphasis function Bit[2:0]: De-emphasis amplitude adjustment
0x4888	MIPI_PHY_8	0x90	RW	Bit[7]: Manual control to enable/disable LP TX regulator pull up switch to EVDD Bit[6]: MIPI LP data reset option 0: LP data reset to 1 1: LP data reset to 0 Bit[5]: Option of open termination output mode Bit[4]: PHY mode control 0: C-PHY mode 1: D-PHY mode Bit[3]: Reserved Bit[2:0]: LP TX regulator output high voltage adjustment
0x4889	MIPI_PHY_9	0x03	RW	Bit[7]: Disable CPHY trio0 Bit[6]: Disable CPHY trio Bit[5]: Disable CPHY trio2 Bit[4]: Disable C-PHY TX termination in idle mode Bit[3]: Enable C-PHY debug mode Bit[2:0]: Set CPHY parallel to serial interface sampling point
0x488A	MIPI_PHY_A	0x00	RW	Bit[7:4]: MIPI internal BG adjustment control Bit[3]: Reserved Bit[2:0]: MIPI HS TX slew rate control
0x488B	MIPI_PHY_B	0x00	RW	Bit[7:5]: Reserved Bit[4]: mipi_data_valid_sel_o Bit[3:2]: bitsel_o Bit[1:0]: mipi_ck_slew_ctrl_o

6.13 ISPFC [0x4900 - 0x4903]

table 6-13 ISPFC registers

address	register name	default value	R/W	description
0x4900	FC_R0	0x08	RW	Bit[7:5]: Reserved Bit[4]: byp_fc Bit[3]: sof_after_lin0 Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fc_rst
0x4901	FC_R1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: rame_on_no[3:0]
0x4902	FC_R2	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: frame_off_no[3:0]
0x4903	FC_R3	0x80	RW	Bit[7]: zero_line_mask_dis Bit[6]: rblue_mask_dis Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

6.14 ISP control [0x5000 - 0x5021, 0x5026 - 0x5038, 0x5080 - 0x508F, 0x50A0 - 0x5AB]

table 6-14 ISP control registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x5000	ISP_CTRL_0	0xE9	RW	Bit[7]: WIN enable Bit[6]: Reserved Bit[5]: DPC enable Bit[4]: OTP enable Bit[3]: AWB_GAIN enable Bit[2:1]: Reserved Bit[0]: ISP enable

table 6-14 ISP control registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x5001	ISP_CTRL_1	0x09	RW	Bit[7:6]: Reserved Bit[5]: man_gain_enable Bit[4]: man_digigaion_enable Bit[3]: CTRL signal latch mode Bit[2:1]: Reserved Bit[0]: Rst_Prt enable
0x5002	ISP_CTRL_2	0x00	RW	Bit[7]: Manual flip Bit[6]: Manual mirror Bit[5]: Reserved Bit[4]: OTP enable Bit[3]: Flip manual mode Bit[2]: Mirror manual mode Bit[1:0]: Reserved
0x5003	ISP_CTRL_3	0x00	RW	Bit[7]: SOF select Bit[6]: EOF select Bit[5:4]: Manual CFA pattern Bit[3]: Exposure manual mode Bit[2]: Real gain manual mode Bit[1]: BLC manual mode Bit[0]: CFA pattern manual mode
0x5004	ISP_CTRL_4	0x00	RW	Bit[7:2]: Reserved Bit[1]: Image size manual mode Bit[0]: ISP module work manual mode
0x5005	RSVD	–	–	Reserved
0x5006	ISP_CTRL_6	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual real gain0[11:8]
0x5007	ISP_CTRL_7	0x10	RW	Bit[7:0]: Manual real gain0[7:0]
0x5008	ISP_CTRL_8	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual real gain1[11:8]
0x5009	ISP_CTRL_9	0x10	RW	Bit[7:0]: Manual real gain1[7:0]
0x500A	ISP_CTRL_A	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual BLC0[11:8]
0x500B	ISP_CTRL_B	0x10	RW	Bit[7:0]: Manual BLC0 [7:0]
0x500C	ISP_CTRL_C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual BLC1[11:8]
0x500D	ISP_CTRL_D	0x10	RW	Bit[7:0]: Manual BLC1 [7:0]
0x500E	ISP_CTRL_E	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual Expo0[19:16]
0x500F	ISP_CTRL_F	0x00	RW	Bit[7:0]: Manual Expo0[15:8]
0x5010	ISP_CTRL_10	0x10	RW	Bit[7:0]: Manual Expo0[7:0]

table 6-14 ISP control registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x5011	RSVD	–	–	Reserved
0x5012	ISP_CTRL_12	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Manual hsize[12:8]
0x5013	ISP_CTRL_13	0x80	RW	Bit[7:0]: Manual hsize[7:0]
0x5014	ISP_CTRL_14	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Manual vsize[11:8]
0x5015	ISP_CTRL_15	0xE0	RW	Bit[7:0]: Manual vsize[7:0]
0x5016	ISP_CTRL_16	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual expo1[19:16]
0x5017	ISP_CTRL_17	0x00	RW	Bit[7:0]: Manual expo1[15:8]
0x5018	ISP_CTRL_18	0x10	RW	Bit[7:0]: Manual expo1[7:0]
0x5019	ISP_CTRL_19	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Manual digital gain0[13:8]
0x501A	ISP_CTRL_1A	0x10	RW	Bit[7:0]: Manual digital gain0[7:0]
0x501B	ISP_CTRL_1B	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Manual digital gain1[13:8]
0x501C	ISP_CTRL_1C	0x10	RW	Bit[7:0]: Manual digital gain1[7:0]
0x501E	ISP_CTRL_1D	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual gain0[11:8]
0x501F	ISP_CTRL_1F	0x10	RW	Bit[7:0]: Manual gain0[7:0]
0x5020	ISP_CTRL_20	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual gain1[11:8]
0x5021	ISP_CTRL_21	0x10	RW	Bit[7:0]: Manual gain1[7:0]
0x5026	ISP_CTRL_26	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: man_pd_cycle_x_1_o
0x5027	ISP_CTRL_27	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: man_pd_cycle_y_1_o
0x5028	ISP_CTRL_28	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: man_pd_y_1_o
0x5029	ISP_CTRL_29	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: man_pd_x1_1_o
0x502A	ISP_CTRL_2A	0x0A	RW	Bit[7:5]: Reserved Bit[4:0]: man_pd_x2_1_o
0x502B	ISP_CTRL_2B	0x06	RW	Bit[7:5]: Reserved Bit[4:0]: man_pd_x3_1_o

table 6-14 ISP control registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x502C	ISP_CTRL_2C	0x0E	RW	Bit[7:5]: Reserved Bit[4:0]: man_pd_x4_1_o
0x502D	NOT USED	–	–	Not Used
0x502E	ISP_CTRL_2E	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: man_win_x_start_1_o[12:8]
0x502F	ISP_CTRL_2F	0x40	RW	Bit[7:0]: man_win_x_start_1_o[7:0]
0x5030	ISP_CTRL_30	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: man_win_y_start_1_o[11:8]
0x5031	ISP_CTRL_31	0x40	RW	Bit[7:0]: man_win_y_start_1_o[7:0]
0x5032	ISP_CTRL_32	0x0C	RW	Bit[7:5]: Reserved Bit[4:0]: man_pd_win_width_1_o[12:8]
0x5033	ISP_CTRL_33	0x80	RW	Bit[7:0]: man_pd_win_width_1_o[7:0]
0x5034	ISP_CTRL_34	0x0B	RW	Bit[7:4]: Reserved Bit[3:0]: man_pd_win_height_1_o[11:8]
0x5035	ISP_CTRL_35	0x40	RW	Bit[7:0]: man_pd_win_height_1_o[7:0]
0x5036	ISP_CTRL_36	0x00	RW	Bit[7]: Dis_ck_gt_win Bit[6]: Dis_ck_gt_dns Bit[5]: Dis_ck_gt_dpc Bit[4]: Reserved Bit[3]: Dis_ck_gt_otp Bit[2]: Dis_ck_gt_awbg Bit[1]: Reserved Bit[0]: Dis_ck_gt_top
0x5037	ISP_CTRL_37	0x00	RW	Bit[7:1]: Reserved Bit[0]: Dis_ck_gt_all
0x5038	ISP_CTRL_38	0x00	RW	Bit[7:6]: Reserved Bit[5:2]: Read margin input Bit[1]: Read margin enable Bit[0]: SramTest1

table 6-14 ISP control registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x5080	ISP_CTRL_80	0x40	RW	Bit[7]: Test enable 0: Disable 1: Enable Bit[6]: Rolling enable (rolling bar in test mode) 0: Disable 1: Enable Bit[5]: Transparent effect enable 0: Disable 1: Enable Bit[4]: Black/white or color square selection 0: Color 1: Black/white Bit[3:2]: Color bar style Bit[1:0]: Test mode select
0x5081	ISP_CTRL_81	0x01	RW	Bit[7]: Reserved Bit[6]: Window cut enable 0: Disable 1: Enable Bit[5]: ISP test Low bits to 0 Bit[4]: Random mode frame-fixed seed enable 0: Disable 1: Enable Bit[3:0]: Random seed
0x5082	ISP_CTRL_82	0x30	RW	Bit[7:6]: Reserved Bit[5]: Mirror option for X offset Bit[4]: Flip option for Y offset Bit[3]: Mirror order Bg or Gb Bit[2]: Flip order Br or Rb Bit[1]: Offset manual enable 0: Disable 1: Enable Bit[0]: Scale input size manual mode 0: Disable 1: Enable
0x5083	ISP_CTRL_83	0x0F	RW	Bit[7:0]: Long ratio fraction part
0x5084	ISP_CTRL_84	0x0F	RW	Bit[7:0]: Short ratio fraction part
0x5085	ISP_CTRL_85	0x00	RW	Bit[7:6]: Reserved Bit[5]: x_skip_man_en Bit[4:0]: x_skip_man

table 6-14 ISP control registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x5086	ISP_CTRL_86	0x00	RW	Bit[7:6]: Reserved Bit[5]: y_skip_man_en Bit[4:0]: y_skip_man
0x5087	RSVD	–	–	Reserved
0x5088	ISP_CTRL_88	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Line number interrupt[11:8]
0x5089	ISP_CTRL_89	0x01	RW	Bit[7:0]: Line number interrupt[7:0]
0x508A	ISP_CTRL_8A	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Line number interrupt[11:8]
0x508B	ISP_CTRL_8B	0x01	RW	Bit[7:0]: Line number interrupt[7:0]
0x508C	ISP_CTRL_8C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: X manual offset[11:8]
0x508D	ISP_CTRL_8D	0x00	RW	Bit[7:0]: X manual offset[7:0]
0x508E	ISP_CTRL_8E	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Y manual offset[11:8]
0x508F	ISP_CTRL_8F	0x00	RW	Bit[7:0]: Y manual offset[7:0]
0x50A0	ISP_CTRL_A0	–	R	Bit[7:5]: Reserved Bit[4:0]: X odd inc
0x50A1	ISP_CTRL_A1	–	R	Bit[7:5]: Reserved Bit[4:0]: Y odd inc
0x50A2	ISP_CTRL_A2	–	R	Bit[7:5]: Reserved Bit[4:0]: X even inc
0x50A3	ISP_CTRL_A3	–	R	Bit[7:5]: Reserved Bit[4:0]: Y even inc
0x50A4	ISP_CTRL_A4	–	R	Bit[7:4]: Reserved Bit[3:0]: X offset[11:8]
0x50A5	ISP_CTRL_A5	–	R	Bit[7:0]: X offset[7:0]
0x50A6	ISP_CTRL_A6	–	R	Bit[7:4]: Reserved Bit[3:0]: Y offset[11:8]
0x50A7	ISP_CTRL_A7	–	R	Bit[7:0]: Y offset[7:0]
0x50A8	ISP_CTRL_A8	–	R	Bit[7:4]: Reserved Bit[3:0]: Pixel number[11:8]
0x50A9	ISP_CTRL_A9	–	R	Bit[7:0]: Pixel number[7:0]
0x50AA	ISP_CTRL_AA	–	R	Bit[7:4]: Reserved Bit[3:0]: Line number[11:8]

table 6-14 ISP control registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x50AB	ISP_CTRL_AB	–	R	Bit[7:0]: Line number[7:0]

6.15 AWB gain [0x5100 - 0x510B, 0x5140 - 0x514B]

table 6-15 AWB gain registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5100	AWB_CTRL_0	0x40	RW	Bit[7:4]: Reserved Bit[3:0]: awb_gain_B[11:8]
0x5101	AWB_CTRL_1	0x00	RW	Bit[7:0]: awb_gain_B[7:0]
0x5102	AWB_CTRL_2	0x40	RW	Bit[7:4]: Reserved Bit[3:0]: awb_gain_G[11:8]
0x5103	AWB_CTRL_3	0x00	RW	Bit[7:0]: awb_gain_G[7:0]
0x5104	AWB_CTRL_4	0x40	RW	Bit[7:4]: Reserved Bit[3:0]: awb_gain_R[11:8]
0x5105	AWB_CTRL_5	0x00	RW	Bit[7:0]: awb_gain_R[7:0]
0x5106	AWB_CTRL_6	0x02	RW	Bit[7:6]: Reserved Bit[5:0]: Digigain[13:8]
0x5107	AWB_CTRL_7	0x00	RW	Bit[7:0]: Digigain[7:0]
0x5108	AWB_CTRL_8	0x00	RW	Bit[7:3]: Reserved Bit[2]: blc_man_en Bit[1]: digigain_man_en Bit[0]: cfaptn_man_en
0x5109	AWB_CTRL_9	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: cfa_ptn_man
0x510A	AWB_CTRL_A	0x20	RW	Bit[7:4]: Reserved Bit[3:0]: BLC[11:8]
0x510B	AWB_CTRL_B	0x00	RW	Bit[7:0]: BLC[7:0]
0x5140	AWB_CTRL_0S	0x40	RW	Bit[7:4]: Reserved Bit[3:0]: awb_gain_B[11:8]
0x5141	AWB_CTRL_1S	0x00	RW	Bit[7:0]: awb_gain_B[7:0]
0x5142	AWB_CTRL_2S	0x40	RW	Bit[7:4]: Reserved Bit[3:0]: awb_gain_G[11:8]
0x5143	AWB_CTRL_3S	0x00	RW	Bit[7:0]: awb_gain_G[7:0]

table 6-15 AWB gain registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5144	AWB_CTRL_4S	0x40	RW	Bit[7:4]: Reserved Bit[3:0]: awb_gain_R[11:8]
0x5145	AWB_CTRL_5S	0x00	RW	Bit[7:0]: awb_gain_R[7:0]
0x5146	AWB_CTRL_6S	0x02	RW	Bit[7:6]: Reserved Bit[5:0]: Digigain[13:8]
0x5147	AWB_CTRL_7S	0x00	RW	Bit[7:0]: Digigain[7:0]
0x5148	AWB_CTRL_8	0x00	RW	Bit[7:3]: Reserved Bit[2]: blc_man_en Bit[1]: digigain_man_en Bit[0]: cfaptn_man_en
0x5149	AWB_CTRL_9	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: cfa_ptn_man
0x514A	AWB_CTRL_A	0x20	RW	Bit[7:4]: Reserved Bit[3:0]: BLC[11:8]
0x514B	AWB_CTRL_B	0x00	RW	Bit[7:0]: BLC[7:0]

6.16 DPC [0x5200 - 0x521F, 0x5280 - 0x529F, 0x5800 - 0x5813]

table 6-16 DPC registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x5200	DPC_CTRL_0	0x1B	RW	Bit[7]: Enable tail Bit[6]: Enable tailing cluster Bit[5]: Enable 3x3 cluster Bit[4]: Enable saturate cross cluster Bit[3]: Enable cross cluster Bit[2]: Manual mode enable Bit[1]: Black pixel enable Bit[0]: White pixel enable
0x5201	DPC_CTRL_1	0x94	RW	Bit[7:6]: Vertical number list Bit[5:4]: Vertical number list Bit[3:2]: Vertical number list Bit[1]: Enable G clip Bit[0]: Enable share buffer
0x5202	DPC_CTRL_2	0x2E	RW	Bit[7:6]: Reserved Bit[5:4]: Bayer pattern order Bit[3:2]: Image boundary extend options Bit[1:0]: Vertical number list

table 6-16 DPC registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x5203	DPC_CTRL_3	0x24	RW	Bit[7]: Reserved Bit[6:3]: White pixel threshold list Bit[2:0]: Maximum vertical number
0x5204	DPC_CTRL_4	0x12	RW	Bit[7:4]: White pixel threshold list Bit[3:0]: White pixel threshold list
0x5205	DPC_CTRL_5	0x41	RW	Bit[7:4]: Dark pixel threshold ratio Bit[3:0]: White pixel threshold list
0x5206	DPC_CTRL_6	0x48	RW	Bit[7:4]: Status threshold Bit[3:0]: Cluster threshold
0x5207	DPC_CTRL_7	0x84	RW	Bit[7:4]: Pattern match threshold Bit[3:0]: Status threshold step
0x5208	DPC_CTRL_8	0x40	RW	Bit[7:4]: Adaptive pattern step Bit[3:0]: Adaptive pattern threshold
0x5209	DPC_CTRL_9	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Saturate pixel threshold for clusters
0x520A	DPC_CTRL_A	0x30	RW	Bit[7:0]: Gain pivot list Non-decreasing order
0x520B	DPC_CTRL_B	0xF0	RW	Bit[7:0]: Gain pivot list Non-decreasing order
0x520C	DPC_CTRL_C	0x3F	RW	Bit[7:0]: Gain pivot list Non-decreasing order
0x520D	DPC_CTRL_D	0xF0	RW	Bit[7:0]: DPC level list
0x520E	DPC_CTRL_E	0xFD	RW	Bit[7:0]: DPC level list
0x520F	DPC_CTRL_F	0xF5	RW	Bit[7:0]: DPC level list
0x5210	DPC_CTRL_10	0xF5	RW	Bit[7:0]: DPC level list
0x5211~ 0x5213	NOT USED	–	–	Not Used
0x5214	DPC_CTRL_14	0x00	RW	Bit[7]: Recover clock gate disable Bit[6]: Recover clock gate disable Bit[5]: Recover clock gate disable Bit[4]: SRAM clock gate disable Bit[3]: Buffer control clock gate disable Bit[2]: Start frame clock gate disable Bit[1]: Clock gate disable Bit[0]: Pixel order manual enable
0x5218	DPC_CTRL_18	–	R	Bit[7]: Reserved Bit[6:0]: Bthre

table 6-16 DPC registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x5219	DPC_CTRL_19	–	R	Bit[7:5]: Reserved Bit[4:0]: Wthre
0x521A	DPC_CTRL_1A	–	R	Bit[7:5]: Reserved Bit[4:0]: Thre1
0x521B	DPC_CTRL_1B	–	R	Bit[7:0]: Thre2
0x521C	DPC_CTRL_1C	–	R	Bit[7]: Reserved Bit[6:0]: Thre3
0x521D	DPC_CTRL_1D	–	R	Bit[7]: Reserved Bit[6:0]: Thre4
0x521E	DPC_CTRL_1E	–	R	Bit[7:4]: Level Bit[3:0]: Pconnected
0x521F	DPC_CTRL_1F	–	R	Bit[7:3]: Reserved Bit[2:0]: Vnum
0x5280	DPC_CTRL_0S	0x1B	RW	Bit[7]: Enable tail Bit[6]: Enable tailing cluster Bit[5]: Enable 3x3 cluster Bit[4]: Enable saturate cross cluster Bit[3]: Enable cross cluster Bit[2]: Manual mode enable Bit[1]: Black pixel enable Bit[0]: White pixel enable
0x5281	DPC_CTRL_1S	0x94	RW	Bit[7:6]: Vertical number list Bit[5:4]: Vertical number list Bit[3:2]: Vertical number list Bit[1]: Enable G clip Bit[0]: Enable share buffer
0x5282	DPC_CTRL_2S	0x2E	RW	Bit[7:6]: Reserved Bit[5:4]: Bayer pattern order Bit[3:2]: Image boundary extend options Bit[1:0]: Vertical number list
0x5283	DPC_CTRL_3S	0x24	RW	Bit[7]: Reserved Bit[6:3]: White pixel threshold list Bit[2:0]: Maximum vertical number
0x5284	DPC_CTRL_4S	0x12	RW	Bit[7:4]: White pixel threshold list Bit[3:0]: White pixel threshold list
0x5285	DPC_CTRL_5S	0x41	RW	Bit[7:4]: Dark pixel threshold ratio Bit[3:0]: White pixel threshold list
0x5286	DPC_CTRL_6S	0x48	RW	Bit[7:4]: Status threshold Bit[3:0]: Cluster threshold

table 6-16 DPC registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x5287	DPC_CTRL_7S	0x84	RW	Bit[7:4]: Pattern match threshold Bit[3:0]: Status threshold step
0x5288	DPC_CTRL_8S	0x40	RW	Bit[7:4]: Adaptive pattern step Bit[3:0]: Adaptive pattern threshold
0x5289	DPC_CTRL_9S	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Saturate pixel threshold for clusters
0x528A	DPC_CTRL_AS	0x30	RW	Bit[7:0]: Gain pivot list Non-decreasing order
0x528B	DPC_CTRL_BS	0xF0	RW	Bit[7:0]: Gain pivot list Non-decreasing order
0x528C	DPC_CTRL_CS	0x3F	RW	Bit[7:0]: Gain pivot list Non-decreasing order
0x528D	DPC_CTRL_DS	0xF0	RW	Bit[7:0]: DPC level list
0x528E	DPC_CTRL_ES	0xFD	RW	Bit[7:0]: DPC level list
0x528F	DPC_CTRL_FS	0xF5	RW	Bit[7:0]: DPC level list
0x5290	DPC_CTRL_10S	0xF5	RW	Bit[7:0]: DPC level list
0x5291~ 0x5293	NOT USED	–	–	Not Used
0x5294	DPC_CTRL_14S	0x00	RW	Bit[7]: Recover clock gate disable Bit[6]: Recover clock gate disable Bit[5]: Recover clock gate disable Bit[4]: SRAM clock gate disable Bit[3]: Buffer control clock gate disable Bit[2]: Start frame clock gate disable Bit[1]: Clock gate disable Bit[0]: Pixel order manual enable
0x5295~ 0x5297	NOT USED	–	–	Not Used
0x5298	DPC_CTRL_18S	–	R	Bit[7]: Reserved Bit[6:0]: Bthre
0x5299	DPC_CTRL_19S	–	R	Bit[7:5]: Reserved Bit[4:0]: Wthre
0x529A	DPC_CTRL_1AS	–	R	Bit[7:5]: Reserved Bit[4:0]: Thre1
0x529B	DPC_CTRL_1BS	–	R	Bit[7:0]: Thre2
0x529C	DPC_CTRL_1CS	–	R	Bit[7]: Reserved Bit[6:0]: Thre3

table 6-16 DPC registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x529D	DPC_CTRL_1DS	–	R	Bit[7]: Reserved Bit[6:0]: Thre4
0x529E	DPC_CTRL_1ES	–	R	Bit[7:4]: Level Bit[3:0]: Pconnected
0x529F	DPC_CTRL_1FS	–	R	Bit[7:3]: Reserved Bit[2:0]: Vnum
0x5800	ISP_CTRL_0	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Window X start[11:8]
0x5801	ISP_CTRL_1	0x00	RW	Bit[7:0]: Window X start[7:0]
0x5802	ISP_CTRL_2	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Window Y start[11:8]
0x5803	ISP_CTRL_3	0x00	RW	Bit[7:0]: Window Y start[7:0]
0x5804	ISP_CTRL_4	0x20	RW	Bit[7:4]: Reserved Bit[3:0]: Window width[11:8]
0x5805	ISP_CTRL_5	0x80	RW	Bit[7:0]: Window width[7:0]
0x5806	ISP_CTRL_6	0x10	RW	Bit[7:4]: Reserved Bit[3:0]: Window height[11:8]
0x5807	ISP_CTRL_7	0xE0	RW	Bit[7:0]: Window height[7:0]
0x5808	ISP_CTRL_8	0x00	RW	Bit[7:3]: emb_num Bit[2]: emb_flag_sel 0: Start line 1: End line Bit[1]: Reserved Bit[0]: win_man_en 0: Window size from window top 1: Window size from register
0x5809	ISP_CTRL_9	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Window height extent line number
0x580A	ISP_CTRL_10	0x00	RW	Bit[7:0]: Minus Y offset
0x580B	ISP_CTRL_11	0x0F	RW	Bit[7:4]: Reserved Bit[3]: r_mirror_en Bit[2]: r_flip_en Bit[1]: r_hwin_en Bit[0]: r_vwin_en
0x580C~ 0x580F	NOT USED	–	–	Not Used
0x5810	ISP_CTRL_16	–	R	Bit[7:4]: Reserved Bit[3:0]: Pixel count[11:8]

table 6-16 DPC registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x5811	ISP_CTRL_17	–	R	Bit[7:0]: Pixel count[7:0]
0x5812	ISP_CTRL_18	–	R	Bit[7:4]: Reserved Bit[3:0]: Line count[11:8]
0x5813	ISP_CTRL_19	–	R	Bit[7:0]: Line count[7:0]

6.17 PSV control [0x3C80 - 0x3C8A, 0x3C8C - 0x3C8D, 0x3C90 - 0x3CAE]

table 6-17 PSV control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3C80	PSV_CTRL0	0x10	RW	Bit[7:4]: Reserved Bit[3]: psv_auto_on_dis 0: PSV mode auto enable if VTS > threshold 1: Disable PSV auto-on mode, only depend on psv_mode_en Bit[2]: psv_mode_en Bit[1]: Reserved Bit[0]: psv_mode 0: Keep SCLK on Frame timing based on SCLK 1: Shut off SCLK at blanking Frame timing switch to pad_clk domain
0x3C81	PSV_CTRL1	0x00	RW	Bit[7:5]: Reserved Bit[4]: Stream CLK all-on Bit[3]: tc_vsync_disable (auto-sleep) Bit[2]: Precharge v-blanking sync disable (auto-sleep) Bit[1:0]: Blanking retiming op (auto-sleep)
0x3C82	PSV_CTRL2	0x00	RW	Bit[7:0]: HTS number in pad_clk domain[15:8] (auto-sleep)
0x3C83	PSV_CTRL3	0xB1	RW	Bit[7:0]: HTS number in pad_clk domain[7:0] (auto-sleep)
0x3C84	PSV_CTRL4	0x00	RW	Bit[7:0]: CS initial value in pad_clk domain[15:8] (auto-sleep)
0x3C85	PSV_CTRL5	0x0F	RW	Bit[7:0]: CS initial value in pad_clk domain[7:0] (auto-sleep)
0x3C86	PSV_CTRL6	0x08	RW	Bit[7:0]: r_stream_st_offset[15:8]

table 6-17 PSV control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3C87	PSV_CTRL7	0x08	RW	Bit[7:0]: r_pchg_st_offset[15:8]
0x3C88	PSV_CTRL8	0x01	RW	Bit[7:0]: r_clk_winp_offset
0x3C89	PSV_CTRL9	0x02	RW	Bit[7:0]: r_stream_rear_offset
0x3C8A	PSV_CTRLA	0x02	RW	Bit[7:0]: r_pchg_rear_offset
0x3C8C	PSV_CTRLC	0x10	RW	Bit[7:0]: psv_auto_on_threshold[15:8] PSV mode auto on when VTS > psv_auto_on_threshold
0x3C8D	PSV_CTRLD	0x00	RW	Bit[7:0]: psv_auto_on_threshold[7:0] PSV mode auto on when VTS > psv_auto_on_threshold
0x3C90	PSV_CTRL10	0x00	RW	Bit[7:0]: r_mipi_pll_pd_sel[1:0] 00: Always-off 01: Stream blank off 10: Always-on 11: Stream CLK off
0x3C91	PSV_CTRL11	0x00	RW	Bit[7:0]: r_asp_pd[7:0]
0x3C92	PSV_CTRL12	0x00	RW	Bit[7:0]: r_asp_pd[15:8]
0x3C93	PSV_CTRL13	0x00	RW	Bit[7:0]: r_asp_pd[23:16]
0x3C94	PSV_CTRL14	0x00	RW	Bit[7:0]: r_asp_pd_sel[7:0]
0x3C95	PSV_CTRL15	0x00	RW	Bit[7:0]: r_asp_pd_sel[15:8]
0x3C96	PSV_CTRL16	0x00	RW	Bit[7:0]: r_asp_pd_sel[23:16]
0x3C97	PSV_CTRL17	0x00	RW	Bit[7:0]: r_asp_pd_sel[31:24]
0x3C98	PSV_CTRL18	0x00	RW	Bit[7:0]: r_asp_pd_sel[39:32]
0x3C99	PSV_CTRL19	0x00	RW	Bit[7:0]: r_asp_pd_sel[47:40]
0x3C9A~ 0x3C9D	NOT USED	–	–	Not Used
0x3C9E	PSV_CTRL1E	0x00	RW	Bit[7:0]: psv_auto_on_threshold[23:16] PSV mode auto on when VTS > psv_auto_on_threshold
0x3C9F	PSV_CTRL1F	0x00	RW	Bit[7:0]: r_steam_st_offset[7:0]
0x3CA0	PSV_CTRL20	0x00	RW	Bit[7:0]: r_pchg_st_offset[7:0]
0x3CA1	PSV_CTRL21	0x00	RW	Bit[7:0]: r_frame_timing_pd_enable[23:16]
0x3CA2	PSV_CTRL22	0x00	RW	Bit[7:0]: r_frame_timing_pd_enable[15:8]
0x3CA3	PSV_CTRL23	0x00	RW	Bit[7:0]: r_frame_timing_pd_enable[7:0]

table 6-17 PSV control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3CA4	PSV_CTRL24	0xFF	RW	Bit[7:0]: r_frame_timing_level_sel[23:16]
0x3CA5	PSV_CTRL25	0xFF	RW	Bit[7:0]: r_frame_timing_level_sel[15:8]
0x3CA6	PSV_CTRL26	0xFF	RW	Bit[7:0]: r_frame_timing_level_sel[7:0]
0x3CA7	NOT USED	–	–	Not Used
0x3CA8	PSV_CTRL28	0x00	RW	Bit[7:0]: r_frame_timing_t1_st_offset[15:8]
0x3CA9	PSV_CTRL29	0x00	RW	Bit[7:0]: r_frame_timing_t1_st_offset[7:0]
0x3CAA	PSV_CTRL2A	0x00	RW	Bit[7:0]: r_frame_timing_t2_st_offset[15:8]
0x3CAB	PSV_CTRL2B	0x00	RW	Bit[7:0]: r_frame_timing_t2_st_offset[7:0]
0x3CAC	PSV_CTRL2C	0x00	RW	Bit[7:0]: r_psv_end_cs_pt[15:8] Manual select CS counter point for switch between PSV and normal mode, adjust based on HTS
0x3CAD	PSV_CTRL2D	0x00	RW	Bit[7:0]: r_psv_end_cs_pt[7:0] Manual select CS counter point for switch between PSV and normal mode, adjust based on HTS
0x3CAE	PSV_CTRL2E	0x00	RW	Bit[7:1]: Reserved Bit[0]: r_psv_end_cs_pt_sel Enable for manual select CS counter point for switch between PSV and normal mode

6.18 TPM control [0x4D00 - 0x4D23]

table 6-18 TPM control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4D00	TPM_CTRL00	0x05	RW	Bit[7:0]: tpm_slope_h[7:0]
0x4D01	TPM_CTRL01	0x19	RW	Bit[7:0]: tpm_slope_h[7:0]
0x4D02	TPM_CTRL02	0xFD	RW	Bit[7:0]: tpm_offset_3[7:0]
0x4D03	TPM_CTRL03	0xD1	RW	Bit[7:0]: tpm_offset_2[7:0]
0x4D04	TPM_CTRL04	0xFF	RW	Bit[7:0]: tpm_offset_1[7:0]
0x4D05	TPM_CTRL05	0xFF	RW	Bit[7:0]: tpm_offset_0[7:0]

table 6-18 TPM control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4D06	TPM_CTRL06	0x08	RW	Bit[7:0]: Div
0x4D07	TPM_CTRL07	0x07	RW	Bit[7:0]: cnt_bit
0x4D08	TPM_CTRL08	0x00	RW	Bit[7:0]: clk_re
0x4D09	TPM_CTRL09	0x00	RW	Bit[7:0]: Stall
0x4D0A	TPM_CTRL10	0x00	RW	Bit[7:0]: otp_ctrl_en
0x4D0B	TPM_CTRL11	0x00	RW	Bit[7:0]: sof_update_en
0x4D0C	TPM_CTRL12	0x05	RW	Bit[7:0]: shift_bit
0x4D0D	TPM_CTRL13	0x00	RW	Bit[7:0]: pd_tpm_snr
0x4D0E	TPM_CTRL14	0x00	RW	Bit[7:0]: div_sel[0]
0x4D0F	TPM_CTRL15	0x00	RW	Bit[7:0]: mul_div_sel[0]
0x4D10	TPM_CTRL16	0x00	RW	Bit[7:0]: tpm_min[7:0]
0x4D11	TPM_CTRL17	0xFF	RW	Bit[7:0]: tpm_max[7:0]
0x4D12	TPM_CTRL18	0x00	RW	Bit[7:0]: tpm_f_en[0]
0x4D13	TPM_CTRL19	0x00	RW	Bit[7:0]: tpm_int_rdout[7:0]
0x4D14	TPM_CTRL20	0x00	RW	Bit[7:0]: tpm_dec_rdout[7:0]
0x4D15	TPM_CTRL21	0x00	RW	Bit[7:0]: tpm_int[7:0]
0x4D16	TPM_CTRL22	0x00	RW	Bit[7:0]: tpm_dec[7:0]
0x4D17	TPM_CTRL23	0x00	RW	Bit[7:0]: db_num[7:0]
0x4D18	TPM_CTRL24	0x00	RW	Bit[7:0]: db_real_h[7:0]
0x4D19	TPM_CTRL25	0x00	RW	Bit[7:0]: db_real_l[7:0]
0x4D1A	TPM_CTRL26	0x00	RW	Bit[7:0]: tpm_abs_3[7:0]
0x4D1B	TPM_CTRL27	0x00	RW	Bit[7:0]: tpm_abs_2[7:0]
0x4D1C	TPM_CTRL28	0x00	RW	Bit[7:0]: tpm_abs_1[7:0]
0x4D1D	TPM_CTRL29	0x00	RW	Bit[7:0]: tpm_abs_0[7:0]
0x4D1E	TPM_CTRL30	0x00	RW	Bit[7:0]: tpm_add_abs_3[7:0]
0x4D1F	TPM_CTRL31	0x00	RW	Bit[7:0]: tpm_add_abs_2[7:0]
0x4D20	TPM_CTRL32	0x00	RW	Bit[7:0]: tpm_add_abs_1[7:0]
0x4D21	TPM_CTRL33	0x00	RW	Bit[7:0]: tpm_add_abs_0[7:0]
0x4D22	TPM_CTRL34	0x00	RW	Bit[7:0]: tpm_add_h[7:0]
0x4D23	TPM_CTRL35	0x00	RW	Bit[7:0]: tpm_add_l[7:0]

7 operating specifications

7.1 absolute maximum ratings

table 7-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device; exposure to absolute maximum rated conditions for extended periods may affect device reliability

7.2 functional temperature

table 7-2 functional temperature

parameter	range
operating temperature[a]	-30°C to +85°C junction temperature
stable image temperature[b]	-10°C to +60°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

7.3 DC characteristics

table 7-3 DC characteristics (-30°C < T_J < 85°C)

symbol	parameter	min	typ	max[a]	unit
supply					
V_{DD-A}	supply voltage (analog)	2.7	2.8	3.0	V
V_{DD-D}	supply voltage (digital core for 2-lane MIPI up to 1000 Mbps/lane)	1.14	1.2	1.26	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	1.9	V
I_{DD-A}	active (operating) current[b]		26	31	mA
I_{DD-IO}			0.02	1	mA
I_{DD-D}			68	80	mA
$I_{DDS-XSHUTDOWN}$	standby current[c]		1	5	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.2V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[d]	SCL and SDA			0.54	V
V_{IH}	SCL and SDA	1.26			V

a. maximum active current is measured under typical supply voltage

b. DVDD is provided by external regulator for lower power consumption. DOVDD = 1.8V

c. standby current is measured at room temperature with external clock

d. based on DOVDD = 1.8V

7.4 timing characteristics

figure 7-1 reference clock input timing diagram

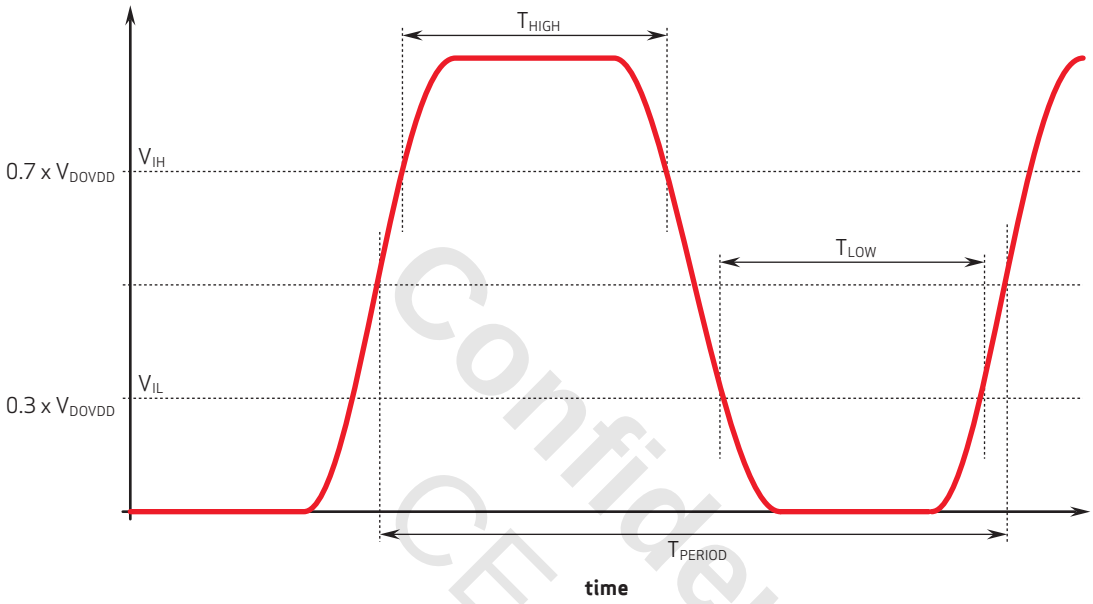


table 7-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{XVCLK}	frequency (EXTCLK)[a]	6	24	27	MHz
T_{PERIOD}	period (EXTCLK)	37	41.7	166.7	ns
T_{LOW}	low level width (XVCLK)	0.35×T_{PERIOD}		0.65×T_{PERIOD}	ns
T_{HIGH}	high level width (XVCLK)	0.35×T_{PERIOD}		0.65×T_{PERIOD}	ns

a. for input clock range 6~27 MHz, OS04C10 can tolerate input clock period jitter up to 600ps peak-to-peak

8 mechanical specifications

8.1 physical specifications

figure 8-1 package specifications

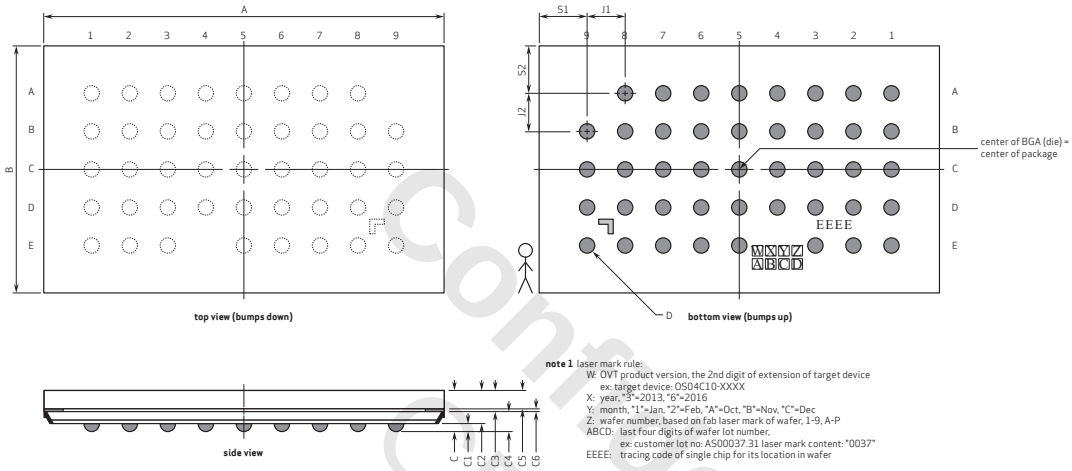


table 8-1 package dimensions (sheet 1 of 2)

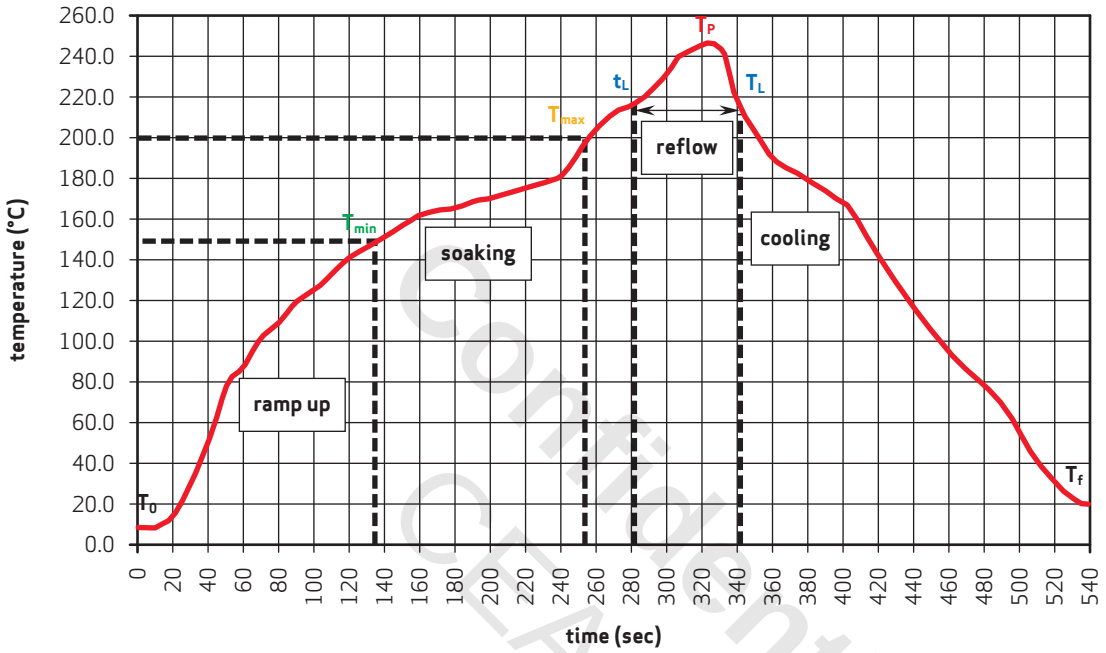
parameter	symbol	min	typ	max	unit
package body dimension x	A	6498.5	6523.5	6548.5	µm
package body dimension y	B	4001	4026	4051	µm
package height	C	610	670	730	µm
ball height	C1	100	130	160	µm
package body thickness	C2	505	540	575	µm
thickness from top glass surface to die	C3	325	345	365	µm
image plane height	C4	280	325	370	µm
glass thickness	C5	285	300	315	
air gap between sensor and glass	C6	41	45	49	
ball diameter	D	220	250	280	µm
total pin count	N		43		
pins pitch x-axis	J1		620		µm
pins pitch y-axis	J2		620		µm

table 8-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
edge-to-pin center distance along x	S1	751.75	781.75	811.75	µm
edge-to-pin center distance along y	S2	743	773	803	µm

8.2 IR reflow specifications

figure 8-2 IR reflow ramp rate requirements



note The OS04C10 uses a lead-free package.

note To reduce image artifacts from infrared light and to provide the best image quality. OmniVision recommends an IR cut filter.

table 8-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_P)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5° (duration max 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30 ~ 120 seconds
ramp down A (T_P to T_L)	cooling down from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling down from 217°C to room temperature	temperature slope ≤ 2°C per second
T_0 to T_P	room temperature to peak temperature	≤ 8 minutes

a. maximum number of reflow cycles = 3

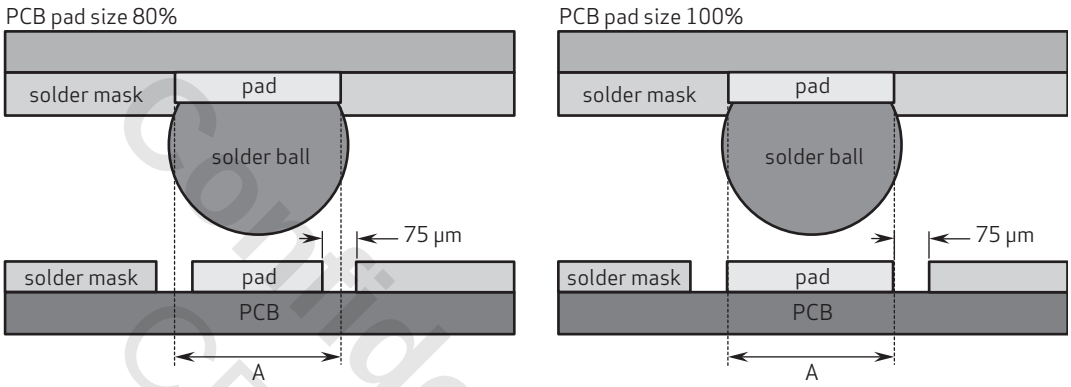
b. N2 gas reflow or control O2 gas PPM <500 as recommendation

8.3 PCB and SMT design recommendations

8.3.1 PCB design recommendations

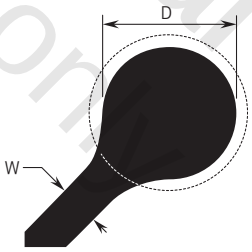
- solder pad of PCB: non solder mask defined (NSMD)
- PCB pad size: 90% ± 10% (80% ~ 100%) of package's ball pad opening
- gap between pad to neighboring solder mask: 75 µm (minimum)

figure 8-3 PCB pad example



- trace width: must be less than 1/2 ball diameter (W<1/2 D)
- recommend adding tear drop design on trace connecting to via and pad

figure 8-4 tear drop design example



- PCB material: high performance FR4 with high Tg and low CTE substrate material is recommended
- package edge to PCB edge minimum 1.0 mm is recommended

table 8-3 ball pad opening size and recommended PCB NSMD ball pad size

device name	package type	package size	CSP/BGA ball pad opening size	recommended PCB NSMD ball pad size
OS04C10	CSP	6523.5 µm × 4026 µm	250 µm	225 µm ± 25 µm

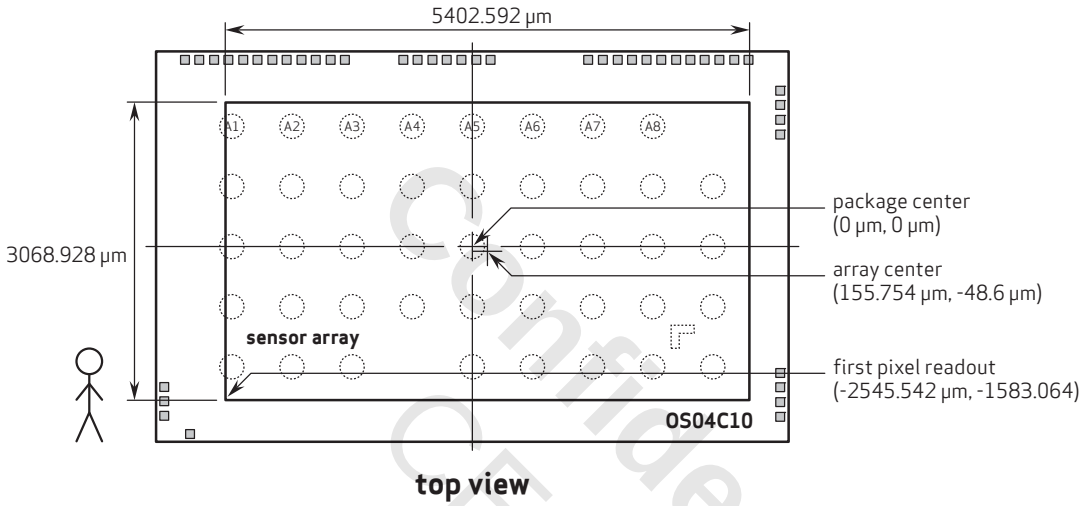
8.3.2 SMT design recommendations

- stencil: laser cut with electro-polishing
- stencil opening: 90~100% of PCB pad size
- stencil thickness: 0.08~0.15 mm
- solder material: SAC 305 is recommended
- solder paste: prefer type 4 (20 µm to 38 µm) or finer solder sphere particle size
- SMT profile: refer to solder paste datasheet and product datasheet

9 optical specifications

9.1 sensor array center

figure 9-1 sensor array center

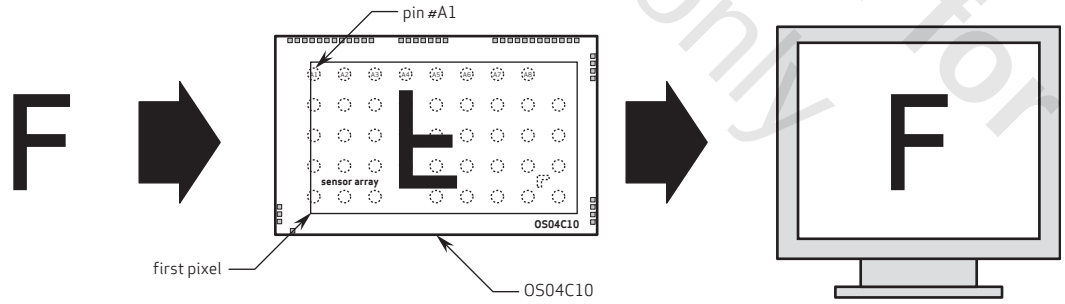


top view

note 1 this drawing is not to scale and is for reference only

note 2 as most optical assemblies mirror image, chip is typically mounted as above with first pixel at bottom left corner

figure 9-2 final image output



original image

output image

9.2 lens chief ray angle (CRA)

figure 9-3 chief ray angle (CRA)

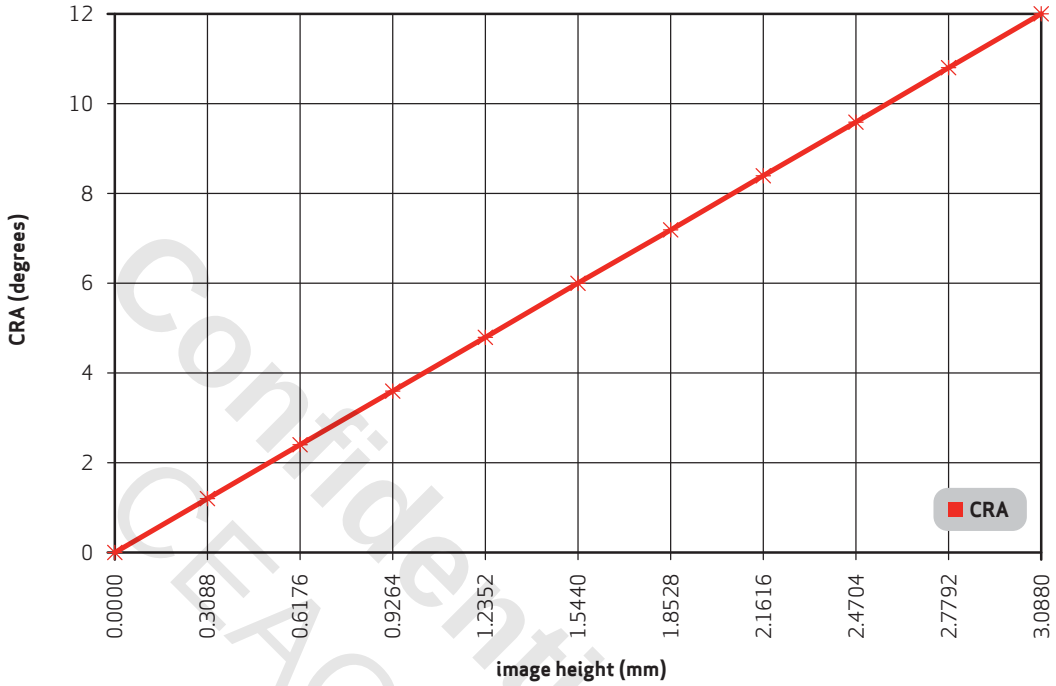


table 9-1 CRA versus image height plot

field (%)	image height (mm)	CRA (degrees)
0.0	0.0000	0.0
0.1	0.3088	1.2
0.2	0.6176	2.4
0.3	0.9264	3.6
0.4	1.2353	4.8
0.5	1.5440	6.0
0.6	1.8528	7.2
0.7	2.1616	8.4
0.8	2.4704	9.6
0.9	2.7792	10.8
1.0	3.0880	12.0

revision history

version 1.0 01.21.2020

- initial release

version 1.01 02.07.2020

- in chapter 7, added section 7.3
- in figure 8-1, changed note 2 to "as most optical assemblies mirror image, chip is typically mounted as above with first pixel at bottom left corner"

version 1.1 07.07.2020

- in features, removed seventh bullet for one-time programmable (OTP) memory
- in section 2.1, removed first sentence of fourth paragraph
- in table 2-2, changed title for fifth column table header to "10-bit output (AO) data rate"
- in table 3-1, added descriptions for register bits 0x3820[5], 0x3820[4], and 0x3820[3]
- in table 4-1, added row for register 0x3716, removed register description title of register 0x3820, added description for register bit 0x3820[5], changed description of register bit 0x3820[4] to "Vertical flip", added descriptions for register bits 0x3820[3], 0x3820[2], and 0x3820[1], and changed description of register bit 0x3820[0] to "vbinf_o"
- in section 4.1, added paragraph and setting examples immediately following table 4-1
- in chapter 4, removed section 4.5
- in table 5-1, removed description for register bits 0x5000[6] and 0x5000[4]
- in chapter 5, removed section 5.7

version 2.0 01.04.2021

- changed datasheet from Preliminary Specification to Product Specification
- in features, removed AO_180p and AO_90p supported image sizes from third bullet
- in key specifications, changed active power requirement specification to 155 mW, changed sensitivity specification to 14,700 e^-/Lux.sec, changed max S/N ratio specification to 37.9 dB, and changed dynamic range specification to 73.8 dB @ 15.5x gain
- in table 2-1, changed methodology for 720p format to "2x2 binning and cropping"
- in table 2-2, changed methodology for 360p format to "bin4" and removed rows for 180p and 90p formats
- in section 5.6, changed second bullet in 2-exposure staggered HDR mode to "...exposure range from 2 line up to VTS - Exp_0 - 12"
- in section 5.7, changed second sentence of third paragraph to "...by registers 0x5100~0x5105 and 0x5140~0x5145, provides..." and completely replaced table 5-7
- added new chapter 6

- in table 7-3 (previously table 6-3), changed typ and max values for supply symbol I_{DD-A} to 26 mA and 31 mA, respectively, changed typ and max values for supply symbol I_{DD-IO} to 0.02 mA and 1 mA, respectively, changed typ and max values for supply symbol I_{DD-D} to 68 mA and 80 mA, respectively, and changed typ and max values for supply symbol $I_{DDS-SHUTDOWN}$ to 1 µA and 5 µA, respectively
- in table 7-4 (previously table 6-4), added min, typ, and max values to symbol T_{PERIOD} and added table footnote a

version 2.01 02.25.2021

- in key specifications, changed dynamic range specification to 82.6 dB @ 15.5x gain
- in figure 2-2, changed D7 signal name to VN1 and C9 signal name to VN2 in U1 block
- in table 6-14, changed description of register bit 0x5000[6] to "Reserved"

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