datasheet

PRELIMINARY SPECIFICATION

1/4" color CMOS 1080p (1920x1080) HD image sensor
with OmniBSI™ technology

OS02F10

color CMOS 1080p (1920 x1080) HD image sensor with OmniBSI™ technology

datasheet (CSP)
PRELIMINARY SPECIFICATION

version 1.2
october 2018

To learn more about OmniVision Technologies, visit www.ovt.com.

applications

- security surveillance systems
- IP cameras
- HD analog cameras

ordering information

- **OS02F10-A34A** (color, lead-free)
  34-pin CSP

features

- supports 1080p (2 megapixel, 1936x1096) resolution
- supports windowing
- supports mirror and flip function
- supports auto black level calibration
- supports defective pixel correction
- supports black sun cancellation
- SCCB control interface for register programming
- supports 1k-bit OTP memory, 9 bytes for customer
- supports 2x2 binning function
- supports 10-bit / 8-bit RAW image data output
- supports MIPI 1-lane serial output interface
- supports DVP 10-bit / 8-bit output interface
- low power mode
- supports multi-camera synchronous function

key specifications (typical)

- **active array size:** 1920 x 1080
- **power supply:**
  core: 1.15V~1.3V (1.2V nominal)
  analog: 2.7V~3.0V (2.8V nominal)
  I/O: 1.7V~1.9V
- **power requirements:**
  active: <120 mW
- **temperature range:**
  operating: -30°C to +85°C junction temperature (see **table 7-2**)
  stable image: -10°C to +60°C junction temperature (see **table 7-2**)
- **output interfaces:** one-lane MIPI / DVP 10-bit/8-bit
- **output formats:** RAW10/RAW8
- **lens size:** 1/4"
- **lens chief ray angle: 9° linear (see figure 9-3)**
- **input clock frequency:** 6 ~ 27 MHz
- **maximum image transfer rate:**
  1080p: 30 fps
  720p: 45 fps
  VGA: 60 fps
- **sensitivity:** 10470 e⁻/Lux-sec (5100K G channel)
- **shutter:** rolling
- **max S/N ratio:** 38.1 dB
- **dynamic range:** 72.9 dB @ 16x gain
- **pixel size:** 2 µm x 2 µm
- **image area:** 3868.128 µm x 2198.808 µm
- **package dimensions:** 4920.6 µm x 2964 µm

note Power requirements specifications are estimated values and are subject to change when measured data using real silicon is available.

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OS02F10 image sensor. The package information is shown in **section 9**.

figure 1-1 pin diagram

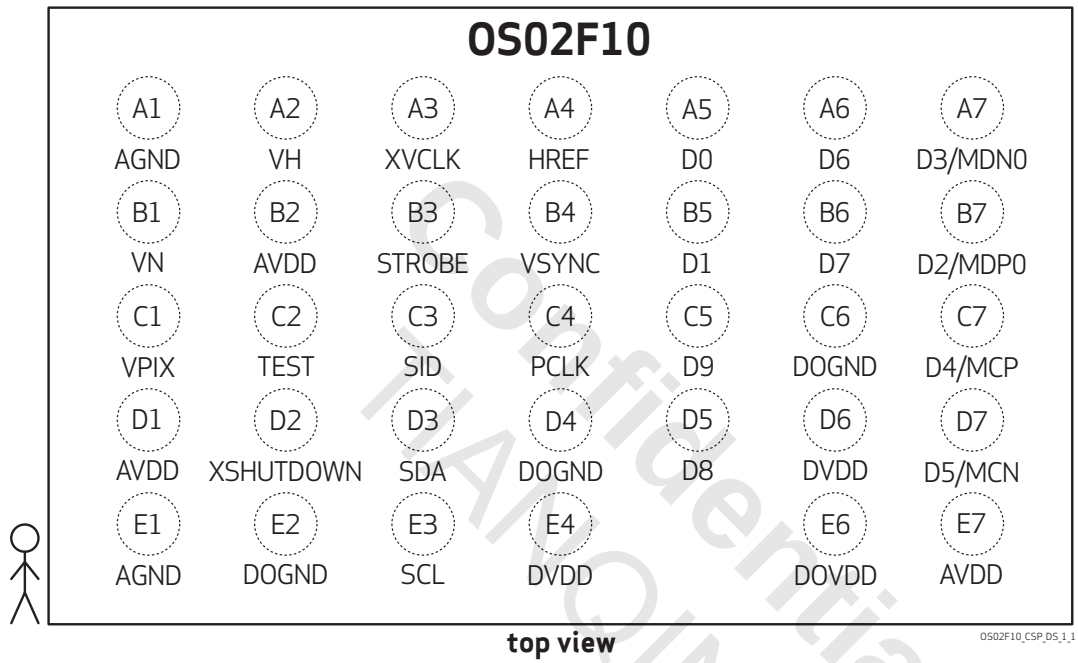


table 1-1 signal descriptions (sheet 1 of 2)

pin number	signal name	pin type	description
A1	AGND	ground	analog ground
A2	VH	reference	internal analog reference
A3	XVCLK	input	external clock input
A4	**HREF**	output	HSYNC output
A5	**D0**	output	data[0] output
A6	**D6**	output	data[6] output
A7	**D3/MDN0**	output	data[3] and MIPI outn0 output
B1	VN	reference	internal analog reference

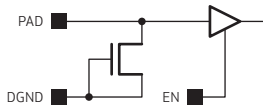
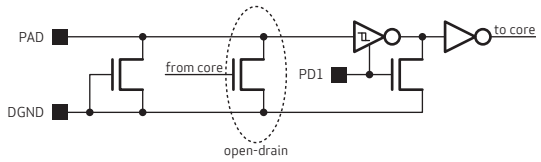
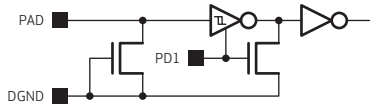
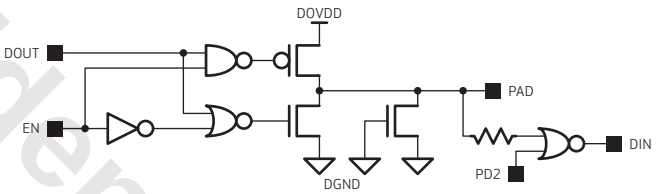
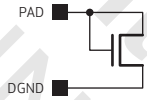
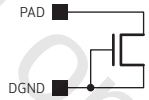
table 1-1 signal descriptions (sheet 2 of 2)

pin number	signal name	pin type	description
B2	AVDD	power	analog power 2.8V
B3	**STROBE**	output	strobe output
B4	**VSYNC**	I/O	VSYNC output and FSIN input
B5	**D1**	output	data[1] output
B6	**D7**	output	data[7] output
B7	**D2/MDP0**	output	data[2] and MIPI outp0 output
C1	VPIX	output	external connect capacitance (1µf)
C2	TEST	reference	internal analog reference
C3	**SID**	input	SID control
C4	**PCLK**	output	pixel output clock
C5	**D9**	output	data[9] output
C6	DOGND	ground	digital ground
C7	**D4/MCP**	output	data[4] and MIPI CLKP output
D1	AVDD	power	analog power 2.8V
D2	**XSHUTDOWN**	input	reset and power down (active low)
D3	**SDA**	I/O	slave SCCB data
D4	DOGND	ground	digital ground
D5	**D8**	output	data[8] output
D6	DVDD	power	digital core power 1.2V
D7	**D5/MCN**	output	data[5] and MIPI CLKN output
E1	AGND	ground	analog ground
E2	DOGND	ground	digital ground
E3	**SCL**	input	slave SCCB CLK
E4	DVDD	power	digital core power 1.2V
E6	DOVDD	power	digital i/o power 1.8V
E7	AVDD	power	analog power 2.8V

table 1-2 pin states under various conditions

pin number	signal name	RESET	after RESET	software standby
A4	HREF	high-z	high-z	high-z by default (configurable)
A5	D0	high-z	high-z	high-z by default (configurable)
A6	D6	high-z	high-z	high-z by default (configurable)
A7	D3/MDN0	high-z	high-z	high-z by default (configurable)
B3	STROBE	high-z	high-z	high-z by default (configurable)
B4	VSYNC	high-z	high-z	high-z by default (configurable)
B5	D1	high-z	high-z	high-z by default (configurable)
B6	D7	high-z	high-z	high-z by default (configurable)
B7	D2/MDP0	high-z	high-z	high-z by default (configurable)
C3	SID	input	input	input
C4	PCLK	high-z	high-z	high-z by default (configurable)
C5	D9	high-z	high-z	high-z by default (configurable)
C7	D4/MCP	high-z	high-z	high-z by default (configurable)
D2	XSHUTDOWN	input	input	input
D3	SDA	open-drain	I/O	I/O
D5	D8	high-z	high-z	high-z by default (configurable)
D7	D5/MCN	high-z	high-z	high-z by default (configurable)
E3	SCL	high-z	input	input

table 1-3 pad symbol and equivalent circuit

symbol	equivalent circuit
XVCLK	
SDA	
SCL	
STROBE, HREF, VSYNC	
VN	
MDP0, MDN0, MCP, MCN, AGND, DOGND, VH	

2 system level description

2.1 overview

The OS02F10 image sensor is a high quality, 1/4 inch, 1080p format, CMOS image sensor. It provides high quality digital images and high-definition (HD) video. The OS02F10 is intended for products including security surveillance systems, IP cameras and HD analog cameras.

By introducing an advanced 2 µm pixel architecture, the OS02F10 achieves excellent low-light sensitivity, signal-to-noise ratio, full-well capacity, quantum efficiency, and low-power consumption. The default mode and programmable mode allow a more convenient way for controlling the parameters of frame size, exposure time, gain value, and so on. It also offers the following image control functions: mirror and flip, windowing, auto black level calibration, defective pixel correction, black sun cancellation, and so forth.

The OS02F10 supports a high frame rate up to 30 fps @ 1080p format though a DVP interface or MIPI interface. These prominent features integrated in the OS02F10 allow for a best-in-class image sensor, bringing users vivid pictures and excellent experience.

2.2 architecture

The OS02F10 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OS02F10 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, pre-charging and sampling the rows of the array sequentially. In the time between pre-charging and sampling a row, the charge in the pixels decreases with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between pre-charging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs up to 10-bit data for each pixel in the array.

figure 2-1 OS02F10 block diagram

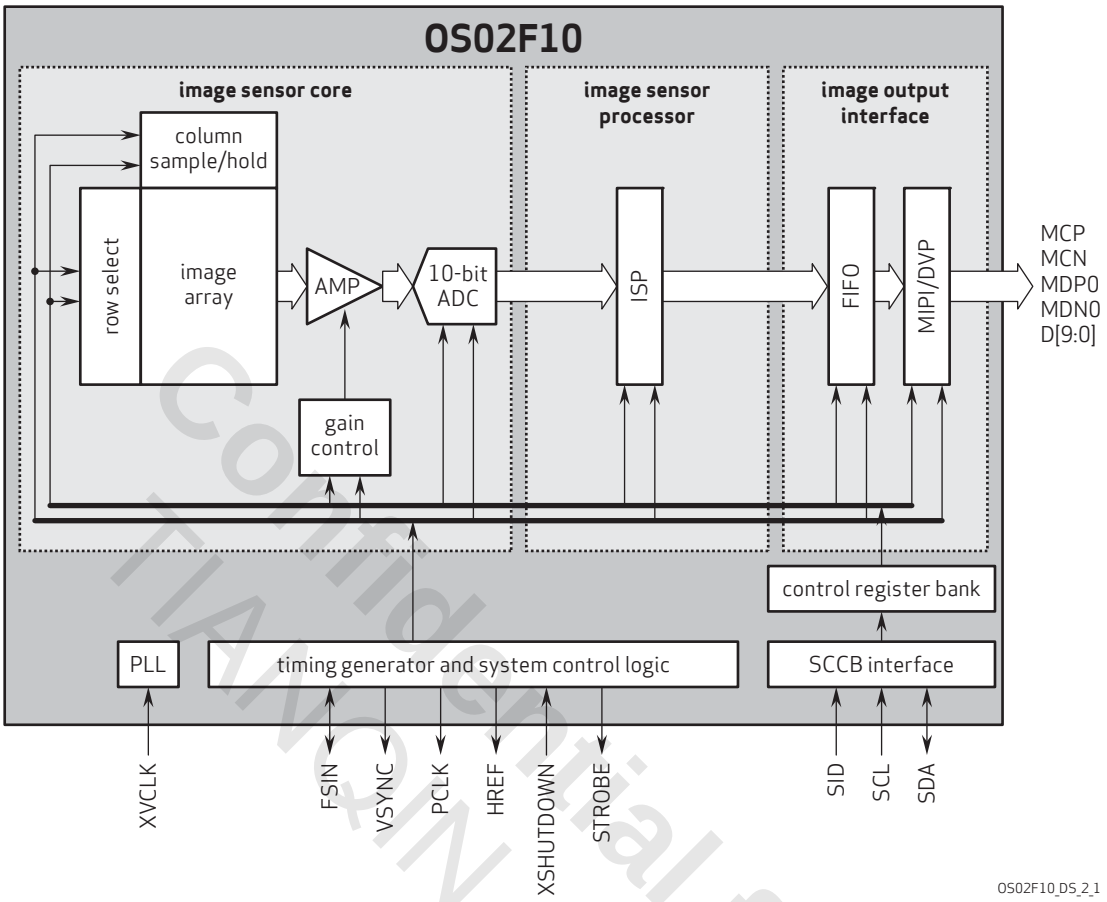
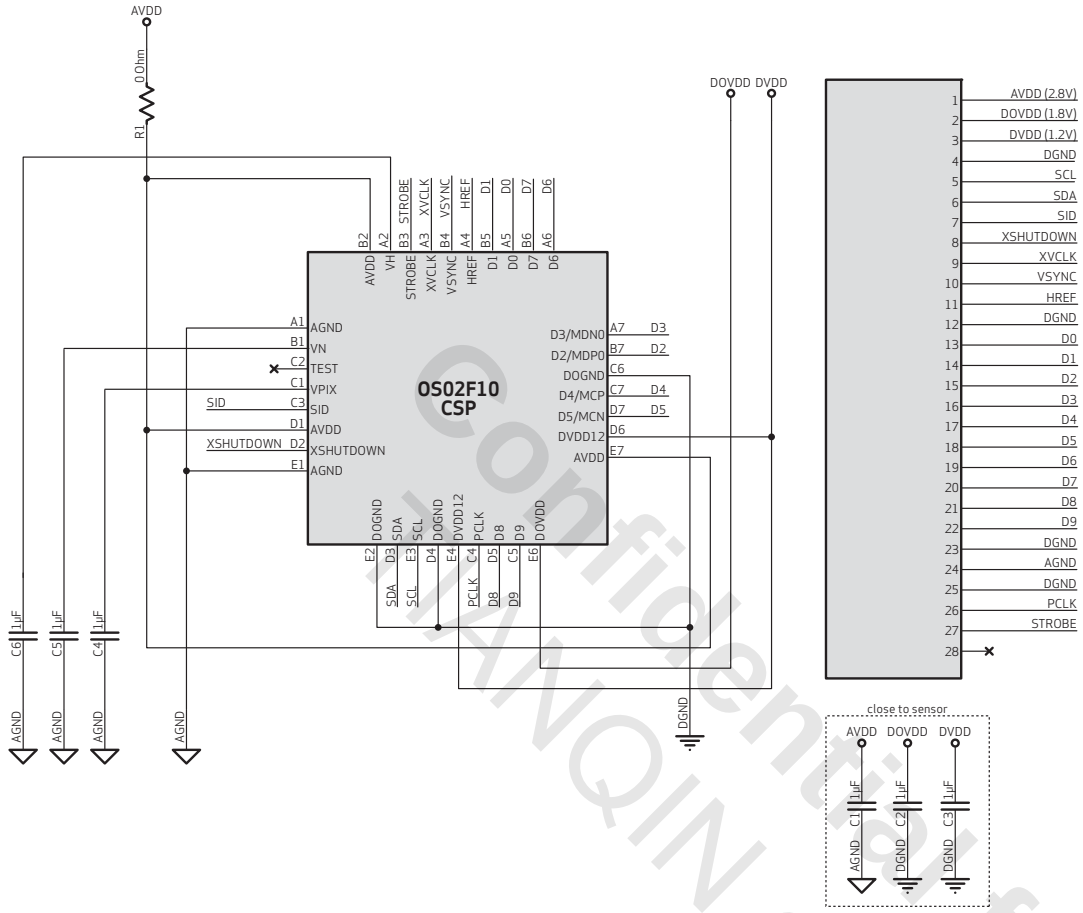


figure 2-2 OS02F10 DVP reference schematic



note 1 AVDD must be set as 2.8V, DOVDD is compatible with 1.8V, DVDD is 1.2V

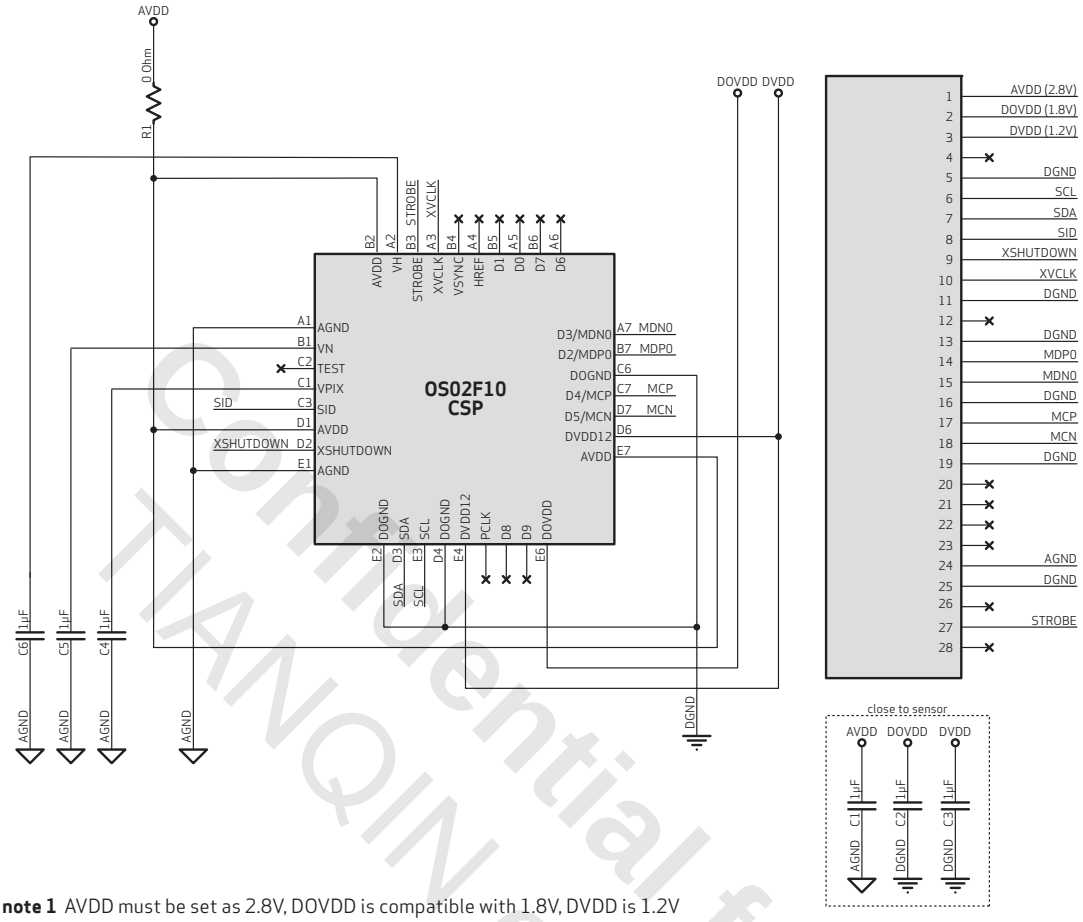
note 2 this design is 10-bit DVP mode, in which D2/MDP0, D3/MDN0, D4/MCP, D5/MCN are multiplexed pins, respectively for D2, D3, D4, D5 to use. When in 8-bit mode, D[9:2], D0, D1 can be suspended, SID is controlled by SCCB address pins. when SID is low, write address is 0x78, and read address is 0X79; when SID is high, write address is 0x7A, and read address is 0X7B

note 3 chip power supply filter capacitor (minimum must be affixed to 0402 1μF) should be placed near power supply pins (AVDD, DOVDD, DVDD, VPIX, VH, VN), platform is sent into chip AVDD to reserve series resistance position and default value is 0 Ohm. Sensor's AGND and DGND should be inside module separately, AVDD and AGND should not be adjacent to clock, power supply should have no finer than 0.12mm design, ground floor dragnet

note 4 FPC using anti-jamming design

OS02F10_CSP_DS_2_2

figure 2-3 OS02F10 MIPI reference schematic



note 1 AVDD must be set as 2.8V, DOVDD is compatible with 1.8V, DVDD is 1.2V

note 2 This design is MIPI mode, in which D2/MDP0, D3/MDN0, D4/MCP, D5/MCN are multiplexed pins, respectively for MDP0, MDN0, MCP, MCN to use. SID is controlled by SCCB address pins. When SID is low, write address is 0x78 and read address is 0x79; when SID is high, write address is 0x7A, and read address is 0x7B

note 3 chip power supply filter capacitor (minimum must be affixed to 0402 1μF) should be placed near power supply pins (AVDD, DOVDD, DVDD, VPIX, VH, VN), platform is sent into chip AVDD to reserve eries resistance position and default value is 0 Ohm. Sensor's AGND and DGND should be inside module separately, AVDD and AGND should not be adjacent to clock, power supply should have no finer than 0.12mm design, ground floor dragnet

note 4 MCP/MCN, MDP0/MDN0 are two pairs of differential lines, line should be covered by the ground as equal distance as possible. Bottom of differential line (or TOP level) must have a complete reference point. When PCB proofing, it is necessary to tell PCB manufacturers which are requirements of differential lines. Manufacturer should also carry out impedance control and impedance standard is 100 Ohm, error should not exceed ±10%.

note 5 FPC using anti-jamming design

OS02F10_CSP_DS_2.3

2.3 format and frame

The OS02F10 supports RAW RGB output with one MIPI interface.

table 2-1 format and frame rate

format	resolution	max frame rate	methodology	10-bit output MIPI data rate	DVP clock frequency
1080p	1936 x 1096	30 fps	full resolution qualified pixel (1920+16) x (1080+16)	1 lane @720 Mbps/lane 10-bit MIPI	72 MHz
720p	1280 x 720	45 fps	crop from full resolution	1 lane @720 Mbps/lane 10-bit MIPI	72 MHz
2x binning	968 x 548	60 fps	2x binning qualified pixel (960+8) x (540+8)	1 lane @720 Mbps/lane 10-bit MIPI	72 MHz
VGA	640 x 480	60 fps	cropping and binning	1 lane @720 Mbps/lane 10-bit MIPI	72 MHz

2.4 output interface

Both MIPI and parallel data output interface are integrated inside the OS02F10.

2.4.1 DVP interface

The DVP interface is used to interface between a peripheral device and a host processor. A traditional DVP interface is embedded in the OS02F10. As a result, the OS02F10 can be compatible with most existing mainstream platforms.

2.4.2 MIPI interface

The MIPI interface is a serial interface which can support high-speed, high-precision, and large-array transmission. So, it plays an important role in security surveillance, video conferencing, traffic sign recognition, etc. With it, the OS02F10 can provide higher definition images to the applications.

The MIPI inside the OS02F10 provides one single uni-directional clock lane and one-data-lane solutions for communication links between components inside the application device. This MIPI can support some kinds of operating mode, such as burst mode, switch mode, ULPs mode, and line sync mode. Users can select appropriate mode according to their requirements.

2.4.3 D-PHY function

The D-PHY converts DVP data from CSI_TOP to serial data that are compatible with MIPI protocol. Detailed time sequences are shown in **figure 2-4** and **figure 2-5**.

figure 2-4 switching the clock lane between clock transmission and low-power mode

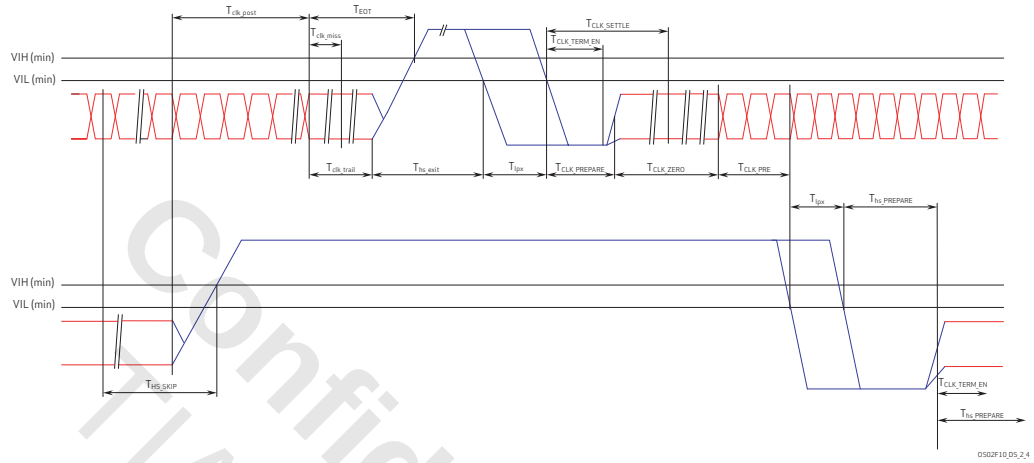
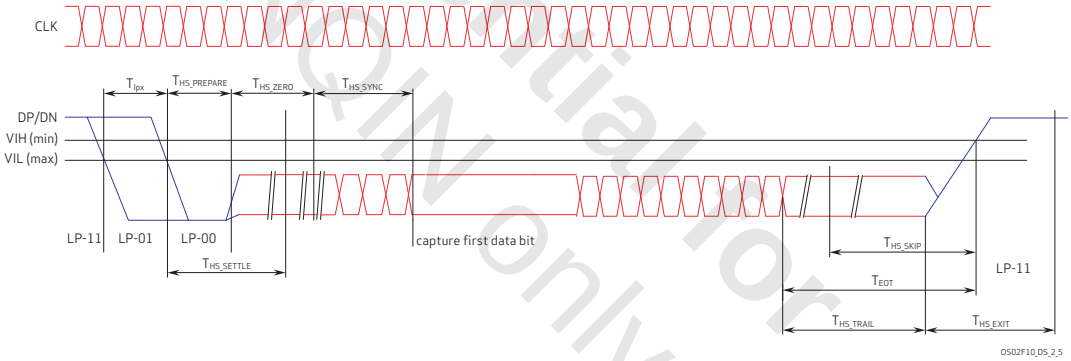


figure 2-5 high-speed data transmission bursts



2.4.4 data lane parameters

table 2-2 data lane parameters

parameter	target	min	max
$T_{HS-PREPARE}$	time that transmitter drives data lane LP-00 line state immediately before HS-0 Line state starts HS transmission	40 ns + 4*UI	85 ns+6*UI
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that transmitter drives HS-0 state prior to transmitting sync sequence	145 ns + 10*UI	
$T_{HS-SETTLE}$	time interval which HS receive shall ignore any data lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$	85 ns + 6*UI	145 ns+10*UI
$T_{HS-SKIP}$	time interval which HS-RX should ignore any transitions on data lane, following a HS burst end point of interval is defined as beginning of LP-11 state following HS burst	40	55 ns+4*UI
$T_{HS-TRAIL}$	time that transmitter drives HS-0 state after last payload clock bit of a HS transmission burst	max (n*8*UI, 60ns + n*4*UI)	
T_{LPX}	transmitted length of any low-power state period	50 ns	
T_{WAKEUP}	time that a transmitter drives a Mark-1 state prior to a stop state in order to initiate an exit from ULPS	1 ms	

2.4.5 clock lane parameters

table 2-3 clock lane parameters

parameter	target	min	max
$T_{CLK-MISS}$	timeout for receive to detect absence of clock transmission and disable clock lane HS-RX	60 ns	
$T_{CLK-POST}$	time that transmitter continues to send HS clock after last associated data lane has transitioned to LP mode interval is define as period from end of $T_{HS-TRAIL}$ to the beginning $T_{CLK-TRAIL}$	60 ns + 52*UI	
$T_{CLK-PRE}$	time that HS clock will be driven by transmitter prior to any associated data lane beginning transition from LP to HS mode	8*UI	
$T_{CLK-PREPARE}$	time that transmitter drives clock lane LP-00 line state immediately before HS-0 line state starts HS transmission	38 ns	95 ns
$T_{CLK-SETTLE}$	time interval which HS receive will ignore any clock lane HS transmissions, starting from beginning of $T_{CLK-PREPARE}$	95 ns	300 ns
$T_{CLK-TRAIL}$	time that the transmitter driver the HS-0 state after the last payload clock bit of a HS transmission burst.	60 ns	
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that transmitter drives HS-0 state prior to starting clock	300 ns	
T_{EOT}	transmitted time interval from start of $T_{CLK-TRAIL}$ or $T_{HS-TRAIL}$, to start of LP-11 state following a HS burst		105 ns + n*12*UI

2.5 power up/off sequence

2.5.1 power up sequence

figure 2-6 power up sequence diagram

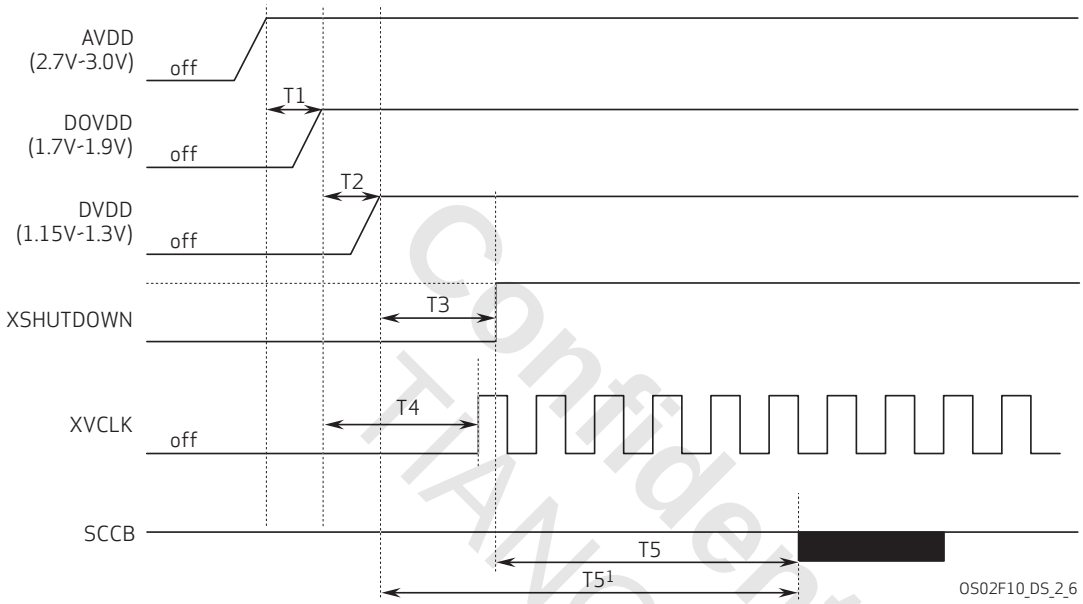


table 2-4 power up sequence parameters

symbol	description	min	unit
T1	delay from AVDD to DOVDD	0	ms
T2	delay from DOVDD to DVDD	0	ms
T3	delay from DVDD stable to sensor power up stable	5	ms
T4	delay from DOVDD stable to XVCLK on	0	ms
T5	delay from sensor power up stable to SCCB initialization	9	ms
T5[1]	if XSHUTDOWN = 1 T5[1] = T3+T5, T5[1] starts at DVDD power up stable	14	ms

2.5.2 power off sequence

figure 2-7 power off sequence diagram

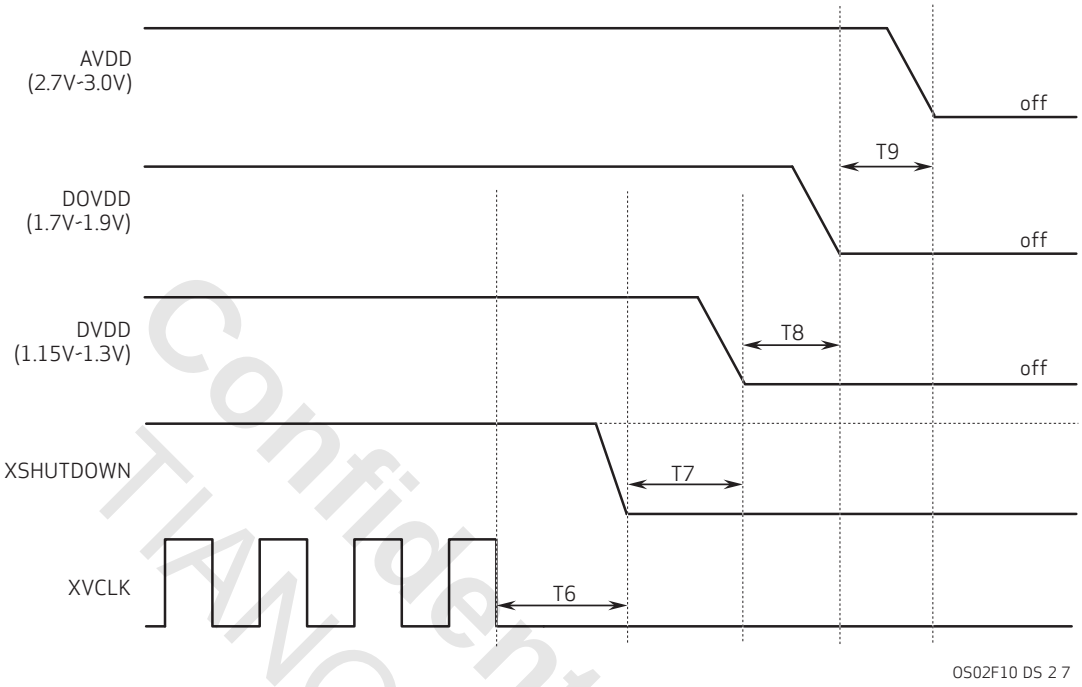


table 2-5 power up sequence parameters

symbol	description	min	unit
T6	delay from XSHUTDOWN pull low stable to XVCLK off	0	ms
T7	delay from sensor power down to DVDD off	0	ms
T8	delay from DVDD off to DOVDD off	0	ms
T9	delay from DOVDD off to AVDD off	0	ms

2.6 SCCB bus

2.6.1 single read and single write

The OS02F10 SCCB write address and read address can be selected by the SID pin. When the pin is set high, the write address is 0x7A and the read address is 0x7B. When the pin is set low, the write address is 0x78 and the read address is 0x79.

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a write and a '1' indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First, the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

figure 2-8 illustrates the OS02F10 single read sequence and single write sequence.

figure 2-8 SCCB read and write message description, SID pin set high

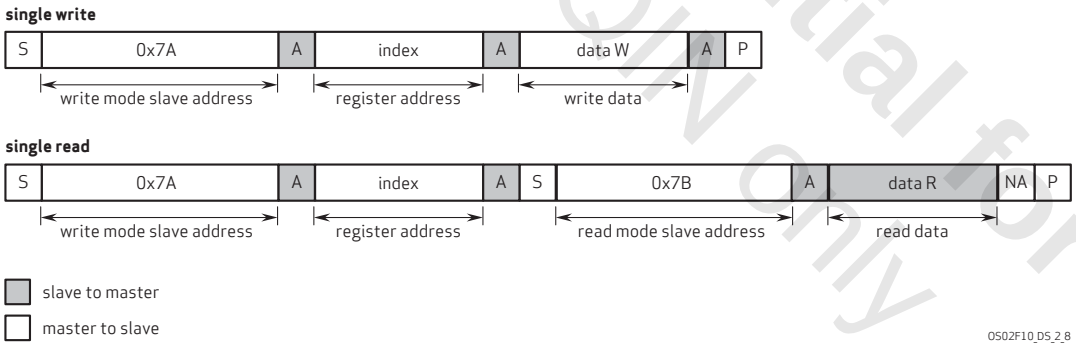
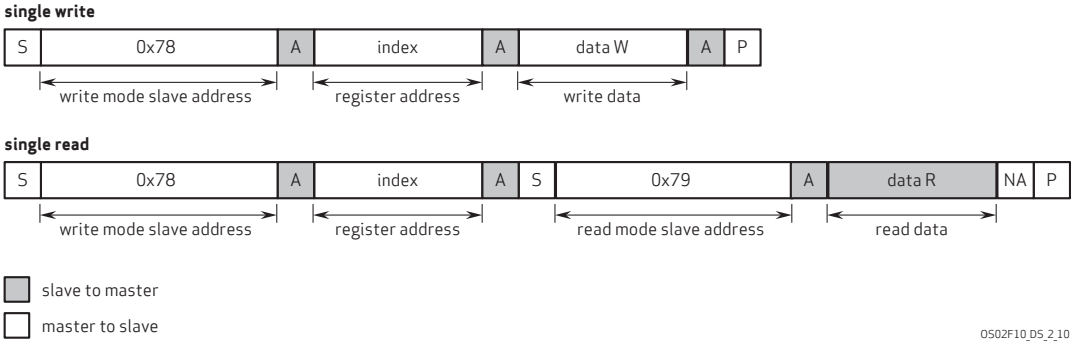


figure 2-9 SCCB read and write message description, SID pin set low



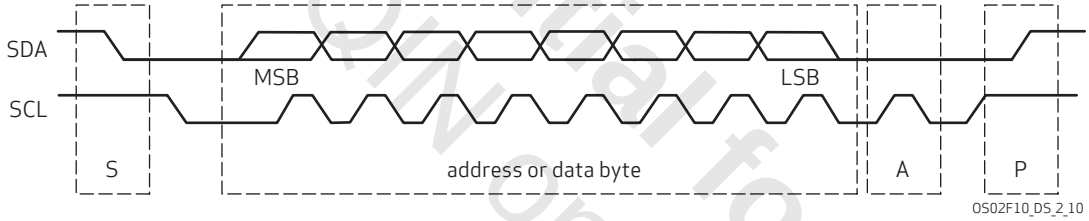
2.6.2 data bit transfer

One data bit is transferred during each clock pulse. The serial clock pulse is provided by the master. The data must be stable during the high period of the serial clock. It can only change when the serial clock is low. Data is transferred 8 bits at a time, followed by an acknowledge bit.

2.6.3 acknowledge bit

The OS02F10 will hold the value of the SDA pin to logic '0' during the logic '1' state of the acknowledge clock pulse on SCL.

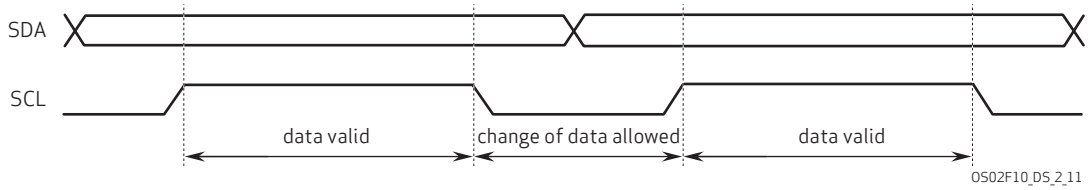
figure 2-10 SCCB acknowledge bit diagram



2.6.4 data valid

The master must ensure that the data is stable during the logic 1 state of the SCL pin. All transitions on the SDA pin can only occur when the logic level on the SCL pin is '0'.

figure 2-11 SCCB data transport diagram



2.6.5 timing parameter

figure 2-12 SCCB bus timing parameter diagram

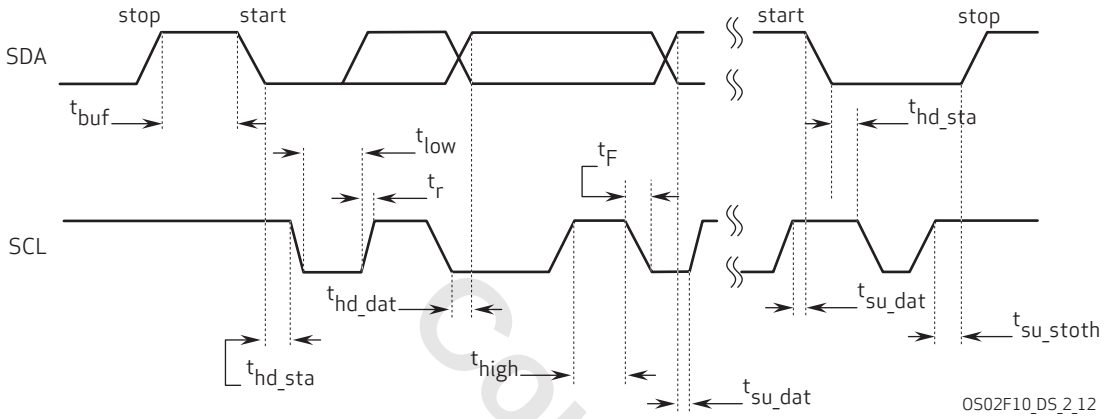


table 2-6 SCCB interface timing specifications

symbol	parameter	min	max	unit
f_{scl}	SCL clock frequency	–	400	kHz
t_{buf}	bus free time between a stop and a start	1.3	–	µs
t_{hd_sta}	hold time for a repeated start	0.6	–	µs
t_{low}	LOW period of SCL	1.3	–	µs
t_{high}	HIGH period of SCL	0.6	–	µs
t_{su_sta}	setup time for a repeated start	0.6	–	µs
t_{hd_dat}	data hold time	0	–	µs
t_{su_dat}	data setup time	0.1	–	µs
t_r	rise time of SCL, SDA	–	0.3	µs
t_f	fall time of SCL, SDA	–	0.1	µs
t_{su_sto}	setup time for a stop	0.6	–	µs
t_{aa}	SCL low to data out valid	0.3	–	µs
t_{dh}	data out hold time	0.2	–	µs
C_b	capacitive load of bus line (SCL, SDA)	–	–	pf

3 block level description

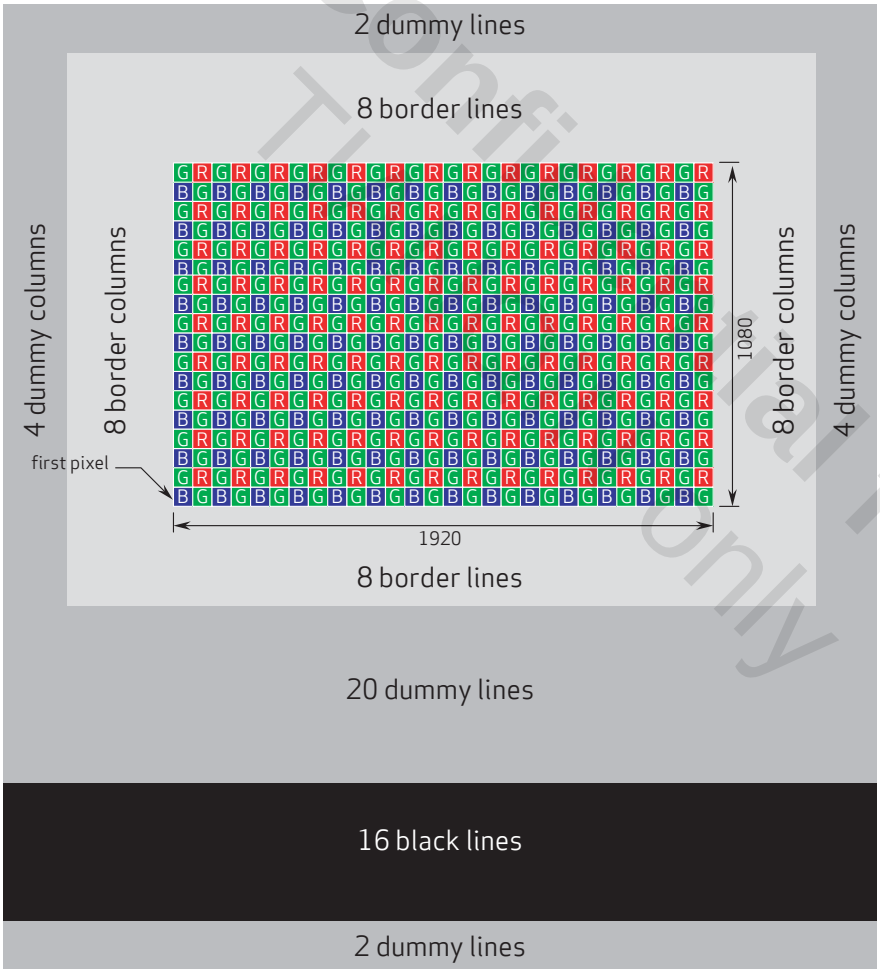
3.1 pixel array structure

The OS02F10 sensor has an image array of 1944 columns by 1136 rows (2,208,384 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color GR/BG array is arranged in line-alternating fashion. Of the 2,208,384 pixels, 2,073,600 (1920x1080) are active pixels and can be output.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

figure 3-1 sensor array region color filter layout



note color filter for first pixel at left bottom is blue

OS02F10_DS_3_1

3.2 2x2 binning

The OS02F10 supports a binning mode to provide a lower resolution output while maintaining the field of view. With binning mode on, the voltage levels of adjacent pixels (of the same color) are averaged before being sent to the ADC. The OS02F10 supports 2x2 binning and mono binning, which is illustrated in **figure 3-2** and **figure 3-3**, where the voltage levels of two horizontal (2x1) adjacent same-color pixels are averaged.

figure 3-2 example of 2x2 binning

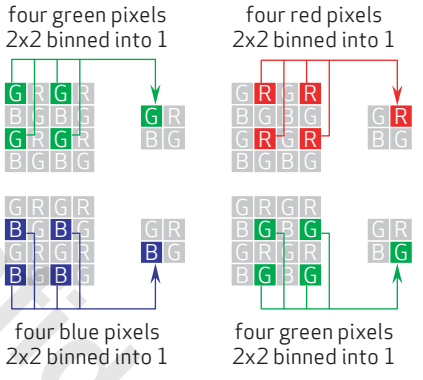
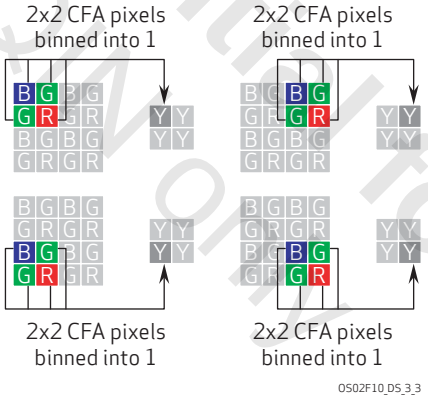


figure 3-3 example of mono binning



3.3 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

3.4 10-bit A/D converters

The balanced signal is then digitized by the on-chip 10-bit ADC.

3.5 PLL and clock generator

3.5.1 PLL

The OS02F10 contains a phase locked loop (PLL) block, which generates all the necessary internal clocks from the external clock input.

The internal function blocks of the PLL are shown in **figure 3-4**.

figure 3-4 clock scheme

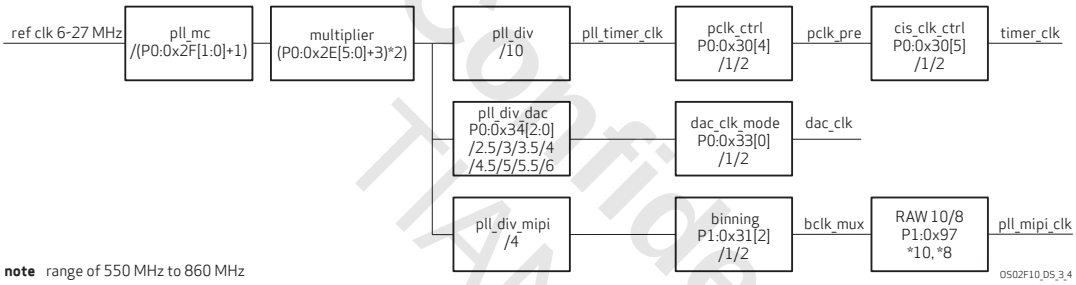


table 3-1 clock registers (sheet 1 of 3)

address	register name	default value	R/W	description
P0:0x2E	PLL_NC_BUF	0x0C	RW	Bit[6:0]: pll_nc_buf PLL_VCO = [PLL input*(pll_nc+3)*2/(pll_mc+1)] Note: Parameters of registers will be enabled in next frame.
P0:0x2F	PLL_CTRL_BUF	0x3C	RW	Bit[7]: pll_clk_sel 0: Disable bypass PLL 1: Enable bypass PLL Bit[1:0]: pll_mc PLL_VCO = [PLL input*(pll_nc+3)*2/(pll_mc+1)] Note: Parameters of registers will be enabled in next frame.

table 3-1 clock registers (sheet 2 of 3)

address	register name	default value	R/W	description
P0:0x30	CLK_MODE_BUF	0x20	RW	Bit[5]: cis_clk_ctrl 0: timer_clk = pclk_pre 1: timer_clk = pclk_pre/2 Bit[4]: pclk_ctrl 0: pclk_pre = pll_timer_clk 1: pclk_pre = pll_timer_clk/2 Bit[0]: isp_clk_ctrl 0: dclk = timer_clk 1: dclk = timer_clk/2
P0:0x32	ROW_CLK_CTRL_BUF	0x02	RW	Bit[1:0]: row_clk_ctrl 00: row_clk = dac_clk/2 01: row_clk = dac_clk/4 10: row_clk = dac_clk/8 11: Not used
P0:0x33	CLK_MODE_CTRL	0x04	RW	Bit[3]: pclk_gating_en_buf 0: Disable PCLK gating 1: Enable PCLK gating Bit[2]: pclk_inv_buf 0: Disable PCLK reverse 1: Enable PCLK reverse Bit[1]: cnt_clk_inv_en_buf 0: Disable cnt_clk reverse 1: Enable cnt_clk reverse Bit[0]: dac_clk_mode_buf 0: dac_clk = cnt_clk 1: dac_clk = cnt_clk/2 Note: Parameters of registers will be enabled in next frame.
P0:0x34	PLL_DIV_CTL	0x71	RW	Bit[6:5]: pll_div_pcp Bit[4:3]: pll_div_ncp Bit[2:0]: pll_div_dac_buf PLL frequency divider control PLL output = CLK * (pll_nc + 3) / (pll_mc + 1) / (2.5 + pll_div_dac * 0.5) Note: Parameters of registers will be enabled in next frame.

table 3-1 clock registers (sheet 3 of 3)

address	register name	default value	R/W	description
P0:0x35	PLL_CTL	0x00	RW	Bit[7:4]: pll_bias_ctl PLL chargepump current control 000: 5 u 001: 10u (default) 010: 15u 011: 20u 100: 25u 101: 30u (default) 110: 35u 111: 40u Bit[3:2]: pll_dctl Choose PLL's PFD delay time to remove dead zone 00: 478p (default) 01: 932p 10: 1.334n 11: 1.736n
P1:0x31	RESOLUTION_ SELECTION	0x00	RW	Bit[2]: Binning mode enable 1: Binning mode enabled (sensor outputs 968x548 and MIPI clock is divided by 2)
P1:0x97	DATA ID	0x2B	RW	Bit[5:0]: Data type sel 0x2A: RAW8 0x2B: RAW10

4 image sensor core digital functions

4.1 mirror and flip

The OS02F10 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

The mirror and flip function can be set by register exp_rpc_en (P1:0x01). exp_rpc_en (P1:0x01) must be configured after configuring the mirror and flip register (P1:0 x01 = 0x01).

figure 4-1 mirror and flip samples

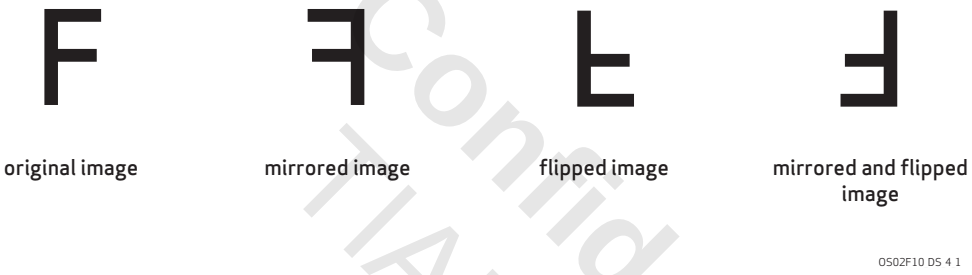


table 4-1 mirror and flip registers

address	register name	default value	R/W	description
P1:0x3F	MIRROR/FLIP	0x00	RW	Bit[1]: Vertical upside down Bit[0]: Horizontal mirror 0x00: Normal (no flip) 0x01: Horizontal flip 0x02: Vertical flip 0x03: Both horizontal and vertical flip

4.2 windowing

The embedded windowing function extracts an image windowing area by defining four parameters, including horizontal start, horizontal width, vertical start, and vertical height. By properly setting the parameters, the portions within the sensor array size can be cropped as a visible area. The windowing function will not conflict with the mirror and flip function.

figure 4-2 windowing function diagram

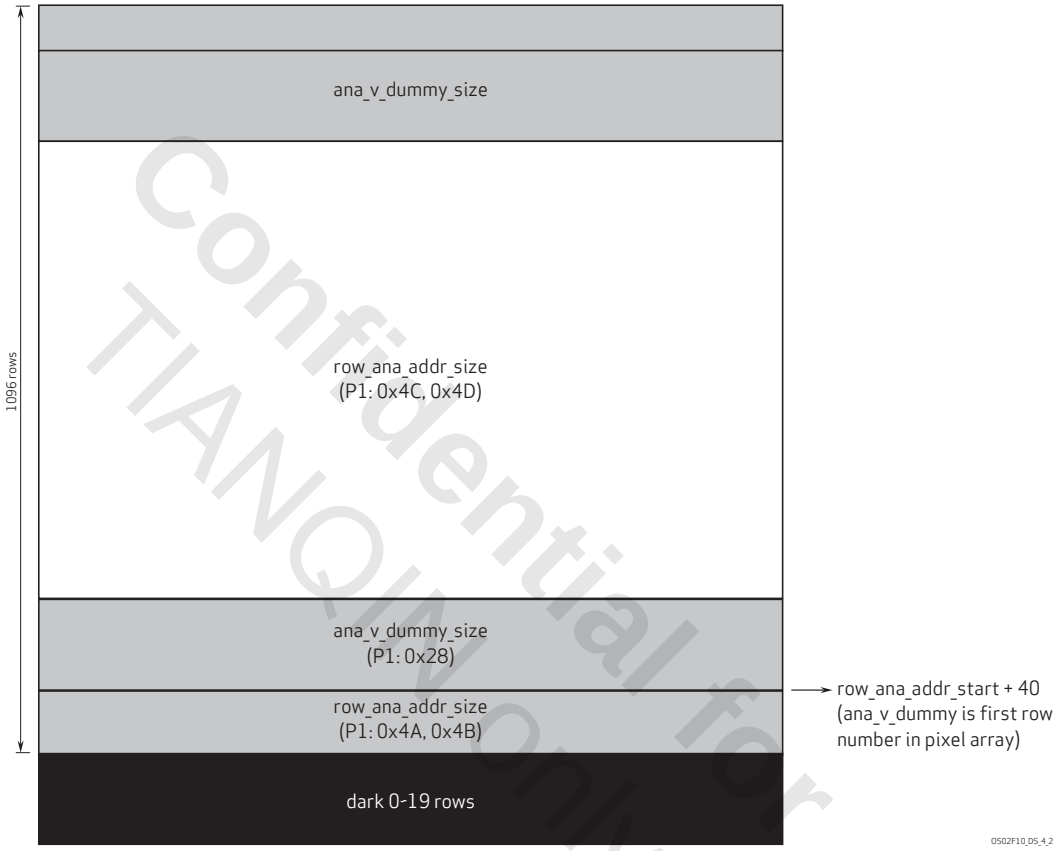


table 4-2 mirror and flip registers (sheet 1 of 2)

address	register name	default value	R/W	description
P2:0xA0	DEM_V_START_4MSB	0x00	RW	Bit[3:0]: dem_v_start[11:8] Image vertical start 4 MSB
P2:0xA1	DEM_V_START_8LSB	0x00	RW	Bit[7:0]: dem_v_start[7:0] Image vertical start 8 LSB

table 4-2 mirror and flip registers (sheet 2 of 2)

address	register name	default value	R/W	description
P2:0xA2	DEM_V_SIZE_4MSB	0x04	RW	Bit[3:0]: dem_v_size[11:8] Image vertical size 4 MSB
P2:0xA3	DEM_V_SIZE_8LSB	0x48	RW	Bit[7:0]: dem_v_size[7:0] Image vertical size 8 LSB
P2:0xA4	DEM_H_START_4MSB	0x00	RW	Bit[3:0]: dem_h_start[11:8] Image horizontal start 4 MSB
P2:0xA5	DEM_H_START_8LSB	0x00	RW	Bit[7:0]: dem_h_start[7:0] Image horizontal start 8 LSB
P2:0xA6	DEM_H_SIZE_4MSB	0x07	RW	Bit[3:0]: dem_h_size[11:8] Image horizontal size 4 MSB
P2:0xA7	DEM_H_SIZE_8LSB	0x90	RW	Bit[7:0]: dem_h_size[7:0] Image horizontal size 8 LSB

4.3 test pattern

Test pattern and color bar are offered for testing purposes.

figure 4-3 test pattern diagram

table 4-3 test pattern registers

address	register name	default value	R/W	description
P1:0x0D	FRAME_EXP_SEPERATE_EN	0x00	RW	Bit[4]: frame_exp_seperate_en When enabled, frame length equals to value of register P1:{0x0E, 0x0F} 0: Disable 1: Enable Bit[1]: timing_test_en 0: Disable timing test mode 1: Enable timing test mode Bit[0]: test_en 0: Disable colorbar test 1: Enable colorbar test
P1:0x30	PATTERN_COL_CTRL0	0x07	RW	Bit[7:4]: pattern_col_start[10:8] Start cols of test pattern (in pixels) Bit[3:0]: pattern_col_size[10:8] Size of cols of test pattern (in pixels)
P1:0x3C	PATTERN_COL_START	0x00	RW	Bit[7:0]: pattern_col_start[7:0] Start cols of test pattern (in pixels)
P1:0x3D	PATTERN_COL_SIZE	0x98	RW	Bit[7:0]: pattern_col_size[7:0] Size of cols of test pattern (in pixels)

4.4 black level calibration (BLC)

The black level calibration (BLC) function is used to set the pixel out of a complete black object to a programmable pedestal value in all kinds of lightning conditions. Due to circuit offset and pixel dark current, the pixel output level of a black object is normally non-zero. The OS02F10 calibrates the black level of the active pixel by subtracting the true optical black pixel output.

The BLC is based on measuring the value at the center of the distribution of the optical black reference pixels and applying digital correction to bring the center to the target value. The center of the pixel distribution is estimated from a combination of median and average filtering. The filtering for the BLC is based on the middle 1024 columns of 8 optical dark rows. Only the values closest to the horizontal center of each row are used in order to minimize influence from any edge effects in the array.

During normal operation, dark current is expected to change slowly with time. During slow changes, the BLC in the OS02F10 will use multi frame iterative averaging statistics to allow for a more stable change. The frame number can be set by the register P1:0xFB[2:1].

table 4-4 BLC registers (sheet 1 of 4)

address	register name	default value	R/W	description
P1:0x22	CIS_DATA_EN	0x00	RW	Bit[1]: cis_data_rand_en Enable to add random number to output data of black level Bit[0]: cis_data_clamp_en Enable to limit maximum of output data of black level
P1:0x46	DC_LEVEL_LIMIT_EN	0xC0	RW	Enable to Limit Maximum of Corrected Statistical Value of Black Level
P1:0x47	DC_LEVEL_LIMIT	0x20	RW	Bit[7:0]: Maximum of corrected statistical value of black level
P1:0x48	BLC_DATA_LIMIT	0xC8	RW	Bit[7:0]: Maximum of output data of black level
P1:0x49	HIGHEST 2BITS OF DC_LEVEL AND BLC DATA	0x33	RW	Bit[5:4]: dc_level_limit[9:8] Bit[1:0]: blc_data_limit[9:8]
P1:0xC0	BLC_RPC_BLUE	0x00	RW	Bit[5:0]: rpc_gain for blue channel (-1x~1x) Accuracy is 1/32
P1:0xC1	BLC_RPC_RED	0x00	RW	Bit[5:0]: rpc_gain for red channel (-1x~1x) Accuracy is 1/32
P1:0xC2	BLC_RPC_GR	0x00	RW	Bit[5:0]: rpc_gain for Gr channel (-1x~1x) Accuracy is 1/32
P1:0xC3	BLC_RPC_GB	0x00	RW	Bit[5:0]: blc_gain for Gr Channel (-1x~1x) Accuracy is 1/32
P1:0xC4	BLC_EXP_BLUE	0x40	RW	Bit[7:0]: blc_gain for Blue channel (-4x~4x) Accuracy is 1/128
P1:0xC5	BLC_EXP_RED	0x40	RW	Bit[7:0]: blc_gain for red channel (-4x~4x) Accuracy is 1/128
P1:0xC6	BLC_EXP_GR	0x40	RW	Bit[7:0]: blc_gain for Gr channel (-4x~4x) Accuracy is 1/128
P1:0xC7	BLC_EXP_GB	0x40	RW	Bit[7:0]: blc_gain for Gr channel (-4x~4x) Accuracy is 1/128
P1:0xC8	BLC_EXP_CTL	0x00	RW	Bit[7:6]: blc_gain_blue[9:8] Bit[5:4]: blc_gain_red[9:8] Bit[3:2]: blc_gain_gr[9:8] Bit[1:0]: blc_gain_gr[9:8]
P1:0xC9	OTP_BLC_CTL	0x00	RW	Bit[1]: otp_blc_gain_en Bit[0]: otp_blc_exp_en
P1:0xCC	BLC_TRIG_EN	0xC0	RW	Enable Output of Corrected Statistical Value of Black Level

table 4-4 BLC registers (sheet 2 of 4)

address	register name	default value	R/W	description
P1:0xCD	BLC_GAIN_BLUE	0x80	RW	Bit[7:0]: blc_gain for blue channel (-2x~2x) Accuracy is 1/128
P1:0xCE	BLC_GAIN_RED	0x80	RW	Bit[7:0]: blc_gain for red channel (-2x~2x) Accuracy is 1/128
P1:0xCF	BLC_GAIN_GR	0x80	RW	Bit[7:0]: blc_gain for Gr channel (-2x~2x) Accuracy is 1/128
P1:0xD0	BLC_GAIN_GB	0x80	RW	Bit[7:0]: blc_gain for Gr channel (-2x~2x) Accuracy is 1/128
P1:0xD1	BLC_GAIN_CTL	0x00	RW	Bit[3]: blc_gain_blue[8] Bit[2]: blc_gain_red[8] Bit[1]: blc_gain_gr[8] Bit[0]: blc_gain_gr[8]
P1:0xD2	DARK_COL_ADDR_START	0x80	RW	Start Point of Column Address of Dark Pixels
P1:0xD3	DARK_SEL	0x0E	RW	Bit[3:2]: dark_col_sel 01: 256 pixels selected in every dark row 10: 512 pixels selected in every dark row 11: 1024 pixels selected in every dark row Bit[1]: dark_first_half_sel 0: Second half dark rows selected 1: First half dark rows selected Bit[0]: dark_half_en 0: All dark rows selected 1: Half dark rows selected
P1:0xF0	GB_SUBOFFSET	0x00	RW	Bit[7:0]: gb_suboffset[7:0] Low 8 bits of Gb channel black level offset Total register is 9 bits with MSB at P1:0xF8[7] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF1	BLUE_SUBOFFSET	0x00	RW	Bit[7:0]: blue_suboffset[7:0] Low 8 bits of blue channel black level offset Total register is 9 bits with MSB at P1:0xF8[6] (-256~255, 0x100~0x0FF) Highest bit is sign bit

table 4-4 BLC registers (sheet 3 of 4)

address	register name	default value	R/W	description
P1:0xF2	RED_SUBOFFSET	0x00	RW	Bit[7:0]: red_suboffset[7:0] Low 8 bits of red channel black level offset Total register is 9 bits with MSB at P1:0xF8[5] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF3	GR_SUBOFFSET	0x00	RW	Bit[7:0]: gr_suboffset[7:0] Low 8 bits of Gr channel black level offset Total register is 9 bits with MSB at P1:0xF8[4] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF4	GAIN_LIMIT	0x0C	RW	gain_limit
P1:0xF5	RSVD	–	–	Reserved
P1:0xF8	SUB_OFFSET_SIGN BITS	0x00	RW	Bit[7]: gb_suboffset[8] High bit of Gb channel black level offset, which is sign bit Bit[6]: blue_suboffset[8] High bit of blue channel black level offset, which is sign bit Bit[5]: red_suboffset[8] High bit of red channel black level offset, which is sign bit Bit[4]: gr_suboffset[8] High bit of Gr channel black level offset, which is sign bit Bit[3:2]: bl_position_set2 Black level position control for calibration Bit[1:0]: bl_position_set Black level position control for statistic
P1:0xFA	ABL_TRIGGER	0x00	RW	Bit[1]: Manual trigger

table 4-4 BLC registers (sheet 4 of 4)

address	register name	default value	R/W	description
P1:0xFB	ABL	0x00	RW	Bit[7]: blc_test_en 0: Low 10 bits output mode 1: High 10 bits output mode Bit[6]: blc_filter_en 0: Dark row median filter disable 1: Dark row median filter enable Bit[4]: blc_bpc_en 0: Dark row BPC disable 1: Dark row BPC enable Bit[3]: random_en Bit[2:1]: blc_mode 00: 1 frame average mode 01: 4 frames average mode 10: 8 frames average mode 11: 1 frame average mode Bit[0]: blc_en 0: Blacklevel disable 1: Blacklevel enable
P1:0xFC	BLC_BPC_TH_P_8LSB	0x40	RW	Bit[7:0]: blc_bpc_th_p[7:0] Blacklevel positive threshold for bad pixel, encoded in absolute value
P1:0xFE	BLC_BPC_TH_N_8LSB	0x40	RW	Bit[7:0]: blc_bpc_th_n[7:0] Blacklevel negative threshold for bad pixel, encoded in complement

4.5 defect pixel correction

Defective pixels will be detected and be replaced by a value calculated from the neighbor pixel during the bad pixel correction unit.

A defect pixel is a pixel which is black and not charged when light hits it and a zero value is read. These bad pixels will be detected and corrected.

In the defect pixel processing, according to the exposure time and the analog gain, it will be divided into four states (outdoor, normal, dummy, lowlight). Different DPC thresholds can be used in different states.

table 4-5 defect pixel registers (sheet 1 of 3)

address	register name	default value	R/W	description
P2:0x34	ISP_MODE	0xFF	RW	Bit[3]: demo_en demo_gf bypass enable 0: Disable demo_gf work 1: Enable demo_gf work
P2:0x5D	DPC_CTRL0	0x01	RW	Bit[4]: wbgain_position_set Wbgain position reverse 0: Disable wbgain_positionrevise 1: Enable wbgain_positionrevise Bit[1:0]: bayer_order Bayer RAW order 00: GBGB 01: BGBG 10: GRGR 11: RGRG
P2:0x60	LSC_DPC_EN	0x0F	RW	Bit[3]: DPC in dummy enable 0: Disable 1: Enable Bit[2]: DPC in outdoor enable 0: Disable 1: Enable Bit[1]: DPC in normal enable 0: Disable 1: Enable Bit[0]: DPC in low light enable 0: Disable 1: Enable
P2:0x62	ROW_START	0x01	RW	Bit[7:0]: row_start[7:0] Low 8 bits of starting point of row counting
P2:0x63	ROW_START	0x00	RW	Bit[3:0]: row_start[11:8] High 3 bits of starting point of row counting

table 4-5 defect pixel registers (sheet 2 of 3)

address	register name	default value	R/W	description
P2:0x98	DPC_MEDIA	0x00	RW	Bit[7]: DPC mean in dummy enable 0: Disable 1: Enable Bit[6]: DPC mean in outdoor enable 0: Disable 1: Enable Bit[5]: DPC mean in normal enable 0: Disable 1: Enable Bit[4]: DPC mean in lowlight enable 0: Disable 1: Enable Bit[3]: dpc_media in dummy enable 0: Disable 1: Enable Bit[2]: dpc_media in outdoor enable 0: Disable 1: Enable Bit[1]: dpc_media in normal enable 0: Disable 1: Enable Bit[0]: bpc_media in low light enable 0: Disable 1: Enable
P2:0x9B	FLAG_RATIO_VT	0x02	RW	DPC Flag Ratio Value
P2:0xA8	TEMP_SIF_EN	0x00	RW	Coordinate Move Along with ana_window Enable
P2:0xA9	TEMP_SIF_R_START _3MSB	0x00	RW	Bit[2:0]: temp_sif_r_start[10:8] High 3 bits of coordinate move of row start
P2:0xAA	TEMP_SIF_R_ START _8LSB	0x00	RW	Bit[7:0]: temp_sif_r_start[7:0] Low 8 bits of coordinate move of row start
P2:0xAB	TEMP_SIF_C_START _3MSB	0x00	RW	Bit[2:0]: temp_sif_c_start[10:8] High 3 bits of coordinate move of column start
P2:0xAC	TEMP_SIF_C_ START _8LSB	0x00	RW	Bit[7:0]: temp_sif_c_start[7:0] Low 8 bits of coordinate move of column start
P2:0xAD	TEMP_SIF_R_SIZE_ 3MSB	0x04	RW	Bit[2:0]: temp_sif_r_size[10:8] High 3 bits of coordinate move of row size
P2:0xAE	TEMP_SIF_R_SIZE_ 8LSB	0x48	RW	Bit[7:0]: temp_sif_r_size[7:0] Low 8 bits of coordinate move of row size

table 4-5 defect pixel registers (sheet 3 of 3)

address	register name	default value	R/W	description
P2:0xAF	TEMP_SIF_C_SIZE_ 3MSB	0x07	RW	Bit[2:0]: temp_sif_c_size[10:8] High 3 bits of coordinate move of column size
P2:0xB0	TEMP_SIF_C_SIZE_ 8LSB	0x90	RW	Bit[7:0]: temp_sif_c_size[7:0] Low 8 bits of coordinate move of column size
P3:0xC0	DP_POS_EN	0x00	RW	OTP Send DPIX Coordinate Enable 0: Disable OTP send DPIX coordinate 1: Enable OTP send DPIX coordinate
P4:0x12	ISP_REGF_12	0x00	RW	dpc_vt_eff Bad Decision Threshold Used to Generate Proportion Bit[5:4]: Bright pixel threshold ratio (weak point coefficient Bit[2:0]: Dark pixel threshold ratio
P4:0x19	ISP_REGF_19	0x10	RW	dpc_dif_thr_outdoor DPC grad difference threshold in outdoor
P4:0x1A	ISP_REGF_1A	0x10	RW	dpc_dif_thr_nr DPC grad difference threshold in normal
P4:0x1B	ISP_REGF_1B	0x10	RW	dpc_dif_thr_dummy DPC grad difference threshold in dummy
P4:0x1C	ISP_REGF_1C	0x10	RW	dpc_dif_thr_low DPC grad difference threshold in lowlight
P4:0x1D	ISP_REGF_1D	0x10	RW	dpc_grad_thr_outdoor DPC edge grad threshold in outdoor
P4:0x1E	ISP_REGF_1E	0x10	RW	dpc_grad_thr_nr DPC edge grad threshold in normal
P4:0x1F	ISP_REGF_1F	0x10	RW	dpc_grad_thr_dummy DPC edge grad threshold in dummy
P4:0x20	ISP_REGF_20	0x10	RW	dpc_grad_thr_low DPC edge grad threshold in lowlight

4.6 digital gain/analog gain

Channel digital gain can be controlled by DG_Gr, DG_Gb, DG_R, and DG_B. Each digital gain can be configured from a gain of 0 to 2.

Global digital gain can be controlled from a gain of 1 to 32.

Analog gain can be obtained by adjusting the ramp's slope using the pga_gain_ctl register. Analog gain can be configured from a gain of 1 to 16. Analog gain is updated by register of exp_rpc_en(P1:0x01). P1:0x01 should be set to 0x01 after configuring analog gain.

table 4-6 digital gain/analog gain registers

address	register name	default value	R/W	description
P1:0x23	RPC1	–	R	PGA Gain Control Low 8 Bits Corresponding to register P1:0x24
P1:0x24	PGA_GAIN_CTL[7:0]	0x20	RW	PGA Gain Manual Control Low 8 Bits Entire PGA gain control is P1:{0x38[0], 0x24} (1x~31x, 0x000~0x1FF)
P1:0x31	RESOLUTION_ SELECTION	0x00	RW	Resolution Selection 0x00: 1936x1096 0x01: ana_window 0x04: 968x548 0x10: 1944x1136
P1:0x38	PGA_GAIN1_MSB8	0x00	RW	Bit[0]: Long pga_gain[8] PGA gain control
P1:0x39	DIG_GAIN_BUF	0x08	RW	Global Digital Gain (1x~32x) 0x08 equals to 1x 0xFF equals to 32x Accuracy is 1/8
P1:0x40	R_GAIN_BUF	0x80	RW	Digital Gain, Red Channel (1~2x) 0x80 equals to 1x 0xFF equals to 2x Accuracy is 1/128
P1:0x41	GR_GAIN_BUF	0x80	RW	Digital Gain, Gr Channel (1~2x) 0x80 equals to 1x 0xFF equals to 2x Accuracy is 1/128
P1:0x42	GB_GAIN_BUF	0x80	RW	Digital Gain, Gb Channel (1~2x) 0x80 equals to 1x 0xFF equals to 2x Accuracy is 1/128
P1:0x43	B_GAIN_BUF	0x80	RW	Digital Gain, Blue Channel (1~2x) 0x80 equals to 1x 0xFF equals to 2x Accuracy is 1/128

4.7 exposure control

The OS02F10 exposure time can be set manually using registers:

Minimum exposure is one line.

{P1:0x03[7:0], P1:0x04[7:0]} for exposure time

All exposure time values are represented by unit of row time:

row time = HTS / row clock

The exposure control can adjust the line time through the HBLANK ({P1:0x09, P1:0x0A}) register where row clock is the system clock and HTS is the horizontal total size. It can be read by {P1:0x8C, P1:0x8D}).

It can adjust the line time through the VBLANK ({P1:0x05, P1:0x06}) register by changing the frame rate after confirmed resolution.

The length of the frame can be determined by reading the register frame_length_readonly ({P1:0x4E, P1:0x4F}).

In full size, v_sub mode: frame length is the readout value of frame_length_readonly ({P1:0x4E, P1:0x4F}).

In binning and VGA mode, actual frame length is double the read value of frame_length_readonly ({P1:0x4E, P1:0x4F}).

Exposure time/VBLANK/HBLANK is updated by register exp_rpc_en (P1:0x01). P1:0x01 should be set to 0x01 after configuring the exposure time/VBLANK/HBLANK.

table 4-7 exposure control registers

address	register name	default value	R/W	description
P1:0x01	EXP_RPC_EN	0x00	RW	Enable of Frame Sync Signal 0: Disable 1: Enable
P1:0x03	BUF_EXP_8MSB	0x00	RW	Exposure Time in “H” Unit 1~65535 (0x0001~0xFFFF)
P1:0x04	BUF_EXP_8LSB	0x9A	RW	Exposure Time in “H” Unit 1~65535 (0x0001~0xFFFF)
P1:0x08	VPOS_BLANK	0x01	RW	Time Width Between Posedge of VSYNC and Posedge of First HSYNC in “H” Unit
P1:0x09	HBLANK_4MSB	0x00	RW	Bit[3:0]: Horizontal blank[11:8] in “timer_clk” unit 0~4095 (0x000~0xFFF)
P1:0x0A	HBLANK_8LSB	0x00	RW	Bit[3:0]: Horizontal blank[7:0] in “timer_clk” Unit 0~4095 (0x000~0xFFF)
P1:0x23	RPC1	–	R	PGA Gain Control Low 8 Bits Corresponding to register P1:0x24
P1:0x3A	VDELAY_BUF_8MSB	0x00	RW	Bit[7:0]: Vertical blank[15:8] in “H” unit
P1:0x3B	VDELAY_BUF_8LSB	0x00	RW	Bit[7:0]: Vertical blank[7:0] in “H” unit

5 OTP memory

The OS02F10 has a total 128 bytes of OTP memory. Using the auto load function, data in OTP memory is written to registers when sensor is powered up (e.g., temperature calibration data).

5.1 OTP memory map

The OTP usage is designed to be as shown in **table 5-1**

table 5-1 OTP batch buffer registers (sheet 1 of 3)

address	register name	default value	R/W	description
P4:0x00	FLAG_LOAD0	0x00	RW	Bit[5]: flag_load0 Block 5 programmed flag 0: Block 5 is empty 1: Block 5 is programmed Bit[4]: flag_load0 Block 4 programmed flag 0: Block 4 is empty 1: Block 4 is programmed Bit[3]: flag_load0 Block 3 programmed flag 0: Block 3 is empty 1: Block 3 is programmed Bit[2]: flag_load0 Block 2 programmed flag 0: Block 2 is empty 1: Block 2 is programmed Bit[1]: flag_load0 Block 1 programmed flag 0: Block 1 is empty 1: Block 1 is programmed Bit[0]: flag_load0 Block 0 programmed flag 0: Block 0 is empty 1: Block 0 is programmed
P4:0x01	FLAG_LOAD1	0x00	RW	Reserved Flag Register
P4:0x02	LINE_CODE	0x00	RW	Production Identification
P4:0x03	LOT_YEAR_MONTH	0x00	RW	Production Identification lot_year and lot_month
P4:0x04	LOT_DAY	0x00	RW	Production Identification lot_day
P4:0x05	LOT_SNUM	0x00	RW	Production Identification lot_snum
P4:0x06	WAFER_ID	0x00	RW	Production Identification wafer_id
P4:0x07	WAFER_X	0x00	RW	Production Identification wafer_x
P4:0x08	WAFER_Y	0x00	RW	Production Identification wafer_y
P4:0x09	OTP_R_GAIN	0x80	RW	User Register 1 Reserved register for user
P4:0x0A	OTP_B_GAIN	0x80	RW	User Register 2 Reserved register for user

table 5-1 OTP batch buffer registers (sheet 2 of 3)

address	register name	default value	R/W	description
P4:0x0B	OTP_GR_GAIN	0x80	RW	User Register 3 Reserved register for user
P4:0x0C	OTP_GB_GAIN	0x80	RW	User Register 4 Reserved register for user
P4:0x0D	USER_RSV_01	0x00	RW	User Register 5 Reserved register for user
P4:0x0E	USER_RSV_02	0x00	RW	User Register 6 Reserved register for user
P4:0x0F	USER_RSV_03	0x00	RW	User Register 7 Reserved register for user
P4:0x10	USER_RSV_04	0x00	RW	User Register 8 Reserved register for user
P4:0x11	USER_RSV_05	0x00	RW	User Register 9 Reserved register for user
P4:0x12	ISP_REGF_12	0x00	RW	12th Byte Data in Batch Operation Mode
P4:0x13	ISP_REGF_13	0x00	RW	13th Byte Data in Batch Operation Mode
P4:0x14	ISP_REGF_14	0x14	RW	14th Byte Data in Batch Operation Mode
P4:0x15	ISP_REGF_15	0x46	RW	15th Byte Data in Batch Operation Mode
P4:0x16	ISP_REGF_16	0x46	RW	16th Byte Data in Batch Operation Mode
P4:0x17	ISP_REGF_17	0x46	RW	17th Byte Data in Batch Operation Mode
P4:0x18	ISP_REGF_18	0x46	RW	18th Byte Data in Batch Operation Mode
P4:0x19	ISP_REGF_19	0x10	RW	19th Byte Data in Batch Operation Mode
P4:0x1A	ISP_REGF_1A	0x10	RW	1A Byte Data in Batch Operation Mode
P4:0x1B	ISP_REGF_1B	0x10	RW	1B Byte Data in Batch Operation Mode
P4:0x1C	ISP_REGF_1C	0x10	RW	1C Byte Data in Batch Operation Mode
P4:0x1D	ISP_REGF_1D	0x10	RW	1D Byte Data in Batch Operation Mode
P4:0x1E	ISP_REGF_1E	0x10	RW	1E Byte Data in Batch Operation Mode
P4:0x1F	ISP_REGF_1F	0x10	RW	1F Byte Data in Batch Operation Mode
P4:0x20	ISP_REGF_20	0x10	RW	20th Byte Data in Batch Operation Mode
P4:0x21	ISP_REGF_21	0x46	RW	21st Byte Data in Batch Operation Mode
P4:0x22	ISP_REGF_22	0x46	RW	22nd Byte Data in Batch Operation Mode
P4:0x23	ISP_REGF_23	0x46	RW	23rd Byte Data in Batch Operation Mode
P4:0x24	ISP_REGF_24	0x46	RW	24th Byte Data in Batch Operation Mode

table 5-1 OTP batch buffer registers (sheet 3 of 3)

address	register name	default value	R/W	description
P4:0x25	ISP_REGF_25	0x3C	RW	25th Byte Data in Batch Operation Mode
P4:0x26	ISP_REGF_26	0x3C	RW	26th Byte Data in Batch Operation Mode
P4:0x27	ISP_REGF_27	0x3C	RW	27th Byte Data in Batch Operation Mode
P4:0x28	ISP_REGF_28	0x3C	RW	28th Byte Data in Batch Operation Mode
P4:0x29	ISP_REGF_29	0x3C	RW	29th Byte Data in Batch Operation Mode
P4:0x2A	ISP_REGF_2A	0x3C	RW	2A Byte Data in Batch Operation Mode
P4:0x2B	ISP_REGF_2B	0x3C	RW	2B Byte Data in Batch Operation Mode
P4:0x2C	ISP_REGF_2C	0x3C	RW	2C Byte Data in Batch Operation Mode
P4:0x2D	ISP_REGF_2D	0x0A	RW	2D Byte Data in Batch Operation Mode
P4:0x2E	ISP_REGF_2E	0x0A	RW	2E Byte Data in Batch Operation Mode
P4:0x2F	ISP_REGF_2F	0x0A	RW	2F Byte Data in Batch Operation Mode
P4:0x30	ISP_REGF_30	0x0A	RW	30th Byte Data in Batch Operation Mode
P4:0x31	ISP_REGF_31	0x32	RW	31st Byte Data in Batch Operation Mode
P4:0x32	ISP_REGF_32	0x32	RW	32nd Byte Data in Batch Operation Mode
P4:0x33	ISP_REGF_33	0x32	RW	33rd Byte Data in Batch Operation Mode
P4:0x34	ISP_REGF_34	0x32	RW	34th Byte Data in Batch Operation Mode
P4:0x35	ISP_REGF_35	0x20	RW	35th Byte Data in Batch Operation Mode
P4:0x36	ISP_REGF_36	0x20	RW	36th Byte Data in Batch Operation Mode
P4:0x37	ISP_REGF_37	0x20	RW	37th Byte Data in Batch Operation Mode
P4:0x38	ISP_REGF_38	0x20	RW	38th Byte Data in Batch Operation Mode
P4:0x39	ISP_REGF_39	0x00	RW	39th Byte Data in Batch Operation Mode
P4:0x3A	ISP_REGF_3A	0xFF	RW	3A Byte Data in Batch Operation Mode
P4:0x3B	ISP_REGF_3B	0x44	RW	3B Byte Data in Batch Operation Mode
P4:0x3C	ISP_REGF_3C	0x0A	RW	3C Byte Data in Batch Operation Mode
P4:0x3D	ISP_REGF_3D	0x0A	RW	3D Byte Data in Batch Operation Mode
P4:0x3E	ISP_REGF_3E	0x0A	RW	3E Byte Data in Batch Operation Mode
P4:0x3F	ISP_REGF_3F	0x0A	RW	3F Byte Data in Batch Operation Mode

6 register tables

The following tables provide descriptions of the device control registers contained in the OS02F10. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x7A for write and 0x7B for read (when I2CID=0, 0x78 for write and 0x79 for read).

6.1 clock [P0:0x2E - P0:0x30, P0:0x32 - P0:0x35]

table 6-1 clock registers (sheet 1 of 2)

address	register name	default value	R/W	description
P0:0x2E	PLL_NC_BUF	0x0C	RW	Bit[7]: Not used Bit[6:0]: pll_nc_buf [PLL input*(pll_nc+3)*2/(pll_mc+1)] Note: Parameters of registers will be enabled in next frame.
P0:0x2F	PLL_CTRL_BUF	0x3C	RW	Bit[7]: pll_clk_sel 0: Disable bypass PLL 1: Enable bypass PLL Bit[6:2]: Not used Bit[1:0]: pll_mc [PLL input*(pll_nc+3)*2/(pll_mc+1)] Note: Parameters of registers will be enabled in next frame.
P0:0x30	CLK_MODE_BUF	0x20	RW	Bit[7:6]: Not used Bit[5]: cis_clk_ctrl 0: timer_clk = pclk_pre 1: timer_clk = pclk_pre/2 Bit[4]: pclk_ctrl 0: pclk_pre = pll_timer_clk 1: pclk_pre = pll_timer_clk/2 Bit[3:1]: Not used Bit[0]: isp_clk_ctrl 0: dclk = timer_clk 1: dclk = timer_clk/2
P0:0x32	ROW_CLK_CTRL_BUF	0x02	RW	Bit[7:2]: Not used Bit[1:0]: row_clk_ctrl 00: row_clk = dac_clk/2 01: row_clk = dac_clk/4 10: row_clk = dac_clk/8 11: Not used

table 6-1 clock registers (sheet 2 of 2)

address	register name	default value	R/W	description
P0:0x33	CLK_MODE_CTRL	0x04	RW	Bit[7:4]: Not used Bit[3]: pclk_gating_en_buf 0: Disable PCLK gating 1: Enable PCLK gating Bit[2]: pclk_inv_buf 0: Disable PCLK reverse 1: Enable PCLK reverse Bit[1]: cnt_clk_inv_en_buf 0: Disable cnt_clk reverse 1: Enable cnt_clk reverse Bit[0]: dac_clk_mode_buf 0: dac_clk = cnt_clk 1: dac_clk = cnt_clk/2 Note: Parameters of registers will be enabled in next frame.
P0:0x34	PLL_DIV_CTL	0x71	RW	Bit[7]: Not used Bit[6:5]: pll_div_pcp Bit[4:3]: pll_div_ncp Bit[2:0]: pll_div_dac_buf PLL frequency divider control PLL output = CLK * (pll_nc + 3) / (pll_mc + 1) / (2.5 + pll_div_dac * 0.5) Note: Parameters of registers will be enabled in next frame.
P0:0x35	PLL_CTL	0x00	RW	Bit[7:4]: pll_bias_ctl PLL chargepump current control 000: 5 u 001: 10u (default) 010: 15u 011: 20u 100: 25u 101: 30u (default) 110: 35u 111: 40u Bit[3:2]: pll_dctl Choose PLL's PFD delay time to remove dead zone 00: 478p (default) 01: 932p 10: 1.334n 11: 1.736n Bit[1:0]: Not used

6.2 soft reset [P0:0x20]

table 6-2 soft reset register

address	register name	default value	R/W	description
P0:0x20	SOFT_RST	0x01	RW	Soft Reset Signal Register cannot be set to self clear 0: Enable soft reset 1: Disable soft reset

6.3 power down [P0:0x36 - P0:0x37]

table 6-3 power down registers

address	register name	default value	R/W	description
P0:0x36	PWD_PLL	0x00	RW	Power Down Control of PLL 0: Disable power down of PLL 1: Enable power down of PLL
P0:0x37	PWD_ASP	0x00	RW	Power Down Control of ASP 0: Disable power down of ASP 1: Enable power down of ASP

6.4 DVP port [P0:0x1B, P0:0x1D, P0:0x40]

table 6-4 DVP port registers (sheet 1 of 2)

address	register name	default value	R/W	description
P0:0x1B	IO_PAD_CTRL	0x1F	RW	Pad Dataout[7:0] Output Enable Signal Bit[7:6]: Not used Bit[5]: vsync_ie_buf Pad VSYNC input enable signal 0: Disable input 1: Enable input Bit[4]: strobe_oe_buf Pad strobe output enable signal 0: Enable output 1: Disable output Bit[3]: out_envsync_buf Pad VSYNC output enable signal 0: Enable output 1: Disable output Bit[2]: out_enhsync_buf Pad HSYNC output enable signal 0: Enable output 1: Disable output Bit[1]: out_enp_buf Pad PCLK output enable signal 0: Enable output 1: Disable output Bit[0]: out_end_buf 0: Enable output 1: Disable output Note: Parameters of registers will be enabled in next frame
P0:0x1D	STROBE_VSYNC_EN _BUF	0x00	RW	Bit[7:1]: Not used Bit[0]: strobe_vsync_en_buf 0: Strobe is output from strobe pad 1: VSYNC is output from strobe pad Note: Parameters of registers will be enabled in next frame.

table 6-4 DVP port registers (sheet 2 of 2)

address	register name	default value	R/W	description
P0:0x40	EXT_SYNC_EN	0x00	RW	Bit[7:2]: Not used Bit[1]: ext_sync_mst_en Enable master mode of external sync function 0: OS02F10 is slave of external sync 1: OS02F10 is master of external sync Bit[0]: ext_sync_en Enable signal of external sync function 0: Disable external sync 1: Enable external sync

6.5 SCCB [P0:0x50 - P0:0x51]

table 6-5 SCCB registers

address	register name	default value	R/W	description
P0:0x50	SCCB_DEV_ADDR_EN	0x00	RW	sccb_dev_addr Enable Signal 0: Disable sccb_dev_addr 1: Enable sccb_dev_addr
P0:0x51	SCCB_DEV_ADDR	0x3D	RW	Manual SCCB Device Address

6.6 other [P0:0x02 - P0:0x04, P0:0xE7, P0:0xFD]

table 6-6 other registers (sheet 1 of 2)

address	register name	default value	R/W	description
P0:0x02	CHIP_ID	0x24	R	chip_id
P0:0x03	CHIP_ID	0x08	R	chip_id
P0:0x04	ECO_VER	0x01	RW	Version of ECO

table 6-6 other registers (sheet 2 of 2)

address	register name	default value	R/W	description
P0:0xE7	REG_UPDATE	0x00	RW	Bit[7:2]: Not used Bit[1]: reg_update_mode Bit[0]: reg_update_cmd Control register to take effect immediately
P0:0xFD	PAGE_FLG	0x00	RW	Bit[7:3]: Not used Bit[2:0]: page_flg Page number

6.7 resolution, exposure, and analog gain [P1:0x01, P1:0x03 - P1:0x3F]

table 6-7 resolution, exposure, and analog gain registers (sheet 1 of 2)

address	register name	default value	R/W	description
P1:0x01	EXP_RPC_EN	0x00	RW	Enable of Frame Sync Signal 0: Disable 1: Enable
P1:0x03	BUF_EXP_8MSB	0x00	RW	Exposure Time in “H” Unit 1~65535 (0x0001~0xFFFF)
P1:0x04	BUF_EXP_8LSB	0x9A	RW	Exposure Time in “H” Unit 1~65535 (0x0001~0xFFFF)
P1:0x05~ P1:0x22	NOT USED	–	–	Not Used
P1:0x23	RPC1	–	R	PGA Gain Control Low 8 Bits Corresponding to register P1:0x24
P1:0x24	PGA_GAIN_CTL	0x20	RW	PGA Gain Manual Control Low 8 Bits Entire PGA gain control is P1:{0x38[0], 0x24} (1x~31x, 0x000~0x1FF)
P1:0x25~ P1:0x30	NOT USED	–	–	Not Used
P1:0x31	RESOLUTION_ SELECTION	0x00	RW	Resolution Selection 0x00: 1936x1096 0x01: ana_window 0x04: 968x548 0x10: 1944x1136
P1:0x32~ P1:0x37	NOT USED	–	–	Not Used

table 6-7 resolution, exposure, and analog gain registers (sheet 2 of 2)

address	register name	default value	R/W	description
P1:0x38	PGA_GAIN1_MSB8	0x00	RW	Bit[7:1]: Not used Bit[0]: Long pga_gain[8] PGA gain control
P1:0x39~ P1:0x3E	NOT USED	–	–	Not Used
P1:0x3F	MIRROR/FLIP	0x00	RW	Bit[7:2]: Not used Bit[1]: Vertical upside down Bit[0]: Horizontal mirror 0x00: Normal (no flip) 0x01: Horizontal flip 0x02: Vertical flip 0x03: Both horizontal and vertical flip

6.8 ana_window [P1:0x28, P1:0x34 - P1:0x37, P1:0x4A - P1:0x4D]

table 6-8 ana_window registers (sheet 1 of 2)

address	register name	default value	R/W	description
P1:0x28	ANA_V_DUMMY_ SIZE	0x10	RW	Number of Dummy Rows in ANA Window
P1:0x34	COL_ANA_ADDR_ START_3MSB	0x01	RW	Bit[7:3]: Not used Bit[2:0]: col_ana_addr_start[10:8] Half of number of columns that are not selected in 1936 columns
P1:0x35	COL_ANA_ADDR_ START_8LSB	0x44	RW	Bit[7:0]: col_ana_addr_start[7:0] Half of number of columns that are not selected in 1936 columns
P1:0x36	COL_ANA_ADDR_ SIZE_3MSB	0x05	RW	Bit[7:3]: Not used Bit[2:0]: col_ana_addr_size[10:8] Number of columns for ANA window
P1:0x37	COL_ANA_ADDR_ SIZE_8LSB	0x08	RW	Bit[7:0]: col_ana_addr_size[7:0] Number of columns for ANA window
P1:0x4A	ROW_ANA_ADDR_ START_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: row_ana_addr_start[10:8] Half of number of rows that are not selected in 1096 lines
P1:0x4B	ROW_ANA_ADDR_ START_8LSB	0xA8	RW	Bit[7:0]: row_ana_addr_start[7:0] Half of number of rows that are not selected in 1096 lines

table 6-8 ana_window registers (sheet 2 of 2)

address	register name	default value	R/W	description
P1:0x4C	ROW_ANA_ADDR_SIZE_3MSB	0x02	RW	Bit[7:3]: Not used Bit[2:0]: row_ana_addr_size[10:8] Number of rows for ANA window
P1:0x4D	ROW_ANA_ADDR_SIZE_8LSB	0xD8	RW	Bit[7:0]: row_ana_addr_size[7:0] Number of rows for ANA window

6.9 digital gain [P1:0x39 - P1:0x43]

table 6-9 digital gain registers

address	register name	default value	R/W	description
P1:0x39	DIG_GAIN_BUF	0x08	RW	Global Digital Gain (1x~32x) 0x08 equals to 1x 0xFF equals to 32x Accuracy is 1/8
P1:0x40	R_GAIN_BUF	0x80	RW	Digital Gain, Red Channel (1~2x) 0x80 equals to 1x 0xFF equals to 2x Accuracy is 1/128
P1:0x41	GR_GAIN_BUF	0x80	RW	Digital Gain, Gr Channel (1~2x) 0x80 equals to 1x 0xFF equals to 2x Accuracy is 1/128
P1:0x42	GB_GAIN_BUF	0x80	RW	Digital Gain, Gb Channel (1~2x) 0x80 equals to 1x 0xFF equals to 2x Accuracy is 1/128
P1:0x43	B_GAIN_BUF	0x80	RW	Digital Gain, Blue Channel (1~2x) 0x80 equals to 1x 0xFF equals to 2x Accuracy is 1/128

6.10 frame_length and row_length [P1:0x05 - P1:0x0F, P1:0x30 - P1:0x8D]

table 6-10 frame_length and row_length registers (sheet 1 of 2)

address	register name	default value	R/W	description
P1:0x05	VBLANK_BUF_8MSB	0x00	RW	Bit[7:0]: Vertical blank[15:8] in “H” unit 0~65535 (0x0000~0xFFFF)
P1:0x06	VBLANK_BUF_8LSB	0x00	RW	Bit[7:0]: Vertical blank[7:0] in “H” unit 0~65535 (0x0000~0xFFFF)
P1:0x08	VPOS_BLANK	0x01	RW	Time Width Between Posedge of VSYNC and Posedge of First HSYNC in “H” Unit
P1:0x09	HBLANK_4MSB	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Horizontal blank[11:8] in “timer_clk” unit 0~4095 (0x000~0xFFF)
P1:0x0A	HBLANK_8LSB	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Horizontal blank[7:0] in “timer_clk” Unit 0~4095 (0x000~0xFFF)
P1:0x0D	FRAME_EXP_ SEPERATE_EN	0x00	RW	Bit[7:5]: Not used Bit[4]: frame_exp_seperate_en When enabled, frame length equals to value of register P1:{0x0E, 0x0F} 0: Disable 1: Enable Bit[3:2]: Not used Bit[1]: timing_test_en 0: Disable timing test mode 1: Enable timing test mode Bit[0]: test_en 0: Disable colorbar test 1: Enable colorbar test
P1:0x0E	FRAME_LENGTH_NUM_ 8MSB	0x04	RW	Bit[7:0]: Frame length for manual frame length setting[15:8] Used with P1:0x0D[4] enabled
P1:0x0F	FRAME_LENGTH_NUM_ 8MSB	0x50	RW	Bit[7:0]: Frame length for manual frame length setting[7:0] Used with P1:0x0D[4] enabled
P1:0x30	PATTERN_COL_CTRL0	0x07	RW	Bit[7:4]: pattern_col_start[10:8] Start cols of test pattern (in pixels) Bit[3:0]: pattern_col_size[10:8] Size of cols of test pattern (in pixels)

table 6-10 frame_length and row_length registers (sheet 2 of 2)

address	register name	default value	R/W	description
P1:0x31~ P1:0x39	NOT USED	–	–	Not Used
P1:0x3A	VDELAY_BUF_8MSB	0x00	RW	Bit[7:0]: Vertical blank[15:8] in “H” unit
P1:0x3B	VDELAY_BUF_8LSB	0x00	RW	Bit[7:0]: Vertical blank[7:0] in “H” unit
P1:0x3C	PATTERN_COL_CTRL1	0x00	RW	Bit[7:0]: Pattern_col_start[7:0] Start cols of test pattern (in pixels)
P1:0x3D	PATTERN_COL_CTRL2	0x98	RW	Bit[7:0]: Pattern_col_size[7:0] Size of cols of test pattern (in pixels)
P1:0x4E	FRAME_LENGTH_ READONLY_8MSB	–	R	Bit[7:0]: Frame length[15:8] in “H” unit
P1:0x4F	FRAME_LENGTH_ READONLY_8LSB	–	R	Bit[7:0]: Frame length[7:0] in “H” unit
P1:0x50~ P1:0x8B	NOT USED	–	–	Not Used
P1:0x8C	HS_PERIOD_NUM_5MSB	–	R	Bit[7:5]: Not used Bit[4:0]: Row length[12:8] in “timer_clk” unit
P1:0x8D	HS_PERIOD_NUM_8LSB	–	R	Bit[7:0]: Row length[7:0] in “timer_clk” unit

6.11 BLC [P1:0x22, P1:0x46 - P1:0x49, P1:0xC0 - P1:0xDF, P1:0xF0 - P1:0xFE]

table 6-11 BLC registers (sheet 1 of 5)

address	register name	default value	R/W	description
P1:0x22	CIS_DATA_EN	0x00	RW	Bit[7:2]: Not used Bit[1]: cis_data_rand_en Enable to add random number to output data of black level Bit[0]: cis_data_clamp_en Enable to limit maximum of output data of black level
P1:0x46	DC_LEVEL_LIMIT_EN	0xC0	RW	Enable to Limit Maximum of Corrected Statistical Value of Black Level

table 6-11 BLC registers (sheet 2 of 5)

address	register name	default value	R/W	description
P1:0x47	DC_LEVEL_LIMIT	0x20	RW	Bit[7:0]: Maximum of corrected statistical value of black level
P1:0x48	BLC_DATA_LIMIT	0xC8	RW	Bit[7:0]: Maximum of output data of black level
P1:0x49	HIGHEST 2BITS OF DC_LEVEL AND BLC DATA	0x33	RW	Bit[7:6]: Not used Bit[5:4]: dc_level_limit[9:8] Bit[3:2]: Not used Bit[1:0]: blc_data_limit[9:8]
P1:0xC0	BLC_RPC_BLUE	0x00	RW	Bit[7:6]: Not used Bit[5:0]: rpc_gain for blue channel (-1x~1x) Accuracy is 1/32
P1:0xC1	BLC_RPC_RED	0x00	RW	Bit[7:6]: Not used Bit[5:0]: rpc_gain for red channel (-1x~1x) Accuracy is 1/32
P1:0xC2	BLC_RPC_GR	0x00	RW	Bit[7:6]: Not used Bit[5:0]: rpc_gain for Gr channel (-1x~1x) Accuracy is 1/32
P1:0xC3	BLC_RPC_GB	0x00	RW	Bit[7:6]: Not used Bit[5:0]: blc_gain for Gr Channel (-1x~1x) Accuracy is 1/32
P1:0xC4	BLC_EXP_BLUE	0x40	RW	Bit[7:0]: blc_gain for Blue channel (-4x~4x) Accuracy is 1/128
P1:0xC5	BLC_EXP_RED	0x40	RW	Bit[7:0]: blc_gain for red channel (-4x~4x) Accuracy is 1/128
P1:0xC6	BLC_EXP_GR	0x40	RW	Bit[7:0]: blc_gain for Gr channel (-4x~4x) Accuracy is 1/128
P1:0xC7	BLC_EXP_GB	0x40	RW	Bit[7:0]: blc_gain for Gr channel (-4x~4x) Accuracy is 1/128
P1:0xC8	BLC_EXP_CTL	0x00	RW	Bit[7:6]: blc_gain_blue[9:8] Bit[5:4]: blc_gain_red[9:8] Bit[3:2]: blc_gain_gr[9:8] Bit[1:0]: blc_gain_gr[9:8]
P1:0xC9	OTP_BLC_CTL	0x00	RW	Bit[7:2]: Not used Bit[1]: otp_blc_gain_en Bit[0]: otp_blc_exp_en
P1:0xCA~ P1:0xCB	NOT USED	–	–	Not Used
P1:0xCC	BLC_TRIG_EN	0xC0	RW	Enable Output of Corrected Statistical Value of Black Level

table 6-11 BLC registers (sheet 3 of 5)

address	register name	default value	R/W	description
P1:0xCD	BLC_GAIN_BLUE	0x80	RW	Bit[7:0]: blc_gain for blue channel (-2x~2x) Accuracy is 1/128
P1:0xCE	BLC_GAIN_RED	0x80	RW	Bit[7:0]: blc_gain for red channel (-2x~2x) Accuracy is 1/128
P1:0xCF	BLC_GAIN_GR	0x80	RW	Bit[7:0]: blc_gain for Gr channel (-2x~2x) Accuracy is 1/128
P1:0xD0	BLC_GAIN_GB	0x80	RW	Bit[7:0]: blc_gain for Gr channel (-2x~2x) Accuracy is 1/128
P1:0xD1	BLC_GAIN_CTL	0x00	RW	Bit[7:4]: Not used Bit[3]: blc_gain_blue[8] Bit[2]: blc_gain_red[8] Bit[1]: blc_gain_gr[8] Bit[0]: blc_gain_gr[8]
P1:0xD2	DARK_COL_ADDR_START	0x80	RW	Start Point of Column Address of Dark Pixels
P1:0xD3	DARK_SEL	0x0E	RW	Bit[7:4]: Not used Bit[3:2]: dark_col_sel 00: Not used 01: 256 pixels selected in every dark row 10: 512 pixels selected in every dark row 11: 1024 pixels selected in every dark row Bit[1]: dark_first_half_sel 0: Second half dark rows selected 1: First half dark rows selected Bit[0]: dark_half_en 0: All dark rows selected 1: Half dark rows selected
P1:0xD4~ P1:0xDF	NOT USED	–	–	Not Used
P1:0xF0	GB_SUBOFFSET	0x00	RW	Bit[7:0]: gb_suboffset[7:0] Low 8 bits of Gb channel black level offset Total register is 9 bits with MSB at P1:0xF8[7] (-256~255, 0x100~0x0FF) Highest bit is sign bit

table 6-11 BLC registers (sheet 4 of 5)

address	register name	default value	R/W	description
P1:0xF1	BLUE_SUBOFFSET	0x00	RW	Bit[7:0]: blue_suboffset[7:0] Low 8 bits of blue channel black level offset Total register is 9 bits with MSB at P1:0xF8[6] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF2	RED_SUBOFFSET	0x00	RW	Bit[7:0]: red_suboffset[7:0] Low 8 bits of red channel black level offset Total register is 9 bits with MSB at P1:0xF8[5] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF3	GR_SUBOFFSET	0x00	RW	Bit[7:0]: gr_suboffset[7:0] Low 8 bits of Gr channel black level offset Total register is 9 bits with MSB at P1:0xF8[4] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF4	GAIN_LIMIT	0x0C	RW	gain_limit
P1:0xF5	RSVD	–	–	Reserved
P1:0xF6~ P1:0xF7	NOT USED	–	–	Not Used
P1:0xF8	SUB_OFFSET_ SIGNBITS	0x00	RW	Bit[7]: gb_suboffset[8] High bit of Gb channel black level offset, which is sign bit Bit[6]: blue_suboffset[8] High bit of blue channel black level offset, which is sign bit Bit[5]: red_suboffset[8] High bit of red channel black level offset, which is sign bit Bit[4]: gr_suboffset[8] High bit of Gr channel black level offset, which is sign bit Bit[3:2]: bl_position_set2 Black level position control for calibration Bit[1:0]: bl_position_set Black level position control for statistic
P1:0xF9	NOT USED	–	–	Not Used

table 6-11 BLC registers (sheet 5 of 5)

address	register name	default value	R/W	description
P1:0xFA	ABL_TRIGGER	0x00	RW	Bit[7:2]: Not used Bit[1]: Manual trigger Bit[0]: Not used
P1:0xFB	ABL	0x00	RW	Bit[7]: blc_test_en 0: Low 10 bits output mode 1: High 10 bits output mode Bit[6]: blc_filter_en 0: Dark row median filter disable 1: Dark row median filter enable Bit[5]: Not used Bit[4]: blc_bpc_en 0: Dark row BPC disable 1: Dark row BPC enable Bit[3]: random_en Bit[2:1]: blc_mode 00: 1 frame average mode 01: 4 frames average mode 10: 8 frames average mode 11: 1 frame average mode Bit[0]: blc_en 0: Blacklevel disable 1: Blacklevel enable
P1:0xFC	BLC_BPC_TH_P_8LSB	0x40	RW	Bit[7:0]: blc_bpc_th_p[7:0] Blacklevel positive threshold for bad pixel, encoded in absolute value
P1:0xFD	NOT USED	–	–	Not Used
P1:0xFE	BLC_BPC_TH_N_8LSB	0x40	RW	Bit[7:0]: blc_bpc_th_n[7:0] Blacklevel negative threshold for bad pixel, encoded in complement

6.12 dual sensor synchronization [P1:0x0B - P1:0x0C, P1:0x17, P1:0x1B]

table 6-12 dual sensor synchronization registers

address	register name	default value	R/W	description
P1:0x0B	EXTER_SYNC_CTL	0x00	RW	External Frame Synchronize Control Signal Bit[7]: Not used Bit[6]: exter_frame_num_x256_en When enabled, 1 LSB of exter_sync_frame_num (P1:0x17) equals 256 frames 0: Disable 1: Enable Bit[5]: exter_del_en 0: Disable 1: Enable Bit[4]: exter_sync_manual_en Configure a POS in this bit to trigger a sync output in master mode Bit[3]: exter_sync_auto_en Sensor in master mode will send sync signal every exter_sync_frame_num (P1:0x17) frames automatically 0: Disable 1: Enable Bit[2]: Not used Bit[1]: External sync slave mode 0: Disable 1: Enable Bit[0]: External sync master mode 0: Disable 1: Enable
P1:0x0C	EXTER_SYNC_OUT_WIDTH	0x08	RW	Width of Sync Signal Output When Sensor is Configured as Master in “dac_clk” Unit
P1:0x17	EXTER_SYNC_FRAME_NUM	0x0A	RW	Interval Frame Number of Auto External Frame Synchronize Pulse
P1:0x1B	ROW_SYNC_MASTER	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Row_sync_master

6.13 timing control [P1:0x11 - P1:0x1A, P1:0x1C, P1:0x44 - P1:0x8B]

table 6-13 timing control registers (sheet 1 of 5)

address	register name	default value	R/W	description
P1:0x11	TIMING_CTRL0	0x18	RW	Bit[7:4]: dac_floor Dac_floor is [16, 240], step is 16 scnt_num = rst_num1 + 1024 + floor Bit[3:0]: Rst_num1 Rst_num1 is [16, 240], step is 16 rcnt_num = rst_num1 * 2, scnt_num = rst_num1 + 1024 + floor
P1:0x12	DAC_FOLD	0x00	RW	Bit[7:2]: Not used Bit[1:0]: dac_fold 00: No fold 01: Second fold 10: Fourth fold 11: Not used
P1:0x13	VLOWSE_CTL1	0x21	RW	Bit[7:4]: vlowse_x2 Bit[3:0]: vlowse_x1
P1:0x14	VLOWSE_CTL2	0x84	RW	Bit[7:4]: vlowse_x8 Bit[3:0]: vlowse_x4
P1:0x15	NOT USED	–	–	Not Used
P1:0x16	TIMING_CTRL1	0x68	RW	Bit[7]: rch_inv_sel 0: Disable to exchange TGA and TGB 1: Exchange TGA and TGB Bit[6]: sc2_timing_sel 0: SC2 is high all time 1: Normal work mode Bit[5]: dac_timing_sel Enable switch mode in bias of DAC Bit[4]: col_addr_blank_sel Control address in hblank Bit[3]: fpn_33ms_data_en 0: Row address is 2047 in vblank 1: Row address is 0 in vblank Bit[2:0]: fpn_33ms_timing_sel Control timing in vertical blank region
P1:0x17~ P1:0x19	NOT USED	–	–	Not Used

table 6-13 timing control registers (sheet 2 of 5)

address	register name	default value	R/W	description
P1:0x1A	TIMING_SEL	0xBB	RW	Bit[7]: timing_no_wait_en 0: Wait to col address to end 1: No wait to col address to end Bit[6]: extra_reset_en Enable double shutter Bit[5]: image_lag_test Enable image lag test timing mode Bit[4]: ref_timing_sel Enable switch mode in VREF of PLDO Bit[3]: pcp_timing_sel Enable switch mode in VREF of PCP Bit[2]: col_en1_timing_sel Bit[1]: col_en2_timing_sel 0: No col_en2 1: Normal Bit[0]: rs_timing_sel
P1:0x1C	TIMING_CTRL2	0x0A	RW	Bit[7]: rowsel_off_en Bit[6]: analog_test_en Bit[5]: col_boost_rst Bit[4]: col_boost_sig Bit[3]: dark23_timing_sel Control Tx in BLC rows Bit[2]: rowsel_timing_sel Control mode of rowsel Bit[1]: nb_timing_sel Enable switch mode in pixel bias Bit[0]: col_test_tx 0: Normal 1: Turn off Tx for test
P1:0x44	SCNT_DDS_3MSB	0x03	RW	scnt_dds_2msb
P1:0x45	SCNT_DDS_8LSB	0x00	RW	scnt_dds_8lsb
P1:0x46~ P1:0x4F	NOT USED	–	–	Not Used
P1:0x50	P0	0x02	RW	P0 Cycle for Pixel Timing (row_clk Unit)
P1:0x51	P1	0x20	RW	P1 Cycle for Pixel Timing (row_clk Unit)
P1:0x52	P2	0x20	RW	P2 Cycle for Pixel Timing (row_clk Unit)
P1:0x53	P3	0x00	RW	P3 Cycle for Pixel Timing (row_clk Unit)
P1:0x54	NOT USED	–	–	Not Used
P1:0x55	P5	0x10	RW	P5 Cycle for Pixel Timing (row_clk Unit)
P1:0x56	P6	0x02	RW	P6 Cycle for Pixel Timing (row_clk Unit)
P1:0x57	P7	0x20	RW	P7 Cycle for Pixel Timing (row_clk Unit)

table 6-13 timing control registers (sheet 3 of 5)

address	register name	default value	R/W	description
P1:0x58	P8	0x01	RW	P8 Cycle for Pixel Timing (row_clk Unit)
P1:0x59	P9	0x04	RW	P9 Cycle for Pixel Timing (row_clk Unit)
P1:0x5A	P10	0x0A	RW	P10 Cycle for Pixel Timing (row_clk Unit)
P1:0x5B	P11_4MSB	0x01	RW	P11 Cycle for Pixel Timing (row_clk Unit)
P1:0x5C	P11_8LSB	0x20	RW	P11 Cycle for Pixel Timing (row_clk Unit)
P1:0x5D	P12	0x10	RW	P12 Cycle for Pixel Timing (row_clk Unit)
P1:0x5E	P13	0x00	RW	P13 Cycle for Pixel Timing (row_clk Unit)
P1:0x5F	P14	0x02	RW	P14 Cycle for Pixel Timing (row_clk Unit)
P1:0x60	NOT USED	–	–	Not Used
P1:0x61	P15	0x26	RW	P15 Cycle for Pixel Timing (row_clk Unit)
P1:0x62	P16	0x03	RW	P16 Cycle for Pixel Timing (row_clk Unit)
P1:0x63	P17	0x13	RW	P17 Cycle for Pixel Timing (row_clk Unit)
P1:0x64	P18	0x23	RW	P18 Cycle for Pixel Timing (row_clk Unit)
P1:0x65	P19	0x00	RW	P19 Cycle for Pixel Timing (row_clk Unit)
P1:0x66	P20	0x2A	RW	P20 Cycle for Pixel Timing (row_clk Unit)
P1:0x67	P21	0x00	RW	P21 Cycle for Pixel Timing (row_clk Unit)
P1:0x68	P22	0x26	RW	P22 Cycle for Pixel Timing (row_clk Unit)
P1:0x69	P23	0x10	RW	P23 Cycle for Pixel Timing (row_clk Unit)
P1:0x6A	P24	0x08	RW	P24 Cycle for Pixel Timing (row_clk Unit)
P1:0x6B	P25	0x00	RW	P25 Cycle for Pixel Timing (row_clk Unit)
P1:0x6C	P26	0x00	RW	P26 Cycle for Pixel Timing (row_clk Unit)
P1:0x6D	P27	0x02	RW	P27 Cycle for Pixel Timing (row_clk Unit)
P1:0x6E	P28	0x20	RW	P28 Cycle for Pixel Timing (row_clk Unit)
P1:0x6F	P29	0x20	RW	P29 Cycle for Pixel Timing (row_clk Unit)
P1:0x70	P30	0x10	RW	P30 Cycle for Pixel Timing (row_clk Unit)
P1:0x71	P31	0x30	RW	P31 Cycle for Pixel Timing (row_clk Unit)
P1:0x72	P32	0x05	RW	P32 Cycle for Pixel Timing (row_clk Unit)
P1:0x73	P33	0x2A	RW	P33 Cycle for Pixel Timing (row_clk Unit)
P1:0x74	P34	0x05	RW	P34 Cycle for Pixel Timing (row_clk Unit)

table 6-13 timing control registers (sheet 4 of 5)

address	register name	default value	R/W	description
P1:0x75	P35/36	0x4F	RW	Bit[7:4]: P35 cycle for pixel timing (row_clk unit) Bit[3:0]: P36 cycle for pixel timing (row_clk unit)
P1:0x76	P37/P38	0xEF	RW	Bit[7:4]: P37 cycle for pixel timing (row_clk unit) Bit[3:0]: p38 cycle for pixel timing (row_clk unit)
P1:0x77	P39/P40	0x46	RW	Bit[7:4]: P39 cycle for pixel timing (row_clk unit) Bit[3:0]: P40 cycle for pixel timing (row_clk unit)
P1:0x78	P41	0x02	RW	P41 Cycle for Pixel Timing (row_clk Unit)
P1:0x79	P42_4MSB	0x00	RW	P42 Cycle for Pixel Timing (row_clk Unit)
P1:0x7A	P42_8LSB	0x02	RW	P42 Cycle for Pixel Timing (row_clk Unit)
P1:0x7B	P43	0x00	RW	P43 Cycle for Pixel Timing (row_clk Unit)
P1:0x7C	P44	0x20	RW	P44 Cycle for Pixel Timing (row_clk Unit)
P1:0x7D	NOT USED	–	–	Not Used
P1:0x7E	P46	0x05	RW	P46 Cycle for Pixel Timing (row_clk Unit)
P1:0x7F	P47	0x00	RW	P47 Cycle for Pixel Timing (row_clk Unit)
P1:0x80	P48	0x10	RW	P48 Cycle for Pixel Timing (row_clk Unit)
P1:0x81	P49	0x10	RW	P49 Cycle for Pixel Timing (row_clk Unit)
P1:0x82	P50/P51	0x1F	RW	Bit[7:4]: P50 cycle for pixel timing (row_clk unit) Bit[3:0]: P51 cycle for pixel timing (row_clk unit)
P1:0x83	P54/P52	0x00	RW	Bit[7:4]: P54 cycle for pixel timing (row_clk unit) Bit[3:0]: P52 cycle for pixel timing (row_clk unit)
P1:0x84	P53	0x04	RW	P53 Cycle for Pixel Timing (row_clk Unit)
P1:0x85	P55_8LSB	0x20	RW	P55 Cycle for Pixel Timing (row_clk Unit)
P1:0x86	P58/P56	0x00	RW	Bit[7:4]: P58 Bit[3:0]: P56
P1:0x87	P55_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: p55_3msb

table 6-13 timing control registers (sheet 5 of 5)

address	register name	default value	R/W	description
P1:0x88~ P1:0x89	NOT USED	–	–	Not Used
P1:0x8A	RH/RL	0x44	RW	Timing Parameter of pixel_bias_ctrl Bit[7]: Not used Bit[6:4]: RH Bit[3]: Not used Bit[2:0]: RL
P1:0x8B	SH/SL	0x44	RW	Timing Parameter of pixel_bias_ctrl Bit[7]: Not used Bit[6:4]: SH Bit[3]: Not used Bit[2:0]: SL

6.14 delete name function [P1:0x18]

table 6-14 delete name function register

address	register name	default value	R/W	description
P1:0x18	DEL_FRAME_CTRL	0x40	RW	Bit[7:6]: del_frame_num Control frame number to be deleted when resolution switching or pwd recovery Bit[5]: switch_del_frame_en Control function for deleting bad frames when resolution switches 0: Disable 1: Enable Bit[4]: pwd_del_frame_en Control function for deleting bad frames when pwd recovery 0: Disable 1: Enable Bit[3]: Not used Bit[2]: updown_del_en Control function for deleting bad frames when updown enable 0: Disable 1: Enable Bit[1]: rst_del_en When enabled, sensor will delete first synchronized frame 0: Disable 1: Enable Bit[0]: rst_colrow_en Sensor column and row reset control 0: Disable 1: Enable

6.15 analog control [P1:0x19, P1:0x1D - P1:0x20, P1:0x25 - P1:0x2F, P1:0xE7]

table 6-15 analog control registers (sheet 1 of 2)

address	register name	default value	R/W	description
P1:0x19	ICOMP	0xA1	RW	Bit[7:4]: Icomp1 Control first stage comparator bias current Bit[3]: Not used Bit[2:0]: Icomp2 Control second stage comparator bias current
P1:0x1D	VBL	0x36	RW	Bit[7:4]: VBL1 Bit[3:0]: VBL2
P1:0x1E	ANA_CTRL0	0x00	RW	Bit[7:5]: test_sel Bit[4]: bin_en_c Bit[3]: bin_en_m Bit[2]: rst_pbuas_boost Bit[1]: sig_pbias_boost Bit[0]: bwi_timing_sel
P1:0x1F	ANA_CTRL1	0x23	RW	Bit[7]: Not used Bit[6]: sc1_sel Bit[5]: p625_sel Bit[4]: gain_sel Bit[3]: gain_test_en Bit[2]: cas_hi_en Bit[1]: en_dac Enable inner DAC Bit[0]: dac_bias_x2 Control current of DAC bias
P1:0x20	VNCP_SEL	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: vncp_sel Control voltage of NCP output
P1:0x25	ANA_CTRL2	0x05	RW	Bit[7:4]: Not used Bit[3]: bl_test_en Bit[2]: Bl_en Sunspot replace enable Bit[1:0]: vref2_sel Control voltage of vref2
P1:0x26	PCP	0x36	RW	Bit[7]: Not used Bit[6:5]: pcp_clkdrv_sel Bit[4]: pcp_clkdrv_en Bit[3:0]: pcp_sel

table 6-15 analog control registers (sheet 2 of 2)

address	register name	default value	R/W	description
P1:0x27	ANA_CTRL3	0x06	RW	Bit[7:5]: Not used Bit[4]: col_bin_avg_en Enable average of 2 columns in binning mode Bit[3:2]: adout_mode Control DDS mode of counter Bit[1]: adout_mode_sel Enable exchange of two DDS mode for two channels Bit[0]: Not used
P1:0x28	NOT USED	–	–	Not Used
P1:0x29	NCP	0x2B	RW	Bit[7:6]: Not used Bit[5:4]: ncp_m_sel Bit[3:2]: ncp_mode Bit[1:0]: ncp_num
P1:0x2A	ADC_RANGE_CTL	0x04	RW	Bit[7:3]: Not used Bit[2:0]: adc_range_ctl Control range of ADC
P1:0x2B	ANA_CTRL4	0x92	RW	Bit[7:6]: pvdd_sel, Bit[5]: sa_mode Bit[4:2]: sa_irst_ctl Control current of SA Bit[1:0]: sa_pw1_ctl Control width of pulse PW1 in SA
P1:0x2C	ANA_CTRL5	0x00	RW	Bit[7:4]: Not used Bit[3]: adc_high_8bit Enable 10-bit output Bit[2:0]: cntclk_delay Control delay of counter clock
P1:0x2D	NOT USED	–	–	Not Used
P1:0x2E	ANA_CTRL6	0x00	RW	Bit[7:6]: Not used Bit[5:3]: dclk_delay Control delay of DCLK Bit[2:0]: saclk_delay Control delay of SACLK
P1:0x2F	ANA_CTRL7	0x00	RW	Bit[7]: Not used Bit[6:4]: colenclk_delay Control delay of COLENCLK Bit[3:0]: pclk_delay
P1:0xE7	REG_UPDATE	0x00	RW	Bit[7:2]: Not used Bit[1]: reg_update_mode Bit[0]: reg_update_cmd Control register to take effect immediately

6.16 MIPI [P1:0x8E - P1:0x98, P1:0x9C - P1:0x9D, P1:0xA0 - P1:0xB6]

table 6-16 MIPI registers (sheet 1 of 3)

address	register name	default value	R/W	description
P1:0x8E	H_SIZE_MIPI_4MSB	0x07	RW	MIPI Column Number
P1:0x8F	H_SIZE_MIPI_8LSB	0x90	RW	MIPI Column Number
P1:0x90	V_SIZE_MIPI_3MSB	0x04	RW	MIPI Line Number
P1:0x91	V_SIZE_MIPI_8LSB	0x48	RW	MIPI Line Number
P1:0x92	HS_CLK_CTRL	0x00	RW	Bit[7:3]: Not used Bit[2]: hs_mode_vf 0: MIPI clock switch per line 1: MIPI clock switch per frame Bit[1]: hs_mode 0: MIPI clock burst mode 1: MIPI clock switch mode Bit[0]: p_denh
P1:0x93	R_CLK_POST	0x0E	RW	Clock Lane Post Time Control
P1:0x94	R_LPX	0x77	RW	Bit[7:4]: Clock lane LPX time control Bit[3:0]: Data lane LPX time control
P1:0x95	R_PREPARE	0x56	RW	Bit[7:4]: Clock lane prepare time control Bit[3:0]: Data lane prepare time control
P1:0x96	R_HS_ZERO	0x1A	RW	Data Lane Zero Time Control
P1:0x97	DATA ID	0x2B	RW	Bit[7:6]: Not used Bit[5:0]: Data type sel 0x2A: RAW8 0x2B: RAW10
P1:0x98	LANE_TRAIL	0x78	RW	Bit[7:4]: Clock lane trail time control Bit[3:0]: Data lane trail time control
P1:0x9C	R_CLK_ZERO	0x22	RW	Clock Lane Zero Time Control
P1:0x9D	HS_LEV	0xC5	RW	Hs_lev
P1:0xA0	HS_PHASE	0x05	RW	Hs_phase
P1:0xA1	MIPI_CTRL0	0x03	RW	Bit[7:5]: Not used Bit[4:3]: MIPI FS packet to LS packet time control Bit[2:0]: MIPI transmission speed select
P1:0xA2	R_INIT_M	0x0B	RW	MIPI Initial Time Control Bit
P1:0xA3	R_INIT_L	0x40	RW	MIPI Initial Time Control Bit

table 6-16 MIPI registers (sheet 2 of 3)

address	register name	default value	R/W	description
P1:0xA4	MIPI_CTRL1	0x10	RW	Bit[7:6]: Not used Bit[5:2]: R_exit Data lane exit time control Bit[1:0]: MIPI wake up time control bit 17~16
P1:0xA5	R_WAKEUP_M	0x86	RW	MIPI Wake Up Time Control Bit
P1:0xA6	R_WAKEUP_L	0x88	RW	MIPI Wake Up Time Control Bit
P1:0xA7	DC_TEST_LP_LK	0x3F	RW	MIPI Output Control When MIPI Work in MIPI DC Test Mode Bit[7]: MIPI clock output control 0: MIPI clock pad output in LP state 1: MIPI clock pad output in HS state Bit[6]: MIPI data output control 0: MIPI clock pad output in LP state 1: MIPI clock pad output in HS state Bit[5:4]: MIPI CKP/CKN voltage control Bit[3:2]: MIPI D0P/D0N voltage control Bit[1:0]: MIPI D1P/D1N voltage control
P1:0xA8	DC_TEST_DATA_HS	0xFF	RW	MIPI Output Control When MIPI Work in MIPI DC Test Mode
P1:0xA9~ P1:0xAD	NOT USED	–	–	Not Used
P1:0xAE	FRAME_END_DLY	0x65	RW	Bit[7:0]: frame_end_dly[7:0] Time control between long packet and fe packet low byte
P1:0xAF	FRAME_END_DLY	0x00	RW	Bit[7:0]: frame_end_dly[15:8] Time control between long packet and fe packet high byte
P1:0xB0	NOT USED	–	–	Not Used
P1:0xB1	MIPI_PHY_EN	0x00	RW	Bit[7:2]: Not used Bit[1]: mipi_en 0: MIPI disable 1: MIPI enable Bit[0]: MIPI PHY shutdown control 0: MIPI DPHY shutdown 1: Enable DPHY
P1:0xB2	MIPI_HSYNC_NUM	0x96	RW	MIPI Line Sync Packet Start Time Control
P1:0xB3	MIPI_PLL_NC	0x1D	RW	MIPI PLL NC Control

table 6-16 MIPI registers (sheet 3 of 3)

address	register name	default value	R/W	description
P1:0xB4	MIPI_CTRL2	0x0D	RW	Bit[7:6]: Not used Bit[5:3]: mipi_pll_bias Bit[2:0]: vcm_ctl
P1:0xB5	MIPI_CTRL3	0x16	RW	Bit[7:6]: Not used Bit[5:2]: mpll_div Bit[1:0]: mipi_dctl
P1:0xB6	MIPI_CTRL4	0x00	RW	Bit[7]: Not used Bit[6]: pause_ck 0: MIPI DC test disable 1: MIPI DC test enable Bit[5]: ls_mode 0: MIPI line sync disable 1: MIPI line sync enable Bit[4]: MIPI output pad control 0: MIPI output pad tri-stated when MIPI is not working 1: MIPI output pad driving ground when MIPI is not working Bit[3]: MIPI initial mode enable 0: MIPI work in normal mode 1: MIPI work in initial mode Bit[2]: MIPI ULP mode enable 0: MIPI work in normal mode 1: MIPI work in ULP mode Bit[1]: FBSEL Bit[0]: Test mode MIPI test color bar 0: MIPI output ISP image 1: Not used

6.17 state [P2:0x05, P2:0x10 - P2:0x19, P2:0x20]

table 6-17 state registers (sheet 1 of 2)

address	register name	default value	R/W	description
P2:0x05	FIX_STATE	0x00	RW	Bit[7:5]: Not used Bit[4]: fix_state_en Fix state enable 0: Disable fix state 1: Enable fix state Bit[3]: Not used Bit[2:0]: fix_state_mode Fix which mode of state

table 6-17 state registers (sheet 2 of 2)

address	register name	default value	R/W	description
P2:0x10	EXP_NR_OUTD_8HSB	0x00	RW	Bit[7:0]: exp_nr_outd[15:8] Exposure threshold high 8 bits from normal into outdoor
P2:0x11	EXP_NR_OUTD_8LSB	0x8B	RW	Bit[7:0]: exp_nr_outd[7:0] Exposure threshold low 8 bits from normal into outdoor
P2:0x12	EXP_OUTD_NR_8HSB	0x00	RW	Bit[7:0]: exp_outd_nr[15:8] Exposure threshold high 8 bits from outdoor into normal
P2:0x13	EXP_OUTD_NR_8LSB	0x8D	RW	Bit[7:0]: exp_outd_nr[7:0] Exposure threshold low 8 bits from outdoor into normal
P2:0x14	EXP_HEQ_DUMMY_8HSM	0x04	RW	Bit[7:0]: exp_heq_dummy[15:8] Exposure threshold high 8 bits between normal and dummy
P2:0x15	EXP_HEQ_DUMMY_8LSM	0x60	RW	Bit[7:0]: exp_heq_dummy[7:0] Exposure threshold low 8 bits between normal and dummy
P2:0x16	EXP_HEQ_LOW_8HSM	0x04	RW	Bit[7:0]: exp_heq_low[15:8] Exposure threshold high 8 bits between normal and lowlight
P2:0x17	EXP_HEQ_LOW_8LSM	0x60	RW	Bit[7:0]: exp_heq_low[7:0] Exposure threshold low 8 bits between normal and lowlight
P2:0x18	RPC_HEQ_LOW_8LSM	0xC0	RW	Bit[7:0]: rpc_heq_low[7:0] RPC threshold low 8 bits between normal and lowlight
P2:0x19	RPC_HEQ_DUMMY_8LSM	0x80	RW	Bit[7:0]: rpc_heq_dummy[7:0] RPC threshold low 8 bits between normal and dummy
P2:0x20	RPC_HEQ	0x00	RW	Bit[7:2]: Not used Bit[1]: rpc_heq_low[8] RPC threshold high bit between normal and lowlight Bit[0]: rpc_heq_dummy[8] RPC threshold high bit between normal and dummy

6.18 package [P2:0x35 - P2:0x36]

table 6-18 package registers

address	register name	default value	R/W	description
P2:0x35	OUTMODE1	0x00	RW	Bit[7:6]: Not used Bit[5]: unpro_raw_out_en Unprocessed RAW output enable 0: Disable unprocessed RAW 1: Enable unprocessed RAW Bit[4:0]: Not used
P2:0x36	OUTMODE2	0x00	RW	Bit[7:4]: Not used Bit[3]: VSYNC inversion Bit[2]: HSYNC inversion Bit[1:0]: Not used

6.19 memory [P2:0x5E]

table 6-19 memory register

address	register name	default value	R/W	description
P2:0x5E	MEM_CTRL0	0x07	RW	Bit[7:2]: Not used Bit[1]: auto_first_en Auto br_frst enable whatever updown or mirror 0: Disable auto Br first 1: Enable auto Br first Bit[0]: br_first Output B/R first or G first 0: Gb/Gr first output 1: B/R first output

6.20 dpc_media [P2:0x98 - P2:0x9A, P4:0x12]

table 6-20 dpc_media registers

address	register name	default value	R/W	description
P2:0x98	DPC_MEDIA	0x00	RW	Bit[7:4]: Not used Bit[3]: dpc_media in dummy enable 0: Disable 1: Enable Bit[2]: dpc_media in outdoor enable 0: Disable 1: Enable Bit[1]: dpc_media in normal enable 0: Disable 1: Enable Bit[0]: dpc_media in low light enable 0: Disable 1: Enable
P2:0x99	DARK_THR	0xC4	RW	Brightness Mean Threshold
P2:0x9A	WHITE_THR	0xC4	RW	White Defect Pixel Threshold
P4:0x12	DPC_VT_EFF	0x00	RW	Bad Decision Threshold Used to Generate Proportion Bit[7:6]: Not used Bit[5:4]: Bright pixel threshold ratio (weak point coefficient) Bit[3]: Not used Bit[2:0]: Dark pixel threshold ratio

6.21 DPC [P2:0x34, P2:0x5D, P2:0x60 - P2:0x63, P2:0x98 - P3:0xC0, P4:0x12 - P4:0x20]

table 6-21 DPC registers (sheet 1 of 5)

address	register name	default value	R/W	description
P2:0x34	ISP_MODE	0xFF	RW	Bit[7:4]: Not used Bit[3]: demo_en demo_gf bypass enable 0: Disable demo_gf work 1: Enable demo_gf work Bit[2:0]: Not used

table 6-21 DPC registers (sheet 2 of 5)

address	register name	default value	R/W	description
P2:0x5D	DPC_CTRL0	0x01	RW	Bit[7:5]: Not used Bit[4]: wbgain_position_set Wbgain position reverse 0: Disable wbgain_positionrevise 1: Enable wbgain_positionrevise Bit[3:2]: Not used Bit[1:0]: bayer_order Bayer RAW order 00: GBGB 01: BGBG 10: GRGR 11: RGRG
P2:0x60	LSC_DPC_EN	0x0F	RW	Bit[7:4]: Not used Bit[3]: DPC in dummy enable 0: Disable 1: Enable Bit[2]: DPC in outdoor enable 0: Disable 1: Enable Bit[1]: DPC in normal enable 0: Disable 1: Enable Bit[0]: DPC in low light enable 0: Disable 1: Enable
P2:0x61	NOT USED	–	–	Not Used
P2:0x62	ROW_START	0x01	RW	Bit[7:0]: row_start[7:0] Low 8 bits of starting point of row counting
P2:0x63	ROW_START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: row_start[11:8] High 3 bits of starting point of row counting

table 6-21 DPC registers (sheet 3 of 5)

address	register name	default value	R/W	description
P2:0x98	DPC_MEDIA	0x00	RW	Bit[7]: DPC mean in dummy enable 0: Disable 1: Enable Bit[6]: DPC mean in outdoor enable 0: Disable 1: Enable Bit[5]: DPC mean in normal enable 0: Disable 1: Enable Bit[4]: DPC mean in lowlight enable 0: Disable 1: Enable Bit[3]: dpc_media in dummy enable 0: Disable 1: Enable Bit[2]: dpc_media in outdoor enable 0: Disable 1: Enable Bit[1]: dpc_media in normal enable 0: Disable 1: Enable Bit[0]: bpc_media in low light enable 0: Disable 1: Enable
P2:0x99~ P2:0x9A	NOT USED	–	–	Not Used
P2:0x9B	FLAG_RATIO_VT	0x02	RW	DPC Flag Ratio Value
P2:0x9C~ P2:0xA7	NOT USED	–	–	Not Used
P2:0xA8	TEMP_SIF_EN	0x00	RW	Coordinate Move Along with ana_window Enable
P2:0xA9	TEMP_SIF_R_START_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: temp_sif_r_start[10:8] High 3 bits of coordinate move of row start
P2:0xAA	TEMP_SIF_R_ START _8LSB	0x00	RW	Bit[7:0]: temp_sif_r_start[7:0] Low 8 bits of coordinate move of row start
P2:0xAB	TEMP_SIF_C_START_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: temp_sif_c_start[10:8] High 3 bits of coordinate move of column start
P2:0xAC	TEMP_SIF_C_ START _8LSB	0x00	RW	Bit[7:0]: temp_sif_c_start[7:0] Low 8 bits of coordinate move of column start

table 6-21 DPC registers (sheet 4 of 5)

address	register name	default value	R/W	description
P2:0xAD	TEMP_SIF_R_SIZE_3MSB	0x04	RW	Bit[7:3]: Not used Bit[2:0]: temp_sif_r_size[10:8] High 3 bits of coordinate move of row size
P2:0xAE	TEMP_SIF_R_SIZE_8LSB	0x48	RW	Bit[7:0]: temp_sif_r_size[7:0] Low 8 bits of coordinate move of row size
P2:0xAF	TEMP_SIF_C_SIZE_3MSB	0x07	RW	Bit[7:3]: Not used Bit[2:0]: temp_sif_c_size[10:8] High 3 bits of coordinate move of column size
P2:0xB0	TEMP_SIF_C_SIZE_8LSB	0x90	RW	Bit[7:0]: temp_sif_c_size[7:0] Low 8 bits of coordinate move of column size
P2:0xB1~ P2:0xBF	NOT USED	–	–	Not Used
P3:0xC0	DP_POS_EN	0x00	RW	OTP Send DPIX Coordinate Enable 0: Disable OTP send DPIX coordinate 1: Enable OTP send DPIX coordinate
P4:0x12	ISP_REGF_12	0x00	RW	dpc_vt_eff Bad Decision Threshold Used to Generate Proportion Bit[7:6]: Not used Bit[5:4]: Bright pixel threshold ratio (weak point coefficient Bit[3]: Not used Bit[2:0]: Dark pixel threshold ratio
P4:0x13~ P4:0x18	NOT USED	–	–	Not Used
P4:0x19	ISP_REGF_19	0x10	RW	dpc_dif_thr_outdoor DPC grad difference threshold in outdoor
P4:0x1A	ISP_REGF_1A	0x10	RW	dpc_dif_thr_nr DPC grad difference threshold in normal
P4:0x1B	ISP_REGF_1B	0x10	RW	dpc_dif_thr_dummy DPC grad difference threshold in dummy
P4:0x1C	ISP_REGF_1C	0x10	RW	dpc_dif_thr_low DPC grad difference threshold in lowlight
P4:0x1D	ISP_REGF_1D	0x10	RW	dpc_grad_thr_outdoor DPC edge grad threshold in outdoor

table 6-21 DPC registers (sheet 5 of 5)

address	register name	default value	R/W	description
P4:0x1E	ISP_REGF_1E	0x10	RW	dpc_grad_thr_nr DPC edge grad threshold in normal
P4:0x1F	ISP_REGF_1F	0x10	RW	dpc_grad_thr_dummy DPC edge grad threshold in dummy
P4:0x20	ISP_REGF_20	0x10	RW	dpc_grad_thr_low DPC edge grad threshold in lowlight

6.22 demo_sif [P2:0xA0 - P2:0xA7, P2:0xD0 - P2:0xD4, P2:0xF9 - P2:0xFA]

table 6-22 demo_sif registers (sheet 1 of 2)

address	register name	default value	R/W	description
P2:0xA0	DEM_V_START_4MSB	0x00	RW	Bit[7:4]: Not used Bit[3:0]: dem_v_start[11:8] image vertical start 4 MSB
P2:0xA1	DEM_V_START_8LSB	0x00	RW	Bit[7:0]: dem_v_start[7:0] Image vertical start 8 LSB
P2:0xA2	DEM_V_SIZE_4MSB	0x04	RW	Bit[7:4]: Not used Bit[3:0]: dem_v_size[11:8] Image vertical size 4 MSB
P2:0xA3	DEM_V_SIZE_8LSB	0x48	RW	Bit[7:0]: dem_v_size[7:0] Image vertical size 8 LSB
P2:0xA4	DEM_H_START_4MSB	0x00	RW	Bit[7:4]: Not used Bit[3:0]: dem_h_start[11:8] Image horizontal start 4 MSB
P2:0xA5	DEM_H_START_8LSB	0x00	RW	Bit[7:0]: dem_h_start[7:0] Image horizontal start 8 LSB
P2:0xA6	DEM_H_SIZE_4MSB	0x07	RW	Bit[7:4]: Not used Bit[3:0]: dem_h_size[11:8] Image horizontal size 4 MSB
P2:0xA7	DEM_H_SIZE_8LSB	0x90	RW	Bit[7:0]: dem_h_size[7:0] Image horizontal size 8 LSB
P2:0xD0	RAW_R_OFFSET_8LSB	0x00	RW	Bit[7:0]: raw_r_offset[7:0] Offset add on R channel
P2:0xD1	RAW_B_OFFSET_8LSB	0x00	RW	Bit[7:0]: raw_b_offset[7:0] Offset add on B channel

table 6-22 demo_sif registers (sheet 2 of 2)

address	register name	default value	R/W	description
P2:0xD2	RAW_GR_OFFSET_8LSB	0x00	RW	Bit[7:0]: raw_gr_offset[7:0] Offset add on Gr channel
P2:0xD3	RAW_GB_OFFSET_8LSB	0x00	RW	Bit[7:0]: raw_gb_offset[7:0] Offset add on Gb channel
P2:0xD4	RAW_OFFSET_2MSB	0x00	RW	Bit[7:6]: raw_r_offset[9:8] Offset add on Gb channel Bit[5:4]: raw_r_offset[9:8] Offset add on Gb channel Bit[3:2]: raw_gr_offset[9:8] Offset add on Gb channel Bit[1:0]: raw_gb_offset[9:8] Offset add on Gb channel
P2:0xF9	DC	0x00	RW	Bit[7:6]: Not used Bit[5]: dc_test_en Bit[4:2]: dc_mist_set Bit[1:0]: dc_data_set[1:0]
P2:0xFA	DC_DATA_SET_H8	0x00	RW	Bit[7:0]: dc_data_set[9:2]

6.23 OTP IP interface [P3:0xE0 - P3:0xE6]

table 6-23 OTP IP interface registers

address	register name	default value	R/W	description
P3:0xE0	TPGM	0xF5	RW	Bit[7:0]: TPGM[7:0] OTP programming time set 8 LSB
P3:0xE1	TPGM	0x00	RW	Bit[7:6]: Not used Bit[5:0]: TPGM[13:8] OTP programming time set 6 MSB
P3:0xE2	TSUP_CS	0x01	RW	OTP Operation Address Setup Time Set
P3:0xE3	THP_CS	0x01	RW	OTP Operation Address Hold Time Set
P3:0xE4	TSQ	0x02	RW	OTP Access Time Set
P3:0xE5	TRD	0x17	RW	OTP Read Time Set
P3:0xE6	TGAP	0x04	RW	Time Gap Set Where Between Steady Outputs Data to Read Enable Signals (this will improve timing)

6.24 OTP status [P3:0xE7, P3:0xEC]

table 6-24 OTP status registers

address	register name	default value	R/W	description
P3:0xE7	PGM_PERMIT	0x00	RW	OTP Programming Permit Flag 0: Forbid PGM process 1: PGM process permit
P3:0xEC	OTP_CTL	–	R	Bit[7:4]: Not used Bit[3]: otp_pgm_flag OTP program flag Bit[2]: read_flag Byte read flag Bit[1]: bat_rd_flag OTP batch read flag Bit[0]: otp_busy OTP busy flag Note: All flags read only

6.25 OTP mode control [P3:0xC0, P3:0xE8, P3:0xEA - P3:0xEB]

table 6-25 OTP mode control registers

address	register name	default value	R/W	description
P3:0xC0	DP_POS_EN	0x00	RW	OTP Send DPIX Coordinate Enable 0: Disable OTP send DPIX coordinate 1: Enable OTP send DPIX coordinate
P3:0xE8	OTP_PGM_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: Start program OTP Warning: Before using this command, user must make sure that OTP is not busy and has written exact address with a suitable value when program operation permits.
P3:0xEA	DATA_BYT_WR	0x00	RW	Data Required to Program to OTP in Byte Program Mode
P3:0xEB	ADDR_BYT_WR	0x00	RW	OTP Cell Address in Byte Program Mode

6.26 OTP batch buffer [P4:0x00 - P4:0x3F]

table 6-26 OTP batch buffer registers (sheet 1 of 3)

address	register name	default value	R/W	description
P4:0x00	FLAG_LOAD0	0x00	RW	Bit[7:6]: Not used Bit[5]: flag_load0 Block 5 programmed flag 0: Block 5 is empty 1: Block 5 is programmed Bit[4]: flag_load0 Block 4 programmed flag 0: Block 4 is empty 1: Block 4 is programmed Bit[3]: flag_load0 Block 3 programmed flag 0: Block 3 is empty 1: Block 3 is programmed Bit[2]: flag_load0 Block 2 programmed flag 0: Block 2 is empty 1: Block 2 is programmed Bit[1]: flag_load0 Block 1 programmed flag 0: Block 1 is empty 1: Block 1 is programmed Bit[0]: flag_load0 Block 0 programmed flag 0: Block 0 is empty 1: Block 0 is programmed
P4:0x01	FLAG_LOAD1	0x00	RW	Reserved Flag Register
P4:0x02	LINE_CODE	0x00	RW	Production Identification
P4:0x03	LOT_YEAR_MONTH	0x00	RW	Production Identification lot_year and lot_month
P4:0x04	LOT_DAY	0x00	RW	Production Identification lot_day
P4:0x05	LOT_SNUM	0x00	RW	Production Identification lot_snum
P4:0x06	WAFER_ID	0x00	RW	Production Identification wafer_id
P4:0x07	WAFER_X	0x00	RW	Production Identification wafer_x
P4:0x08	WAFER_Y	0x00	RW	Production Identification wafer_y
P4:0x09	OTP_R_GAIN	0x80	RW	User Register 1 Reserved register for user
P4:0x0A	OTP_B_GAIN	0x80	RW	User Register 2 Reserved register for user
P4:0x0B	OTP_GR_GAIN	0x80	RW	User Register 3 Reserved register for user
P4:0x0C	OTP_GB_GAIN	0x80	RW	User Register 4 Reserved register for user
P4:0x0D	USER_RSV_01	0x00	RW	User Register 5 Reserved register for user

table 6-26 OTP batch buffer registers (sheet 2 of 3)

address	register name	default value	R/W	description
P4:0x0E	USER_RSV_02	0x00	RW	User Register 6 Reserved register for user
P4:0x0F	USER_RSV_03	0x00	RW	User Register 7 Reserved register for user
P4:0x10	USER_RSV_04	0x00	RW	User Register 8 Reserved register for user
P4:0x11	USER_RSV_05	0x00	RW	User Register 9 Reserved register for user
P4:0x12	ISP_REGF_12	0x00	RW	12th Byte Data in Batch Operation Mode
P4:0x13	ISP_REGF_13	0x00	RW	13th Byte Data in Batch Operation Mode
P4:0x14	ISP_REGF_14	0x14	RW	14th Byte Data in Batch Operation Mode
P4:0x15	ISP_REGF_15	0x46	RW	15th Byte Data in Batch Operation Mode
P4:0x16	ISP_REGF_16	0x46	RW	16th Byte Data in Batch Operation Mode
P4:0x17	ISP_REGF_17	0x46	RW	17th Byte Data in Batch Operation Mode
P4:0x18	ISP_REGF_18	0x46	RW	18th Byte Data in Batch Operation Mode
P4:0x19	ISP_REGF_19	0x10	RW	19th Byte Data in Batch Operation Mode
P4:0x1A	ISP_REGF_1A	0x10	RW	1A Byte Data in Batch Operation Mode
P4:0x1B	ISP_REGF_1B	0x10	RW	1B Byte Data in Batch Operation Mode
P4:0x1C	ISP_REGF_1C	0x10	RW	1C Byte Data in Batch Operation Mode
P4:0x1D	ISP_REGF_1D	0x10	RW	1D Byte Data in Batch Operation Mode
P4:0x1E	ISP_REGF_1E	0x10	RW	1E Byte Data in Batch Operation Mode
P4:0x1F	ISP_REGF_1F	0x10	RW	1F Byte Data in Batch Operation Mode
P4:0x20	ISP_REGF_20	0x10	RW	20th Byte Data in Batch Operation Mode
P4:0x21	ISP_REGF_21	0x46	RW	21th Byte Data in Batch Operation Mode
P4:0x22	ISP_REGF_22	0x46	RW	22th Byte Data in Batch Operation Mode
P4:0x23	ISP_REGF_23	0x46	RW	23th Byte Data in Batch Operation Mode
P4:0x24	ISP_REGF_24	0x46	RW	24th Byte Data in Batch Operation Mode
P4:0x25	ISP_REGF_25	0x3C	RW	25th Byte Data in Batch Operation Mode
P4:0x26	ISP_REGF_26	0x3C	RW	26th Byte Data in Batch Operation Mode
P4:0x27	ISP_REGF_27	0x3C	RW	27th Byte Data in Batch Operation Mode
P4:0x28	ISP_REGF_28	0x3C	RW	28th Byte Data in Batch Operation Mode

table 6-26 OTP batch buffer registers (sheet 3 of 3)

address	register name	default value	R/W	description
P4:0x29	ISP_REGF_29	0x3C	RW	29th Byte Data in Batch Operation Mode
P4:0x2A	ISP_REGF_2A	0x3C	RW	2A Byte Data in Batch Operation Mode
P4:0x2B	ISP_REGF_2B	0x3C	RW	2B Byte Data in Batch Operation Mode
P4:0x2C	ISP_REGF_2C	0x3C	RW	2C Byte Data in Batch Operation Mode
P4:0x2D	ISP_REGF_2D	0x0A	RW	2D Byte Data in Batch Operation Mode
P4:0x2E	ISP_REGF_2E	0x0A	RW	2E Byte Data in Batch Operation Mode
P4:0x2F	ISP_REGF_2F	0x0A	RW	2F Byte Data in Batch Operation Mode
P4:0x30	ISP_REGF_30	0x0A	RW	30th Byte Data in Batch Operation Mode
P4:0x31	ISP_REGF_31	0x32	RW	31th Byte Data in Batch Operation Mode
P4:0x32	ISP_REGF_32	0x32	RW	32th Byte Data in Batch Operation Mode
P4:0x33	ISP_REGF_33	0x32	RW	33th Byte Data in Batch Operation Mode
P4:0x34	ISP_REGF_34	0x32	RW	34th Byte Data in Batch Operation Mode
P4:0x35	ISP_REGF_35	0x20	RW	35th Byte Data in Batch Operation Mode
P4:0x36	ISP_REGF_36	0x20	RW	36th Byte Data in Batch Operation Mode
P4:0x37	ISP_REGF_37	0x20	RW	37th Byte Data in Batch Operation Mode
P4:0x38	ISP_REGF_38	0x20	RW	38th Byte Data in Batch Operation Mode
P4:0x39	ISP_REGF_39	0x00	RW	39th Byte Data in Batch Operation Mode
P4:0x3A	ISP_REGF_3A	0xFF	RW	3A Byte Data in Batch Operation Mode
P4:0x3B	ISP_REGF_3B	0x44	RW	3B Byte Data in Batch Operation Mode
P4:0x3C	ISP_REGF_3C	0x0A	RW	3C Byte Data in Batch Operation Mode
P4:0x3D	ISP_REGF_3D	0x0A	RW	3D Byte Data in Batch Operation Mode
P4:0x3E	ISP_REGF_3E	0x0A	RW	3E Byte Data in Batch Operation Mode
P4:0x3F	ISP_REGF_3F	0x0A	RW	3F Byte Data in Batch Operation Mode

7 operating specifications

7.1 absolute maximum ratings

table 7-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 functional temperature

table 7-2 functional temperature

parameter	range
operating temperature (for applications up to 90 fps)[a]	-30°C to +85°C junction temperature
stable image temperature[b]	-10°C to +60°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

7.3 DC characteristics

table 7-3 DC characteristics (-30°C < T_J < 85°C)[ab]

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.7	2.8	3.0	V
V_{DD-D}	supply voltage (digital core)	1.15	1.2	1.3	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	1.9	V
digital inputs (typical conditions: DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[c]	SCL and SDA			0.54	V
V_{IH}[c]	SCL and SDA	1.26			V

a. external clock is stopped during measurement

b. standby current is based on room temperature

c. based on DOVDD = 1.8V

7.4 timing characteristics

figure 7-1 reference clock input timing diagram

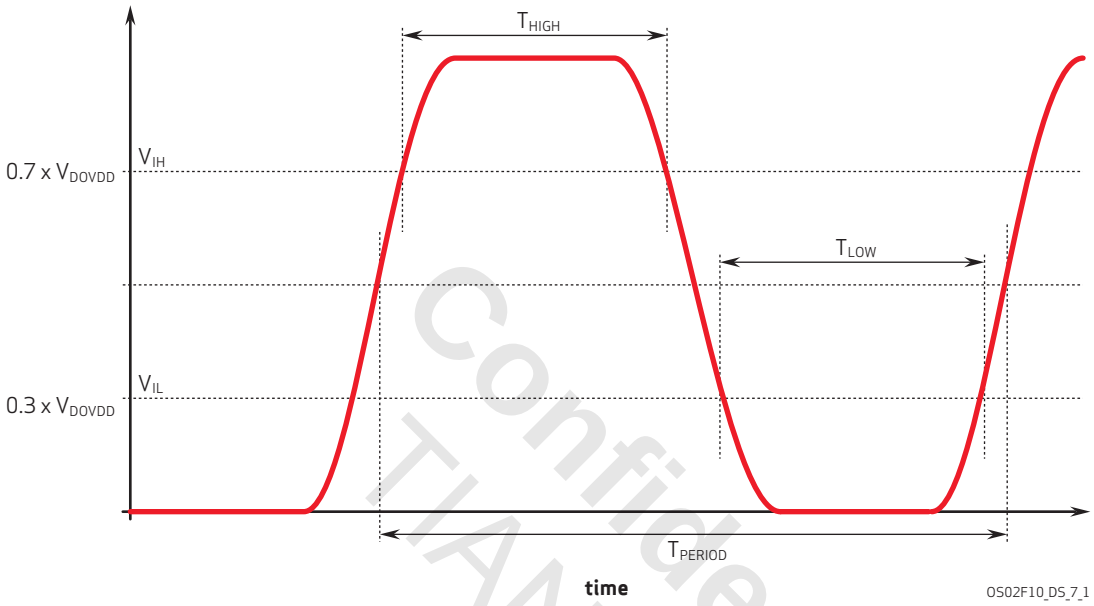


table 7-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{XVCLK}	frequency (XVCLK)[a]	6	24	27	MHz
T_{PERIOD}	period (XVCLK)	37.0	41.7	166.7	ns
T_{LOW}	low level width (XVCLK)	0.35×T_{PERIOD}		0.65×T_{PERIOD}	ns
T_{HIGH}	high level width (XVCLK)	0.35×T_{PERIOD}		0.65×T_{PERIOD}	ns

a. for input clock range 6~27 MHz, the OS02F10 can tolerate input clock period jitter up to 600 ps peak-to-peak

8 mechanical specifications

8.1 physical specifications

figure 8-1 package specifications

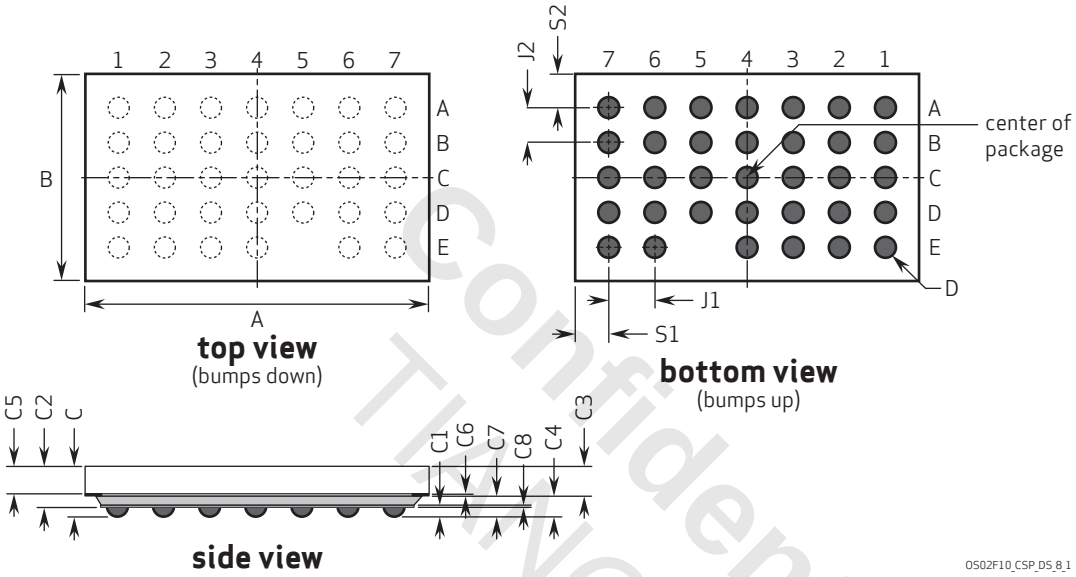


table 8-1 package dimensions (sheet 1 of 2)

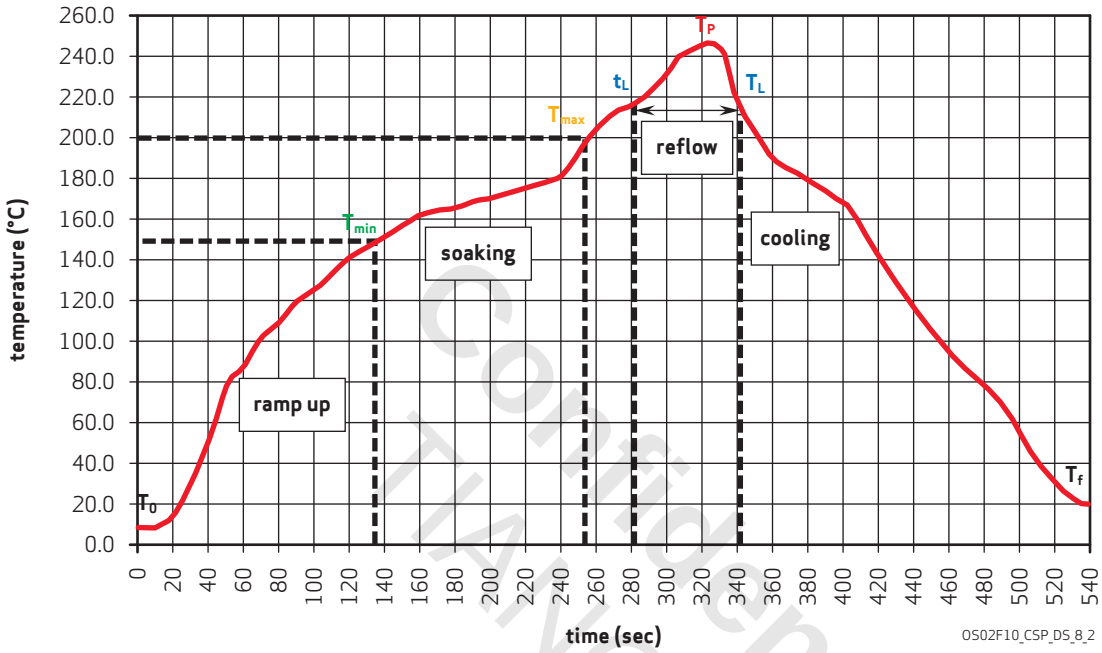
parameter	symbol	min	typ	max	unit
package body dimension x	A	4895.6	4920.6	4945.6	µm
package body dimension y	B	2939.0	2964.0	2989.0	µm
package height	C	586.5	641.5	696.5	µm
ball height	C1	100	130	160	µm
package body thickness	C2	476.5	511.5	546.5	µm
thickness from top glass surface to die	C3	316	330	344	µm
image plane height	C4	270.5	311.5	352.5	µm
glass thickness	C5	290	300	310	µm
air gap between sensor and glass	C6	25	30	35	µm
silicon thickness	C7	140	150	160	µm
IR block thickness	C8	1.4	1.5	1.6	µm

table 8-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
ball diameter	D	220	250	280	µm
total pin count	N		34		
pin count x-axis	N1		7		
pin count y-axis	N2		5		
pins pitch x-axis	J1	650	660	670	µm
pins pitch y-axis	J2	490	500	510	µm
edge-to-pin center distance along x	S1	450.3	480.3	510.3	µm
edge-to-pin center distance along y	S2	452	482	512	µm

8.2 IR reflow specifications

figure 8-2 IR reflow ramp rate requirements



note The OS02F10 uses a lead-free package.

note To reduce image artifacts from infrared light and to provide the best image quality. OmniVision recommends an IR cut filter.

table 8-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_P)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5° (duration max 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30 ~ 120 seconds
ramp down A (T_P to T_L)	cooling down from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling down from 217°C to room temperature	temperature slope ≤ 2°C per second
T_0 to T_P	room temperature to peak temperature	≤ 8 minutes

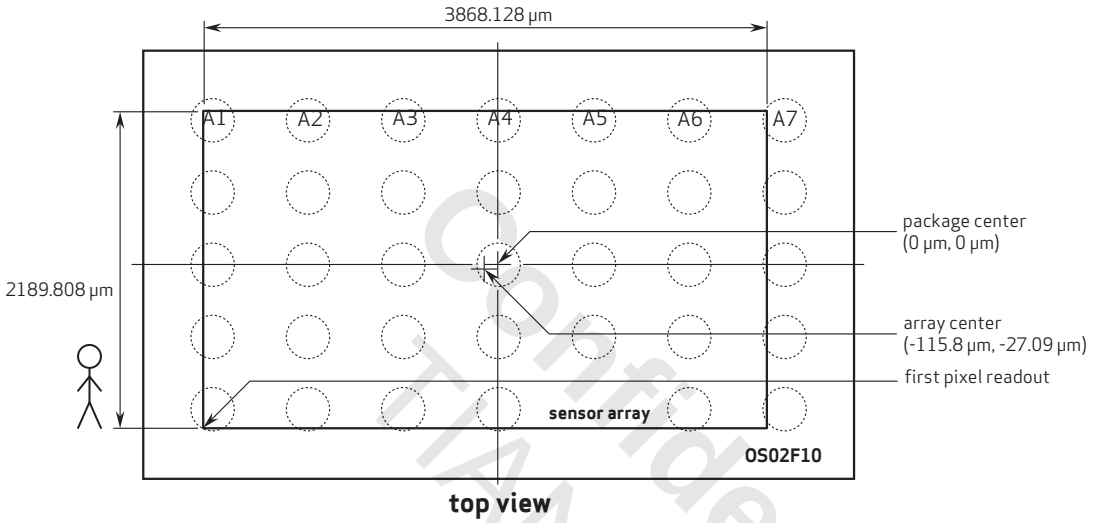
a. maximum number of reflow cycles = 3

b. N2 gas reflow or control O2 gas PPM <500 as recommendation

9 optical specifications

9.1 sensor array center

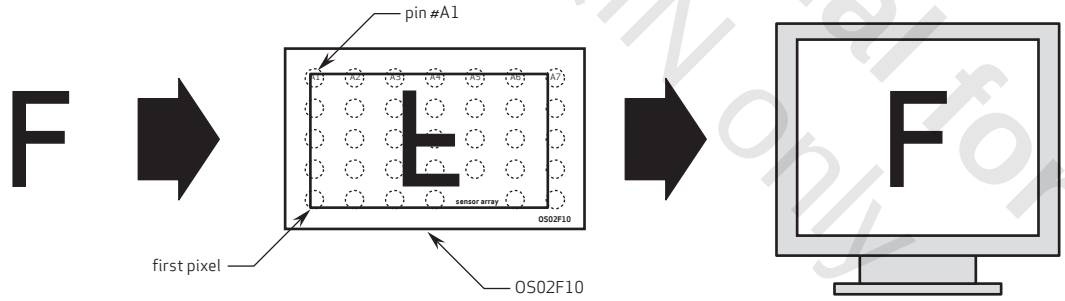
figure 9-1 sensor array center



note 1 this drawing is not to scale and is for reference only.

OS02F10_CSP_DS_9_1

figure 9-2 final image output



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9.2 lens chief ray angle (CRA)

figure 9-3 chief ray angle (CRA)

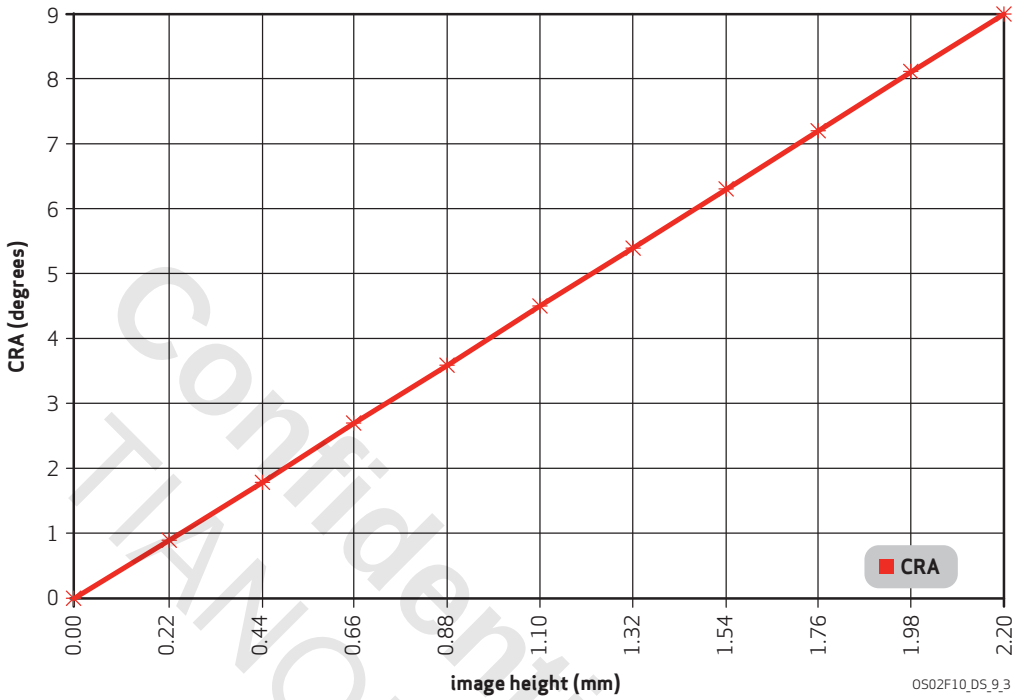

table 9-1 CRA versus image height plot

field (%)	image height (mm)	CRA (degrees)
0.0	0.00	0.0
0.1	0.22	0.9
0.2	0.44	1.8
0.3	0.66	2.7
0.4	0.88	3.6
0.5	1.10	4.5
0.6	1.32	5.4
0.7	1.54	6.3
0.8	1.76	7.2
0.9	1.98	8.1
1.0	2.20	9.0

revision history

version 1.0 04.12.2018

- initial release

version 1.1 05.16.2018

- changed "PureCel" to "OmniBSI" throughout datasheet
- in section 3.5.1, updated figure 3-4
- in table 3-1, added rows for registers P1:0x31 and P1:0x97
- in table 3-1, changed PLL_VCO equation in description of registers P0:0x2E and P0:0x2F to "[PLL input*(pll_nc+3)*2/(pll_mc+1)]" and changed description of register bit P0:0x30[4] to "pclk_ctrl, 0: pclk_pre = pll_timer_clk, 1: pclk_pre = pll_timer_clk/2"
- in table 6-1, changed PLL_VCO equation in description of registers P0:0x2E and P0:0x2F to "[PLL input*(pll_nc+3)*2/(pll_mc+1)]" and changed description of register bit P0:0x30[4] to "pclk_ctrl, 0: pclk_pre = pll_timer_clk, 1: pclk_pre = pll_timer_clk/2"

version 1.11 08.23.2018

- in section 8.1, updated figure 8-1
- in section 9.1, updated figure 9-1 and added new figure 9-2

version 1.2 10.31.2018

- in key specifications, changed sensitivity to 10470 e⁻/Lux-sec (5100K G channel), changed max S/N ratio to 38.1 dB, and changed dynamic range to 72.9 dB @ 16x gain
- in section 3.5.1, updated figure 3-4
- in table 4-2, removed "half" from description of register bits P2:0xA6[3:0] and P2:0xA7[7:0]
- in table 4-4, changed name of register P1:0xF5 to RSVD, changed default value of register P1:0xF5 to –, changed RW of register P1:0xF5 to –, changed description of register P1:0xF5 to Reserved, and removed description of register bits P1:0xFA[4] and P1:0xFA[2]
- in section 4.6, removed tables 4-7 and 4-8
- in table 6-11, changed name of register P1:0xF5 to RSVD, changed default value of register P1:0xF5 to –, changed RW of register P1:0xF5 to –, and changed description of register P1:0xF5 to Reserved
- in table 6-11, changed description of register bit P1:0xFA[7:2] to Not used
- in table 6-22, removed "half" from description of register bits P2:0xA6[3:0] and P2:0xA7[7:0]

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