SONY

Diagonal 11.1 mm (Type 2/3) CMOS solid-state Image Sensor with Square Pixel for Monochrome Cameras

IMX566-AAMJ-C

Pregius S

1. Description

The IMX566-AAMJ-C is a diagonal 11.1 mm (Type 2/3) CMOS active pixel type solid-state image sensor with a square pixel array and 8.13 M effective pixels. This chip features a global shutter with variable charge-integration time. This chip operates with analog 3.3 V, 2.9 V, digital 1.1 V, and interface 1.8 V quadruple power supply. High sensitivity and low dark current characteristics are achieved.
(Applications: FA cameras, ITS cameras)

2. Features

- CMOS active pixel type dots
- Built-in timing adjustment circuit, H/V driver and serial communication circuit
- Global shutter function
- Input frequency 37.125 MHz / 74.25 MHz / 54 MHz
- Number of recommended recording pixels: 2840 (H) × 2840 (V) approx. 8.06 M pixels
- Readout mode
  All-pixel scan mode
  Vertical / Horizontal 1/2 Subsampling mode
  2 × 2 FD binning mode
  ROI mode
  Vertical / Horizontal ‐ Normal / Inverted readout mode
- Readout rate
  Maximum frame rate in

  All-pixel scan mode: 8 bit 62.6 frame/s, 10 bit 51.3 frame/s, 12 bit 43.4 frame/s
  (*) At high frame rates, control so as not to exceed Tj = +100 °C
- Variable-speed shutter function (resolution 1 H units)
- Pulse Output Function

  The monitor output for Exposure period (TOUT0)
  Programmable pulse output (TOUT1 and TOUT2)
- 8-bit / 10-bit / 12-bit A/D converter
- CDS / PGA function
  0 dB to 24 dB: Analog Gain (0.1 dB step)
  24.1 dB to 48 dB: Analog Gain: 24 dB + Digital Gain: 0.1 dB to 24 dB (0.1 dB step)
- I/O interface
  CSI-2 serial data output (2 Lane / 4 Lane switching)
- Recommended lens F number: 2.8 or more (Close side)

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3. Device Structure

◆ CMOS image sensor

◆ Image size

Diagonal 11.1 mm (Type 2/3) Approx. 8.13 M pixels

◆ Total number of pixels

2856 (H) × 2912 (V) Approx. 8.31 M pixels

◆ Number of effective pixels

2856 (H) × 2848 (V) Approx. 8.13 M pixels

◆ Number of active pixels

2856 (H) × 2848 (V) Approx. 8.13 M pixels

◆ Number of recommended recording pixels

2840 (H) × 2840 (V) Approx. 8.06 M pixels

◆ Unit cell size

2.74 µm (H) × 2.74 µm (V)

◆ Optical black

Horizontal (H) direction: Front 0 pixels, rear 0 pixels
Vertical (V) direction: Front 64 pixels, rear 0 pixels

◆ Substrate material

Silicon

4. Absolute Maximum Ratings

Item	Symbol	Rating			Unit	Remarks
Supply voltage (Analog 3.3 V)	$AV_{DD}1$	-0.3	to	4.65	V	
Supply voltage (Analog 2.9 V)	$AV_{DD}2$	-0.3	to	4.65	V	
Supply voltage (Interface 1.8 V)	OV_{DD}	-0.3	to	4.65	V	
Supply voltage (Digital 1.1 V)	DV_{DD}	-0.3	to	1.65	V	
Input voltage	VI	-0.3	to	OV_{DD} + 0.3	V	Do not exceed 4.65V
Output voltage	VO	-0.3	to	OV_{DD} + 0.3	V	Do not exceed 4.65V
Operating temperature	Topr	-30	to	+75	˚C	High temperature side: Tj = +100°C *1
Storage temperature	Tstg	-40	to	+85	˚C	

*1 Please control not to exceed "Tj = + 100 °C" using the thermometer function built in the image sensor.
For the thermometer function, please refer to the application note of "Thermometer".

5. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (Analog 3.3 V)	$AV_{DD}1$	3.15	3.3	3.45	V
Supply voltage (Analog 2.9 V)	$AV_{DD}2$	2.75	2.9	3.05	V
Supply voltage (Interface 1.8 V)	OV_{DD}	1.7	1.8	1.9	V
Supply voltage (Digital 1.1 V)	DV_{DD}	1.0	1.1	1.2	V
Performance guarantee temperature	Tspec	-10	–	+60	˚C

6. USE RESTRICTION NOTICE

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General-0.0.9

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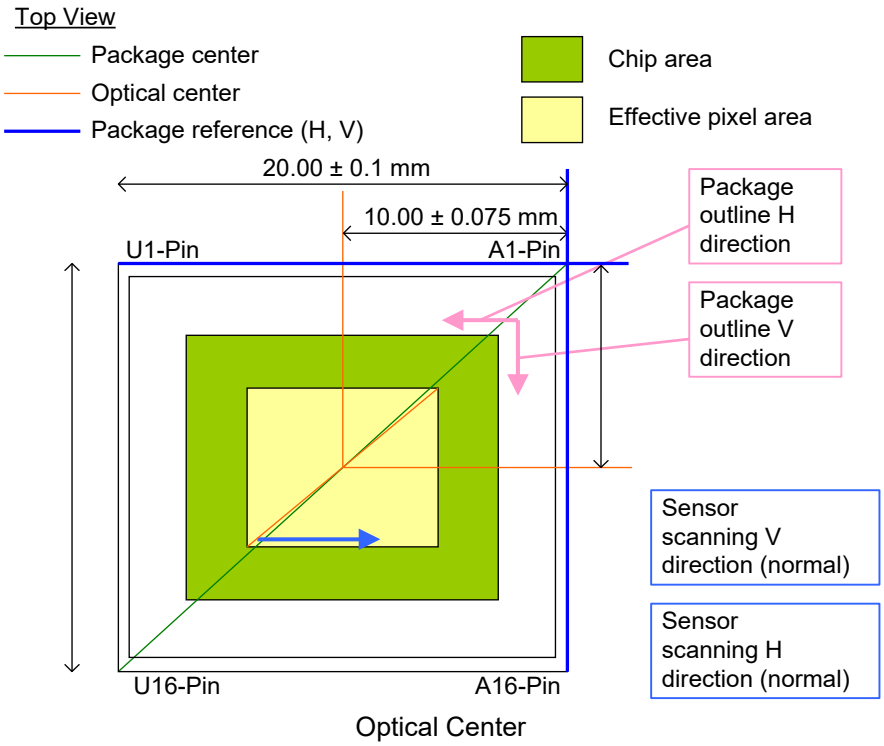
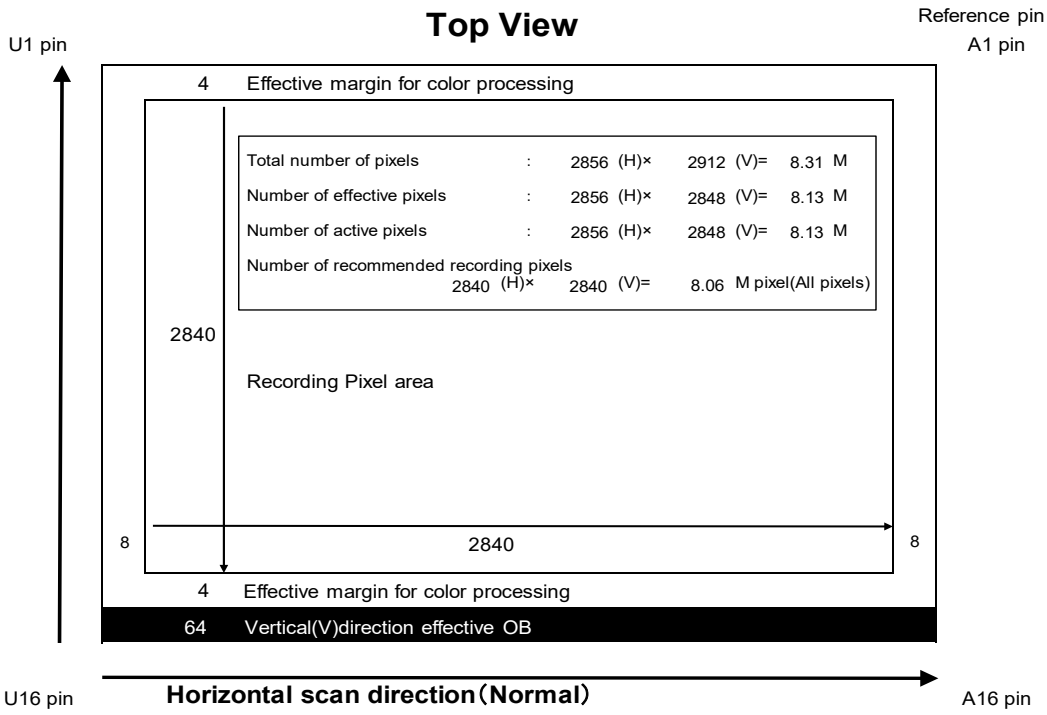
7. Chip Center and Optical Center



8. Pixel Arrangement

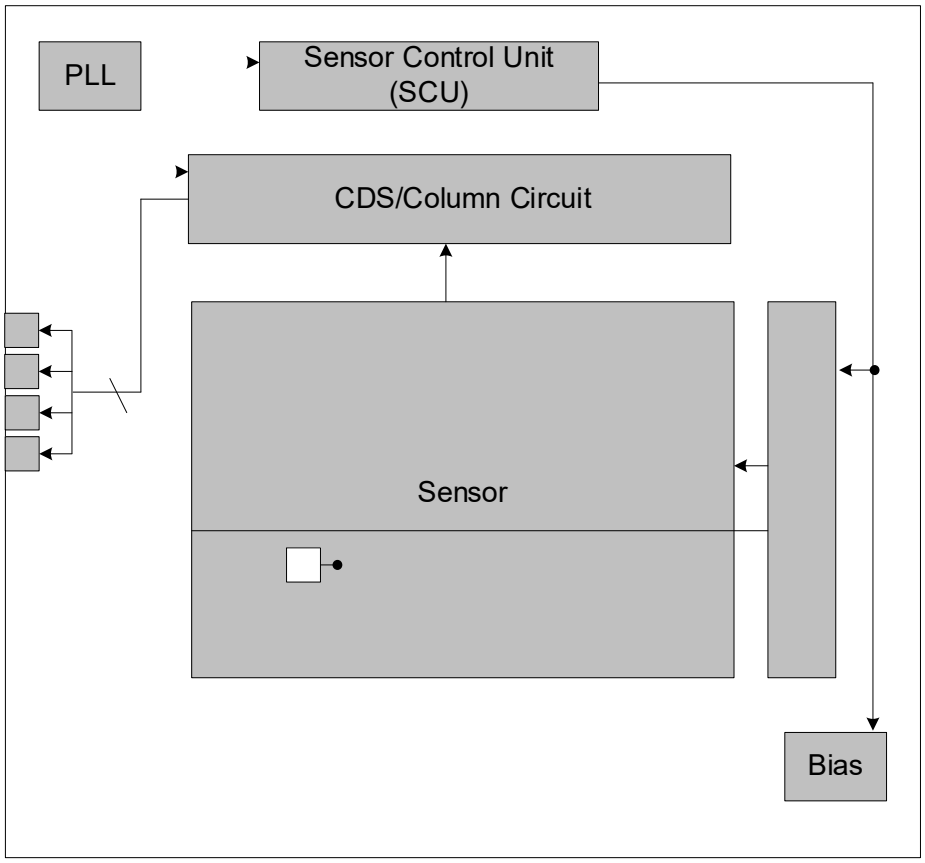


* Reference pin number is consecutive numbering of package pin array.
See the Pin Configuration for the number of each pin.

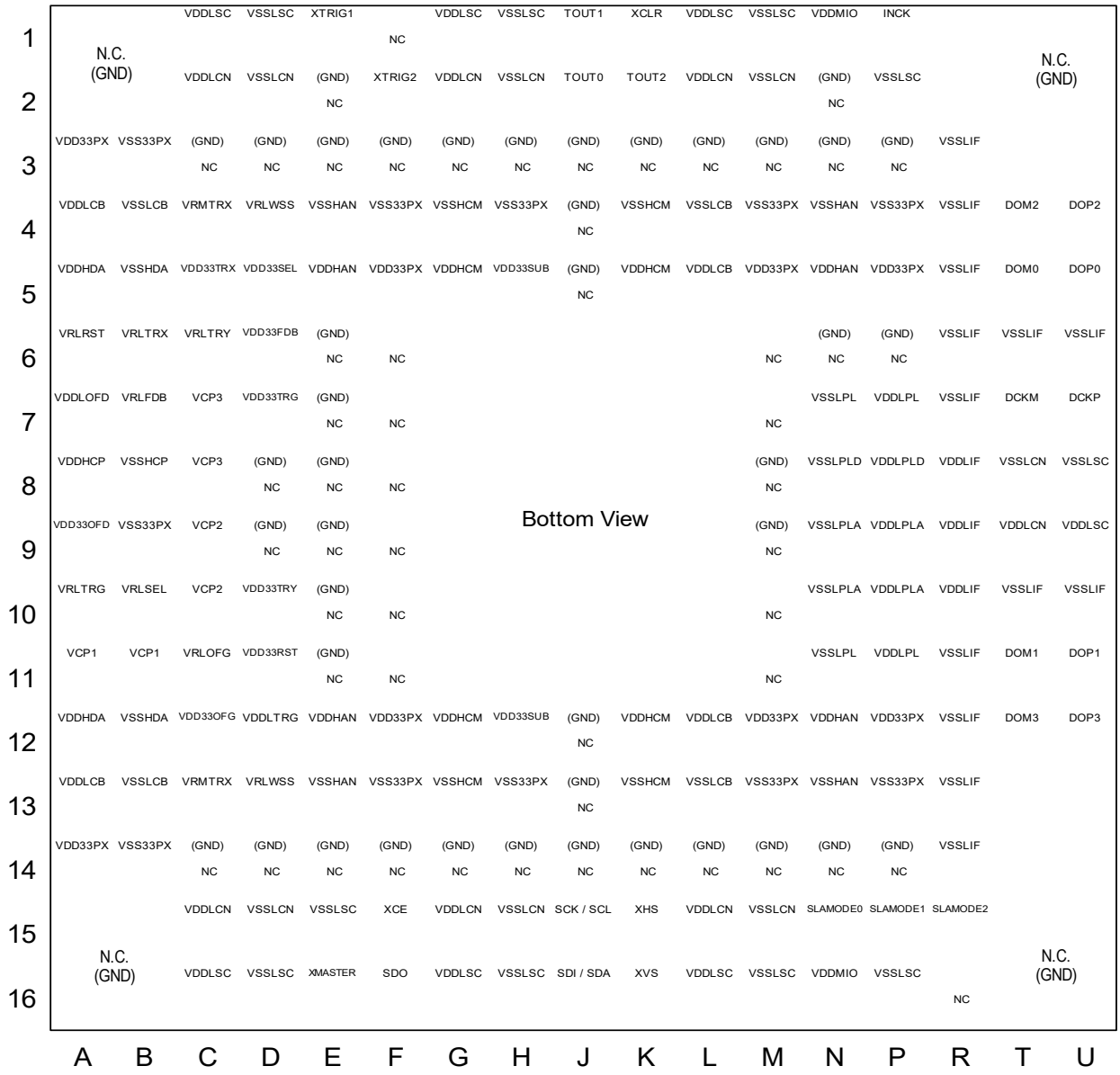
Pixel Arrangement

9. Block Diagram and Pin Configuration

(Top View)



Block Diagram



3.3 V Power Supply	3.3 V GND
2.9 V Power Supply	2.9 V GND
1.8 V Power Supply	1.8 V GND
1.1 V Power Supply	1.1 V GND
Clock	Data output
N.C.	Signal I/O

*The N.C. pin with (GND) can be connected to GND.

Pin Configuration

10. Pin Description

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
1	A1	—	—	N.C.	GND connection is allowed
2	A3	Power	A	VDD33PX	3.3 V power supply
3	A4	Power	A	VDDLCB	1.1 V power supply
4	A5	Power	A	VDDHDA	2.9 V power supply
5	A6	GND	A	VRLRST	3.3 V GND
6	A7	Power	A	VDDLOFD	1.1 V power supply
7	A8	Power	A	VDDHCP	2.9 V power supply
8	A9	Power	A	VDD33OFD	3.3 V power supply
9	A10	I	A	VRLTRG	Connect to VCP1
10	A11	O	A	VCP1	Connect to VRLTRG (Connect 4.7 µF × 4 to GND)
11	A12	Power	A	VDDHDA	2.9 V power supply
12	A13	Power	A	VDDLCB	1.1 V power supply
13	A14	Power	A	VDD33PX	3.3 V power supply
14	A16	—	—	N.C.	GND connection is allowed
15	B3	GND	A	VSS33PX	3.3 V GND
16	B4	GND	A	VSSLCB	1.1 V GND
17	B5	GND	A	VSSHDA	2.9 V GND
18	B6	I	A	VRLTRX	Connect to VCP2 and VCP3
19	B7	I	A	VRLFDB	Connect to VCP2 and VCP3
20	B8	GND	A	VSSHCP	2.9 V GND
21	B9	GND	A	VSS33PX	3.3 V GND
22	B10	I	A	VRLSEL	Connect to VCP2 and VCP3
23	B11	O	A	VCP1	Connect to VRLTRG (Connect 4.7 µF × 4 to GND)
24	B12	GND	A	VSSHDA	2.9 V GND
25	B13	GND	A	VSSLCB	1.1 V GND
26	B14	GND	A	VSS33PX	3.3 V GND
27	C1	Power	D	VDDLSC	1.1 V power supply
28	C2	Power	D	VDDLCN	1.1 V power supply
29	C3	—	—	N.C.	GND connection is allowed
30	C4	GND	A	VRMTRX	3.3 V GND
31	C5	Power	A	VDD33TRX	3.3 V power supply
32	C6	I	A	VRLTRY	Connect to VCP2 and VCP3
33	C7	O	A	VCP3	Connect to VRLOFG, VRLSEL, VRLFDB, VRLTRX, VRLTRY (Connect 4.7 µF × 4 to GND)
34	C8	O	A	VCP3	Connect to VRLOFG, VRLSEL, VRLFDB, VRLTRX, VRLTRY (Connect 4.7 µF × 4 to GND)
35	C9	O	A	VCP2	Connect to VRLOFG, VRLSEL, VRLFDB, VRLTRX, VRLTRY (Connect 4.7 µF × 4 to GND)
36	C10	O	A	VCP2	Connect to VRLOFG, VRLSEL, VRLFDB, VRLTRX, VRLTRY (Connect 4.7 µF × 4 to GND)
37	C11	I	A	VRLOFG	Connect to VCP2 and VCP3
38	C12	Power	A	VDD33OFG	3.3 V power supply
39	C13	GND	A	VRMTRX	3.3 V GND
40	C14	—	—	N.C.	GND connection is allowed
41	C15	Power	D	VDDLCN	1.1 V power supply
42	C16	Power	D	VDDLSC	1.1 V power supply
43	D1	GND	D	VSSLSC	1.1 V GND
44	D2	GND	D	VSSLCN	1.1 V GND
45	D3	—	—	N.C.	GND connection is allowed
46	D4	GND	A	VRLWSS	3.3 V GND
47	D5	Power	A	VDD33SEL	3.3 V power supply
48	D6	Power	A	VDD33FDB	3.3 V power supply
49	D7	Power	A	VDD33TRG	3.3 V power supply
50	D8	—	—	N.C.	GND connection is allowed
51	D9	—	—	N.C.	GND connection is allowed
52	D10	Power	A	VDD33TRY	3.3 V power supply
53	D11	Power	A	VDD33RST	3.3 V power supply

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
54	D12	Power	A	VDDLTRG	1.1 V power supply
55	D13	GND	A	VRLWSS	3.3 V GND
56	D14	—	—	N.C.	GND connection is allowed
57	D15	GND	D	VSSLCN	1.1 V GND
58	D16	GND	D	VSSLSC	1.1 V GND
59	E1	I	D	XTRIG1	Trigger input 1
60	E2	—	—	N.C.	GND connection is allowed
61	E3	—	—	N.C.	GND connection is allowed
62	E4	GND	A	VSSHAN	2.9 V GND
63	E5	Power	A	VDDHAN	2.9 V power supply
64	E6	—	—	N.C.	GND connection is allowed
65	E7	—	—	N.C.	GND connection is allowed
66	E8	—	—	N.C.	GND connection is allowed
67	E9	—	—	N.C.	GND connection is allowed
68	E10	—	—	N.C.	GND connection is allowed
69	E11	—	—	N.C.	GND connection is allowed
70	E12	Power	A	VDDHAN	2.9 V power supply
71	E13	GND	A	VSSHAN	2.9 V GND
72	E14	—	—	N.C.	GND connection is allowed
73	E15	GND	D	VSSLSC	1.1 V GND
74	E16	I	D	XMASTER	Master / Slave select (Slave Mode: High, Master Mode: Low)
75	F1	—	—	N.C.	—
76	F2	I	D	XTRIG2	Trigger input 2
77	F3	—	—	N.C.	GND connection is allowed
78	F4	GND	A	VSS33PX	3.3 V GND
79	F5	Power	A	VDD33PX	3.3 V power supply
80	F6	—	—	N.C.	—
81	F7	—	—	N.C.	—
82	F8	—	—	N.C.	—
83	F9	—	—	N.C.	—
84	F10	—	—	N.C.	—
85	F11	—	—	N.C.	—
86	F12	Power	A	VDD33PX	3.3 V power supply
87	F13	GND	A	VSS33PX	3.3 V GND
88	F14	—	—	N.C.	GND connection is allowed
89	F15	I	D	XCE	4-wire: Serial communication I/F XCE pin I^2C: Fixed to High
90	F16	O	D	SDO	4-wire: Serial communication I/F SDO pin I^2C: OPEN
91	G1	Power	D	VDDLSC	1.1 V power supply
92	G2	Power	D	VDDLCN	1.1 V power supply
93	G3	—	—	N.C.	GND connection is allowed
94	G4	GND	A	VSSHCM	2.9 V GND
95	G5	Power	A	VDDHCM	2.9 V power supply
96	G12	Power	A	VDDHCM	2.9 V power supply
97	G13	GND	A	VSSHCM	2.9 V GND
98	G14	—	—	N.C.	GND connection is allowed
99	G15	Power	D	VDDLCN	1.1 V power supply
100	G16	Power	D	VDDLSC	1.1 V power supply
101	H1	GND	D	VSSLSC	1.1 V GND
102	H2	GND	D	VSSLCN	1.1 V GND
103	H3	—	—	N.C.	GND connection is allowed
104	H4	GND	A	VSS33PX	3.3 V GND
105	H5	Power	A	VDD33SUB	3.3 V power supply
106	H12	Power	A	VDD33SUB	3.3 V power supply
107	H13	GND	A	VSS33PX	3.3 V GND
108	H14	—	—	N.C.	GND connection is allowed

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
109	H15	GND	D	VSSLCN	1.1 V GND
110	H16	GND	D	VSSLSC	1.1 V GND
111	J1	O	D	TOUT1	Pulse1 output pin
112	J2	O	D	TOUT0	Pulse0 output pin
113	J3	—	—	N.C.	GND connection is allowed
114	J4	—	—	N.C.	GND connection is allowed
115	J5	—	—	N.C.	GND connection is allowed
116	J12	—	—	N.C.	GND connection is allowed
117	J13	—	—	N.C.	GND connection is allowed
118	J14	—	—	N.C.	GND connection is allowed
119	J15	I	D	SCK / SCL	4-wire: Serial communication I/F SCK pin I^2C: Serial clock line
120	J16	I/O	D	SDI / SDA	4-wire: Serial communication I/F SDI pin I^2C: Serial data line
121	K1	I	D	XCLR	System clear (Normal: High, Clear: Low)
122	K2	O	D	TOUT2	Pulse2 output pin
123	K3	—	—	N.C.	GND connection is allowed
124	K4	GND	A	VSSHCM	2.9 V GND
125	K5	Power	A	VDDHCM	2.9 V power supply
126	K12	Power	A	VDDHCM	2.9 V power supply
127	K13	GND	A	VSSHCM	2.9 V GND
128	K14	—	—	N.C.	GND connection is allowed
129	K15	I/O	D	XHS	Horizontal sync signal
130	K16	I/O	D	XVS	Vertical sync signal
131	L1	Power	D	VDDLSC	1.1 V power supply
132	L2	Power	D	VDDLCN	1.1 V power supply
133	L3	—	—	N.C.	GND connection is allowed
134	L4	GND	A	VSSLCB	1.1 V GND
135	L5	Power	A	VDDLCB	1.1 V power supply
136	L12	Power	A	VDDLCB	1.1 V power supply
137	L13	GND	A	VSSLCB	1.1 V GND
138	L14	—	—	N.C.	GND connection is allowed
139	L15	Power	D	VDDLCN	1.1 V power supply
140	L16	Power	D	VDDLSC	1.1 V power supply
141	M1	GND	D	VSSLSC	1.1 V GND
142	M2	GND	D	VSSLCN	1.1 V GND
143	M3	—	—	N.C.	GND connection is allowed
144	M4	GND	A	VSS33PX	3.3 V GND
145	M5	Power	A	VDD33PX	3.3 V power supply
146	M6	—	—	N.C.	—
147	M7	—	—	N.C.	—
148	M8	—	—	N.C.	GND connection is allowed
149	M9	—	—	N.C.	GND connection is allowed
150	M10	—	—	N.C.	—
151	M11	—	—	N.C.	—
152	M12	Power	A	VDD33PX	3.3 V power supply
153	M13	GND	A	VSS33PX	3.3 V GND
154	M14	—	—	N.C.	GND connection is allowed
155	M15	GND	D	VSSLCN	1.1 V GND
156	M16	GND	D	VSSLSC	1.1 V GND
157	N1	Power	D	VDDMIO	1.8 V power supply
158	N2	—	—	N.C.	GND connection is allowed
159	N3	—	—	N.C.	GND connection is allowed
160	N4	GND	A	VSSHAN	2.9 V GND
161	N5	Power	A	VDDHAN	2.9 V power supply
162	N6	—	—	N.C.	GND connection is allowed
163	N7	GND	D	VSSLPL	1.1 V GND

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
164	N8	GND	D	VSSLPLD	1.1 V GND
165	N9	GND	D	VSSLPLA	1.1 V GND
166	N10	GND	D	VSSLPLA	1.1 V GND
167	N11	GND	D	VSSLPL	1.1 V GND
168	N12	Power	A	VDDHAN	2.9 V power supply
169	N13	GND	A	VSSHAN	2.9 V GND
170	N14	—	—	N.C.	GND connection is allowed
171	N15	I	D	SLAMODE0	Slave address select
172	N16	Power	D	VDDMIO	1.8 V power supply
173	P1	I	D	INCK	Master clock input
174	P2	GND	D	VSSLSC	1.1 V GND
175	P3	—	—	N.C.	GND connection is allowed
176	P4	GND	A	VSS33PX	3.3 V GND
177	P5	Power	A	VDD33PX	3.3 V power supply
178	P6	—	—	N.C.	GND connection is allowed
179	P7	Power	D	VDDLPL	1.1 V power supply
180	P8	Power	D	VDDLPLD	1.1 V power supply
181	P9	Power	D	VDDLPLA	1.1 V power supply
182	P10	Power	D	VDDLPLA	1.1 V power supply
183	P11	Power	D	VDDLPL	1.1 V power supply
184	P12	Power	A	VDD33PX	3.3 V power supply
185	P13	GND	A	VSS33PX	3.3 V GND
186	P14	—	—	N.C.	GND connection is allowed
187	P15	I	D	SLAMODE1	Slave address select
188	P16	GND	D	VSSLSC	1.1 V GND
189	R1	—	—	N.C.	—
190	R2	—	—	N.C.	—
191	R3	GND	D	VSSLIF	1.1 V GND
192	R4	GND	D	VSSLIF	1.1 V GND
193	R5	GND	D	VSSLIF	1.1 V GND
194	R6	GND	D	VSSLIF	1.1 V GND
195	R7	GND	D	VSSLIF	1.1 V GND
196	R8	Power	D	VDDLIF	1.1 V power supply
197	R9	Power	D	VDDLIF	1.1 V power supply
198	R10	Power	D	VDDLIF	1.1 V power supply
199	R11	GND	D	VSSLIF	1.1 V GND
200	R12	GND	D	VSSLIF	1.1 V GND
201	R13	GND	D	VSSLIF	1.1 V GND
202	R14	GND	D	VSSLIF	1.1 V GND
203	R15	I	D	SLAMODE2	Slave address select
204	R16	—	—	N.C.	—
205	T3	—	—	N.C.	—
206	T4	O	D	DOM2	CSI-2 IF output (Data)
207	T5	O	D	DOM0	CSI-2 IF output (Data)
208	T6	GND	D	VSSLIF	1.1 V GND
209	T7	O	D	DCKM	CSI-2 IF output (Clock)
210	T8	GND	D	VSSLCN	1.1 V GND
211	T9	Power	D	VDDLCN	1.1 V power supply
212	T10	GND	D	VSSLIF	1.1 V GND
213	T11	O	D	DOM1	CSI-2 IF output (Data)
214	T12	O	D	DOM3	CSI-2 IF output (Data)
215	T13	—	—	N.C.	—
216	T14	—	—	N.C.	—
217	U1	—	—	N.C.	GND connection is allowed
218	U3	—	—	N.C.	—

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
219	U4	O	D	DOP2	CSI-2 IF output (Data)
220	U5	O	D	DOP0	CSI-2 IF output (Data)
221	U6	GND	D	VSSLIF	1.1 V GND
222	U7	O	D	DCKP	CSI-2 IF output (Clock)
223	U8	GND	D	VSSLSC	1.1 V GND
224	U9	Power	D	VDDLSC	1.1 V power supply
225	U10	GND	D	VSSLIF	1.1 V GND
226	U11	O	D	DOP1	CSI-2 IF output (Data)
227	U12	O	D	DOP3	CSI-2 IF output (Data)
228	U13	—	—	N.C.	—
229	U14	—	—	N.C.	—
230	U16	—	—	N.C.	GND connection is allowed

* N.C. pins in the table above should be left open on the board.

11. Electrical Characteristics

11.1. DC Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	V_{DD}33x	AV_{DD}1	—	3.15	3.3	3.45	V
	Analog	V_{DD}Hx	AV_{DD}2	—	2.75	2.9	3.05	V
	Digital	V_{DD}Mx	OV_{DD}	—	1.7	1.8	1.9	V
	Digital	V_{DD}Lx	DV_{DD}	—	1.0	1.1	1.2	V
Digital input voltage		XHS XVS XCLR INCK XMASTER SLAMODE0 SLAMODE1 SLAMODE2 SCK SDI XCE XTRIG1 XTRIG2	VIH	XVS / XHS in Slave mode	0.7 × OV_{DD}	—	—	V
			VIL		—	—	0.3 × OV_{DD}	V
Digital output voltage		XHS XVS SDO TOUT0 TOUT1 TOUT2	VOH	XVS / XHS in Master mode	OV_{DD} – 0.2	—	—	V
			VOL		—	—	0.2	V

11.2. Power Consumption

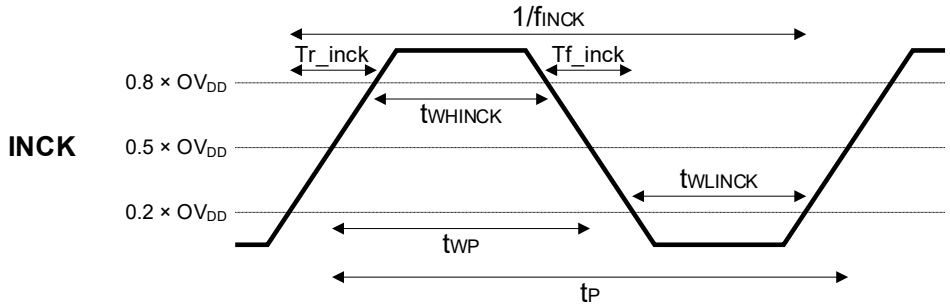
Item	Pins	Symbol	Typ.	Max.	Unit
Operating current MIPI CSI-2 4 Lane 12 bit 43.4 frame/s	V_{DD}33	IAV_{DD}1	35	45	mA
	V_{DD}H	IAV_{DD}2	100	135	mA
	V_{DD}M	IOV_{DD}	1	2	mA
	V_{DD}L	IDV_{DD}	200	315	mA
Standby current	V_{DD}33	IAV_{DD}1	—	0.1	mA
	V_{DD}H	IAV_{DD}2	—	0.1	mA
	V_{DD}M	IOV_{DD}_STB	—	0.05	mA
	V_{DD}L	IDV_{DD}_STB	—	200	mA

Operating current:
(Typical value condition) : Supply voltage: 3.3 V / 2.9 V / 1.8 V / 1.1 V, Tj = 25 ˚C
(Maximum value condition) : Supply voltage: 3.45 V / 3.05 V / 1.9 V / 1.2 V, Tj = 60 ˚C
Worst state of internal circuit operating current consumption.

Standby current:
(Maximum value condition) : Supply voltage: 3.45 V / 3.05 V / 1.9 V / 1.2 V, Tj = 60 ˚C, INCK = 0 V,
The device in the light-obstructed state.

11.3. AC Characteristics

11.3.1. Master Clock (INCK)

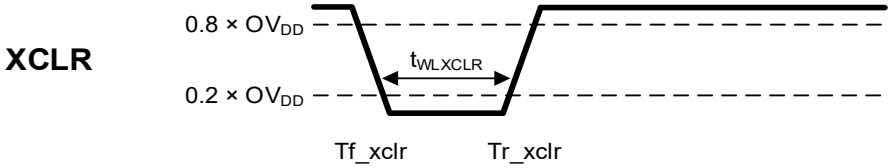


Duty Ratio = t_{WP} / t_P × 100

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 37.125 MHz, 74.25 MHz, 54 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	
INCK clock duty	—	40.0	50.0	60.0	%	Define with 0.5 × OV_{DD}
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	20 % to 80 %

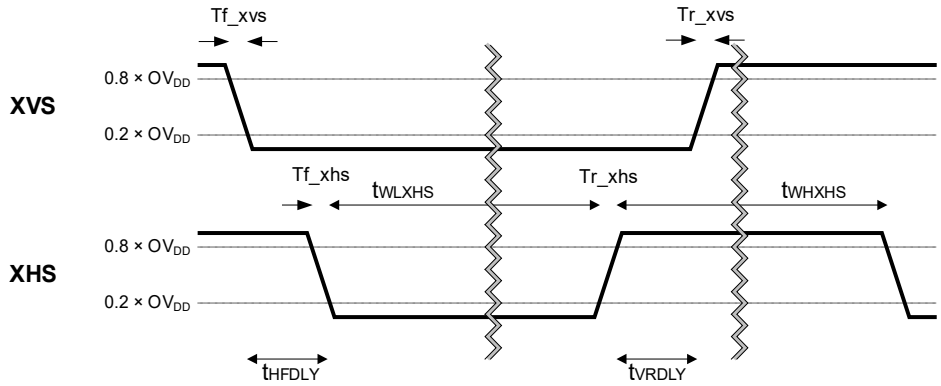
* The INCK fluctuation affects the frame rate.

11.3.2. System Clear (XCLR)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XCLR Low level pulse width	t_{WLXCLR}	$4/f_{INCK}$	—	—	ns	f_{INCK} = 37.125 MHz, 74.25 MHz, 54 MHz
XCLR Fall time	Tf_xclr	—	—	5	ns	80 % to 20 %
XCLR Rise time	Tr_xclr	—	—	5	ns	20 % to 80 %

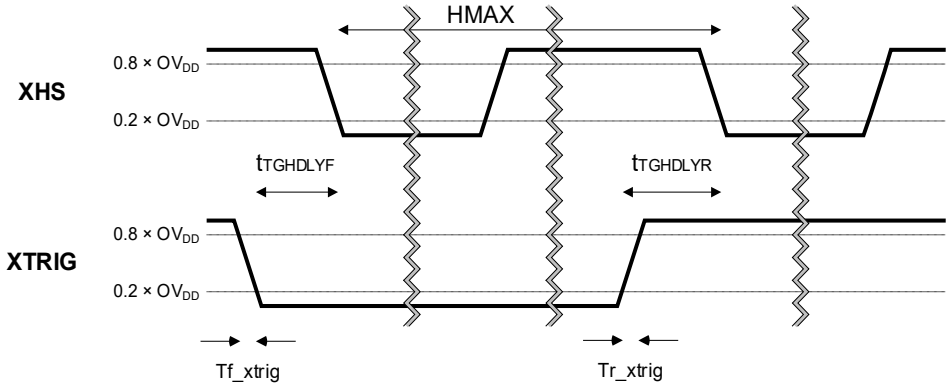
11.3.3. XVS / XHS Input Characteristics in Slave Mode (XMASTER = High)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{WLXHS}	$4/f_{INCK}$	—	—	ns	
XHS High level pulse width	t_{WHXHS}	$4/f_{INCK}$	—	—	ns	
XVS - XHS fall width	t_{HFDLY}	$1/f_{INCK}$	—	—	ns	
XHS - XVS rise width	t_{VRDLY}	$1/f_{INCK}$	—	—	ns	
XVS Fall time	Tf_xvs	—	—	5	ns	80 % to 20 %
XVS Rise time	Tr_xvs	—	—	5	ns	20 % to 80 %
XHS Fall time	Tf_xhs	—	—	5	ns	80 % to 20 %
XHS Rise time	Tr_xhs	—	—	5	ns	20 % to 80 %

Synchronization cannot be performed from XVS and XHS signal in mater mode. Detect the packet header output from the image sensor.

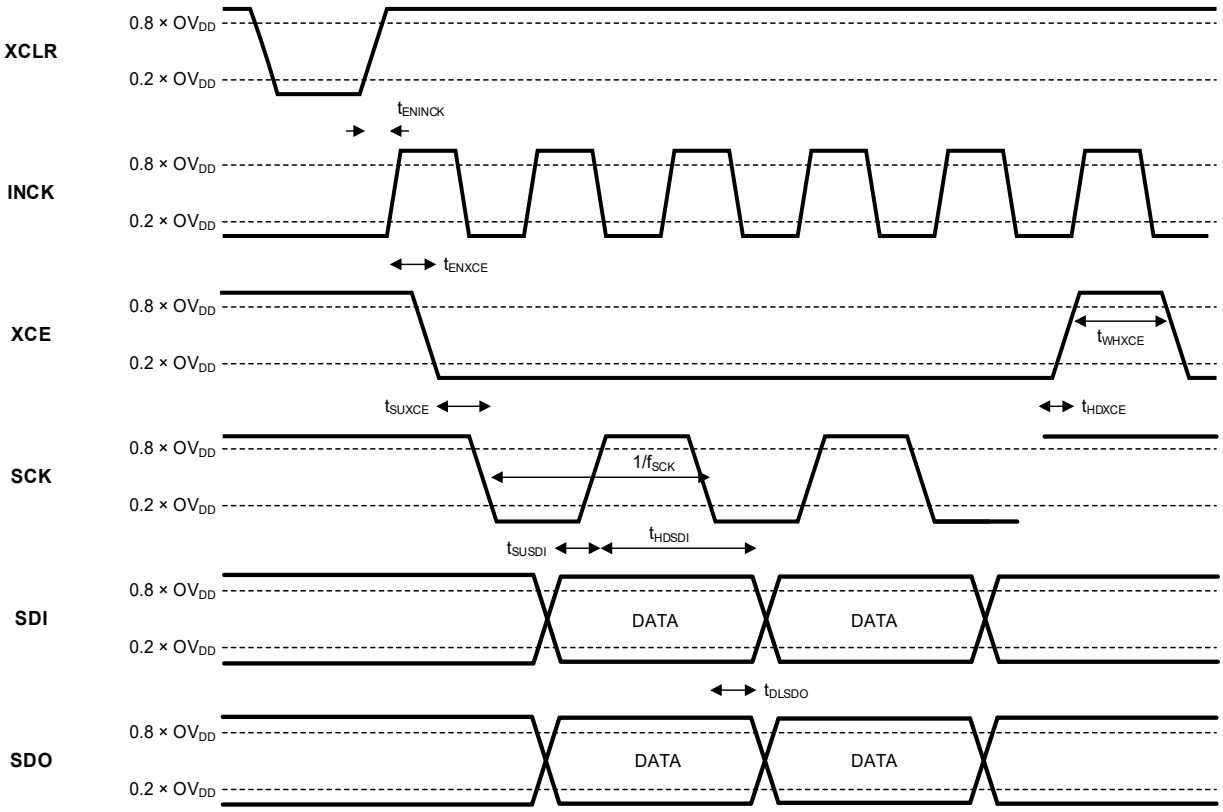
11.3.4. XTRIG Input Characteristics in Slave Mode (XMASTER = High) only



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XTRIG fall - XHS fall width	$t_{TGHDLYF}$	10	—	HMAX-10	INCK	
XTRIG rise - XHS fall width	$t_{TGHDLYR}$	10	—	HMAX-10	INCK	
XTRIG Fall time	Tf_xtrig	—	—	5	ns	80 % to 20 %
XTRIG Rise time	Tr_xtrig	—	—	5	ns	20 % to 80 %

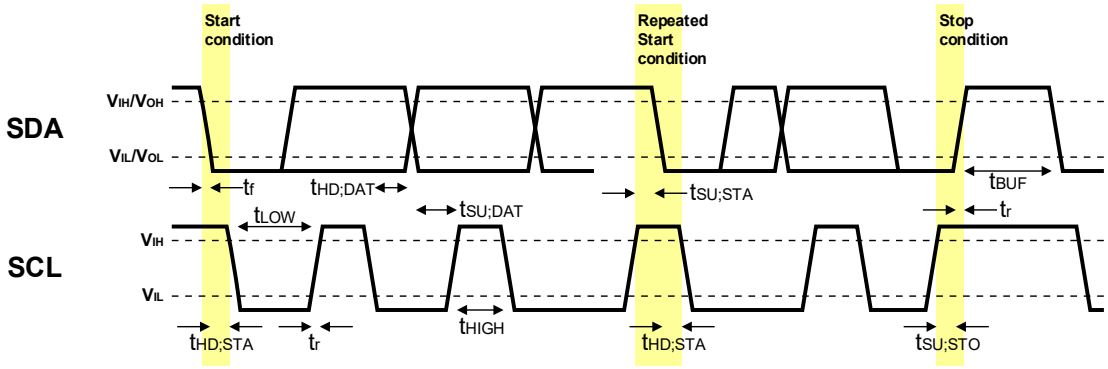
11.3.5. Serial Communication

4-wire



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK clock frequency	f_{SCK}	—	—	13.5	MHz	
INCK effective margin	t_{ENINCK}	1	—	—	µs	
XCE effective margin	t_{ENXCE}	20	—	—	µs	
XCE input setup time	t_{SUXCE}	20	—	—	ns	
XCE input hold time	t_{HDXCE}	20	—	—	ns	
XCE High level pulse width	t_{WHXCE}	20	—	—	ns	
SDI input setup time	t_{SUSDI}	10	—	—	ns	
SDI input hold time	t_{HDSDI}	10	—	—	ns	
SDO output delay time	t_{DLSDO}	0	—	25	ns	Output load capacitance: 20 pF

I²C



I²C Specification

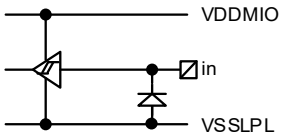
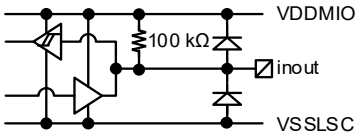
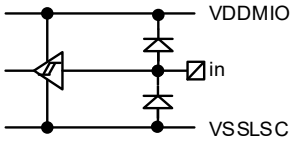
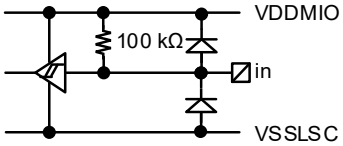
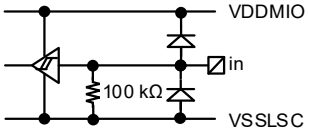
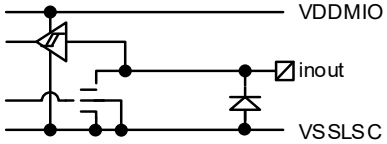
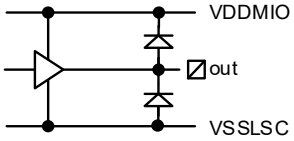
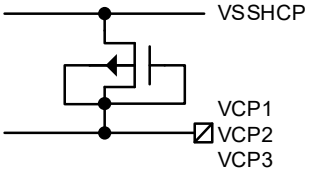
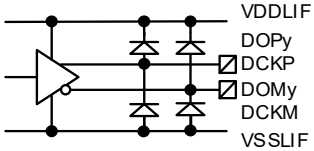
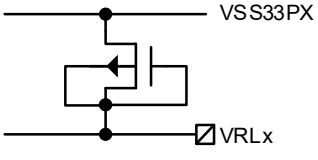
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	-0.3	—	0.3 × OV_{DD}	V	
High level input voltage	V_{IH}	0.7 × OV_{DD}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × OV_{DD}	V	OV_{DD} < 2 V, Sink 3 mA
High level output voltage	V_{OH}	0.8 × OV_{DD}	—	—	V	
Output fall time from VI_{Hmin} to V_{ILmax}	tof	—	—	250	ns	Load 10 pF – 400 pF, 0.7 × OV_{DD} – 0.3 × OV_{DD}
Input current	Ii	-10	—	10	µA	0.1 × OV_{DD} – 0.9 × OV_{DD}
Capacitance for SCK (/SCL) , SDI (/SDA)	Ci	—	—	10	pF	

I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	t_{HDSTA}	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	t_{SUSTA}	0.6	—	—	µs
Data hold time	t_{HDDAT}	0	—	0.9	µs
Data set-up time	t_{SUDAT}	100	—	—	ns
Rise time of both SDA and SCL signals	t_R	—	—	300	ns
Fall time of both SDA and SCL signals	t_F	—	—	300	ns
Set-up time (Stop Condition)	t_{SUSTO}	0.6	—	—	µs
Bus free time between a Stop and Start Condition	t_{BUF}	1.3	—	—	µs

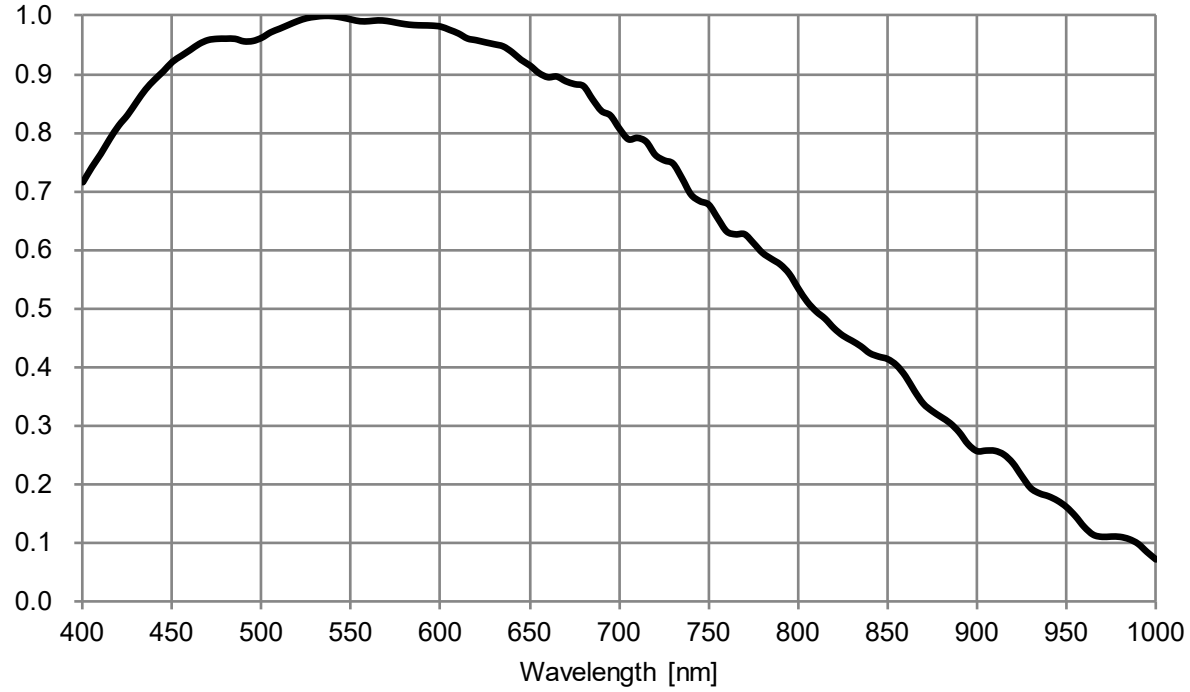
12. I/O Equivalent Circuit Diagram

□ : External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
INCK		XVS XHS	
XCLR XCE XMASTER		XTRIG1, 2	
SLAMODE 0, 1, 2		SDI / SDA SCK / SCL	
SDO		VCP1 VCP2 VCP3	
DOPy DOMy DCKP DCKM y : 0 to 3		VRLFDB VRLOFG VRLSEL VRLTRG VRLTRX VRLTRY	 VRLx: VRLFDB, VRLOFG, VRLSEL, VRLTRG, VRLTRX and VRLTRY

13. Spectral Sensitivity Characteristics

(Characteristics in the wafer status)



14. Image Sensor Characteristics

($AV_{DD}1$ = 3.3 V, $AV_{DD}2$ = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.1 V, All-pixel scan mode, AD: 12 bit, Tj = 60 ˚C, Gain = 0 dB)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	12333 (2252)	14510 (2649)	—	Digit/lx/s (mV/lx/s)	1	12 bit converted value
Saturation signal	Vsat2D	4094 (748[*1])	—	—	Digit (mV)	2	
Video signal shading	SH01	—	—	20	%	3	
	SH2D	—	—	25	%		
Dark signal	Vdt	—	—	0.82 (0.15)	Digit (mV)	4	1/30 s storage
Dark signal shading	ΔVdt	—	—	1.37 (0.25)	Digit (mV)	5	1/30 s storage
PLS (Parasitic Light Sensitivity)	Sm	—	—	-72	dB	6	

Note) 1. Converted value into mV using 1Digit = 0.1826 mV for 12-bit output, 1Digit = 0.7304 mV for 10-bit output and 1Digit = 0.7304 mV for 8-bit output.
2. The video signal shading is the measured value in the wafer status and does not include characteristics of the seal glass.

*1 In case of 8 bit, Vsat2D becomes 1/4 of it at 12 bit.

15. Image Sensor Characteristics Measurement Method

15.1. Measurement Conditions

In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the signal output of the measurement system.

15.2. Definition of standard imaging conditions

◆ Standard imaging condition I:
Using a purple excitation LED light source with a color temperature of 2850 K, an IR cut filter CM700 (t = 1.0 mm) is placed between the LED light source and the sensor receiving surface to irradiate substantially parallel light.

◆ Standard image condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM700 (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard image condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance -100 mm) with CM700 (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

15.3. Measurement Method

(1) Sensitivity
Set the measurement condition to the standard imaging condition I, and calculate using the illuminance (Ev) of the sensor receiving surface, the signal values (V) at the center of the screen, and the integration time (T).

$$Sg = V / (Ev \times T) \text{ [Digit/lx/s]}$$

(2) Saturation signal
Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with the average value of the signal outputs, 562 mV, measure the minimum values of the signal outputs.

(3) Video signal shading
Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the signal outputs is 562 mV. Then measure the maximum value (Vmax [mV]) and the minimum value (Vmin [mV]) of the signal outputs, and substitute the values into the following formula.

$$SH = (Vmax - Vmin) / 562 \times 100 \text{ [\%]}$$

(4) Dark signal
With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/3 s integration at 3 frame/s and 1/30 s integration at 30 frame/s by 9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

(5) Dark signal shading
Measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output with the device junction temperature of 60 ˚C and the device in the light-obstructed state and 1/30 s integration. The measuring values substitute into the following formula.

$$\Delta Vdt = Vdmax - Vdmin \text{ [mV]}$$

(6) PLS
Set the measurement condition to the standard imaging condition II, the output signal Vave measured by standard image condition. Then, adjust the luminous intensity to 500 times the intensity with average value of the signal output, Vave. When the charge drain is executed be the electronic shutter and the condition that not be readout from photo diode to analog memory, readout by dropping to 30 frame/s.

$$Sm = 20 \times \log ((Vsm / Vave) \times (1 / 500) \times (10 / 33.3)) \text{ [dB]}$$

16. Setting Registers Using Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by 4-wire serial communication and I^2C communication. See the Register Map for the addresses and setting values to be set. Because the two communication systems are judged at the first communication, once they are judged, the communication cannot be switched until sensor reset. The pin for 4-wire serial communication and I^2C communication is shared, so the external pin XCE must be fixed to power supply side when using I^2C communication.

16.1. Description of Setting Registers (4-wire)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Serial Data Transfer Order

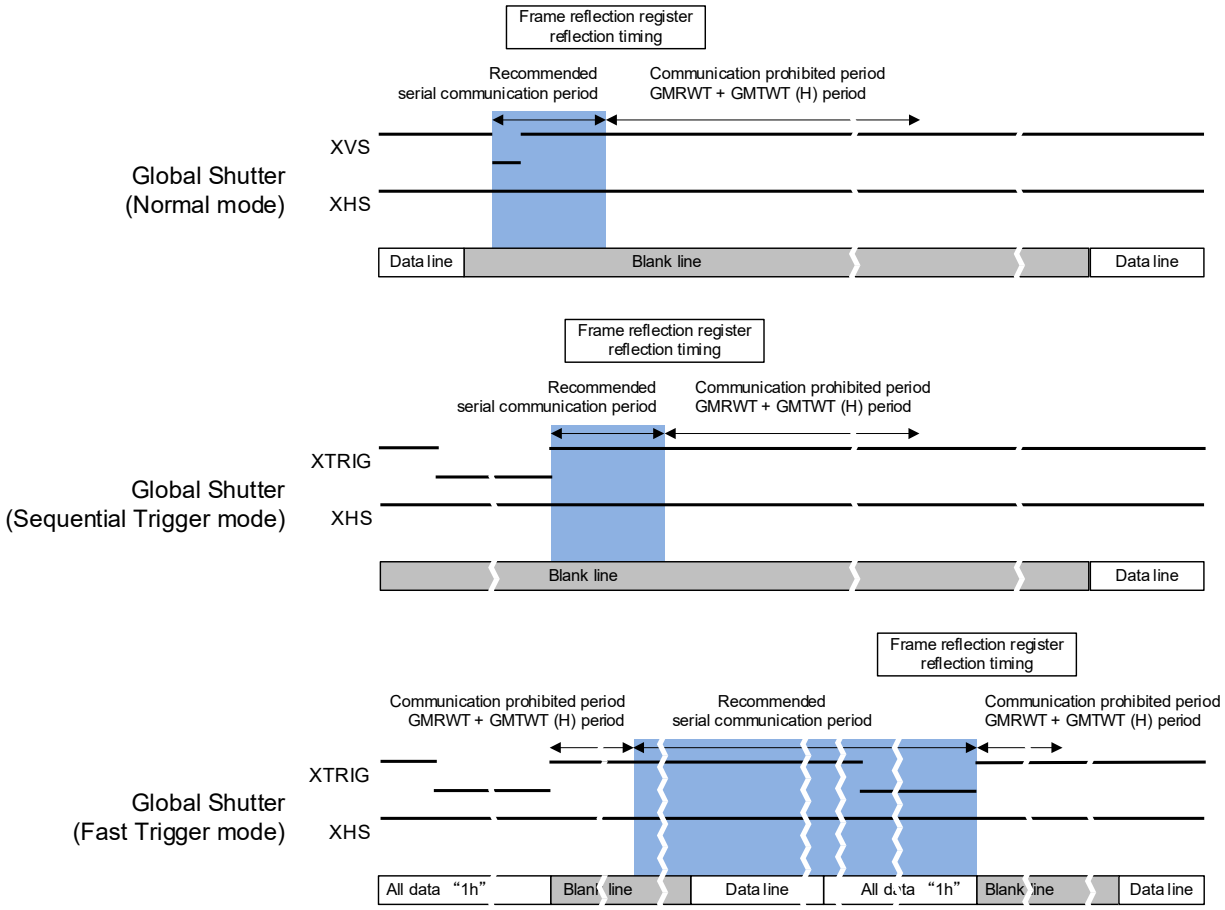
Chip ID	Start address	Data	Data	Data	…
(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)

Type and Description

Type	Description
Chip ID	Chip ID: 02 Write: 02h / Read: 82h
	Chip ID: 03 Write: 03h / Read: 83h
	Chip ID: 04 Write: 04h / Read: 84h
	Chip ID: 05 Write: 05h / Read: 85h
	Chip ID: 06 Write: 06h / Read: 86h
	Chip ID: 07 Write: 07h / Read: 87h
	Chip ID: 08 Write: 08h / Read: 88h
	Chip ID: 09 Write: 09h / Read: 89h
	Chip ID: 0A Write: 0Ah / Read: 8Ah
	Chip ID: 0B Write: 0Bh / Read: 8Bh
	Chip ID: 0C Write: 0Ch / Read: 8Ch
	Chip ID: 0D Write: 0Dh / Read: 8Dh
	Chip ID: 0E Write: 0Eh / Read: 8Eh
	Chip ID: 0F Write: 0Fh / Read: 8Fh
	Chip ID: 10 Write: 10h / Read: 90h
	Chip ID: 11 Write: 11h / Read: 91h
	Chip ID: 12 Write: 12h / Read: 92h
	Chip ID: 13 Write: 13h / Read: 93h
	Chip ID: 14 Write: 14h / Read: 94h
	Chip ID: 15 Write: 15h / Read: 95h
	Chip ID: 16 Write: 16h / Read: 96h
	Chip ID: 17 Write: 17h / Read: 97h
	Chip ID: 18 Write: 18h / Read: 98h
	Chip ID: 19 Write: 19h / Read: 99h
	Chip ID: 1A Write: 1Ah / Read: 9Ah
	Chip ID: 1B Write: 1Bh / Read: 9Bh
	Chip ID: 1C Write: 1Ch / Read: 9Ch
	Chip ID: 1D Write: 1Dh / Read: 9Dh
	Chip ID: 1E Write: 1Eh / Read: 9Eh
Address	Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

16.2. Register Communication Timing (4-wire)

Perform serial communication in sensor standby mode or within communication period. For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed.
For GMRWT and GMTWT, refer to the register list of each readout mode.



Communication Timing and Register Reflection Timing

16.3. Register Write and Read (4-wire)

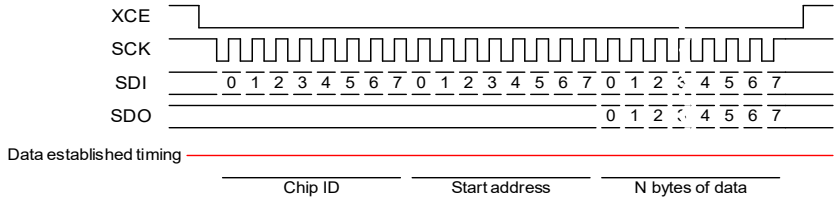
◆ Follow the communication procedure below when writing registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input the Chip ID (CID = 02h to 1Eh) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.
(7) Set XCE High to end communication.

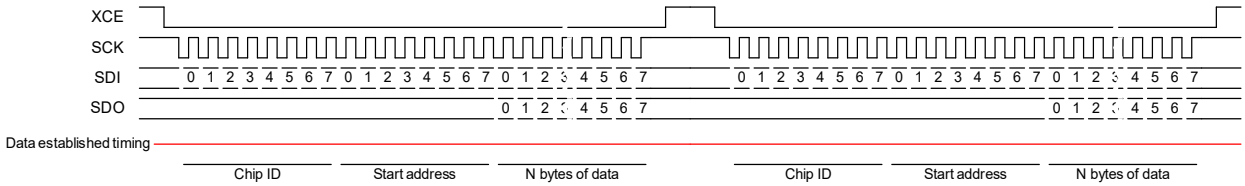
◆ Follow the communication procedure below when reading registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input Chip ID (CID = 82h to 9Eh) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input data to the third and subsequent bytes. Input dummy data in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.
(7) Set XCE High to end communication.

Note) When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.



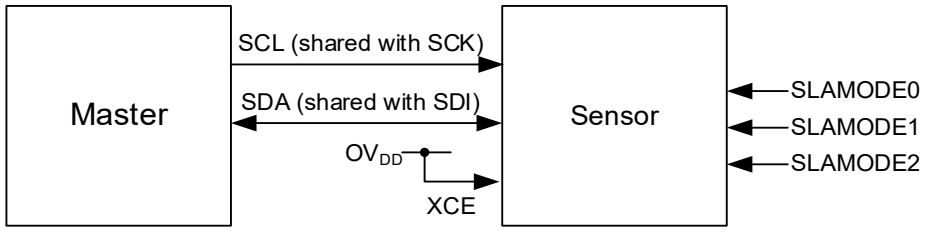
Serial Communication (Continuous Addresses)



Serial Communication (Discontinuous Addresses)

16.4. Description of Setting Registers (I^2C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

The sensor can use two kinds of slave addresses by switching the polarity of SLAMODE0, SLAMODE1 and SLAMODE2 Pins for one I^2C bus, and can use a common slave address in both polarities of SLAMODE [2:0] Pins for one I^2C bus.

1st SLAVE Address (SLAMODE [2:0])

SLAMODE [2:0]	MSB							LSB
0h	0	1	1	0	1	1	0	R / W
1h	0	1	1	0	1	1	1	R / W
2h	0	1	1	1	0	0	0	R / W
3h	0	1	1	1	0	0	1	R / W
4h	0	1	1	1	0	1	0	R / W
5h	0	1	1	1	0	1	1	R / W
6h	0	1	1	1	1	0	0	R / W
7h	0	1	1	1	1	0	1	R / W

2nd SLAVE Address (Common in all SLAMODE [2:0])

MSB							LSB
0	0	1	1	0	1	0	R / W

* R/W is data direction bit

R/W

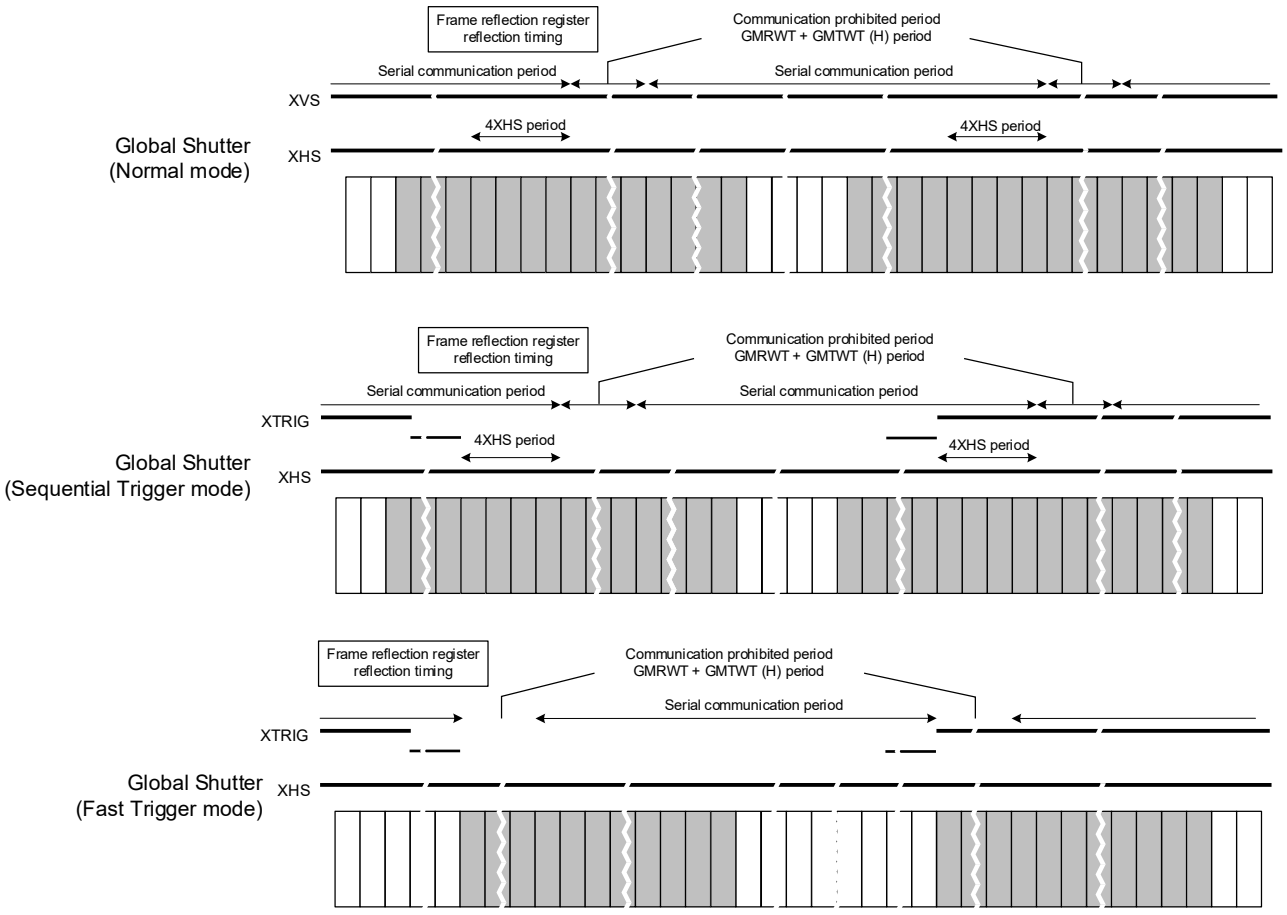
R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

I^2C pin description

Symbol	Pin No.	Description
SCL (common to SCK)	J15	Serial clock input
SDA (common to SDI)	J16	Serial data communication
SLAMODE0	N15	I^2C 1st Slave address select
SLAMODE1	P15	I^2C 1st Slave address select
SLAMODE2	R15	I^2C 1st Slave address select
XCE	F15	Fixed to High when using I^2C

16.5. Register Communication Timing (I^2C)

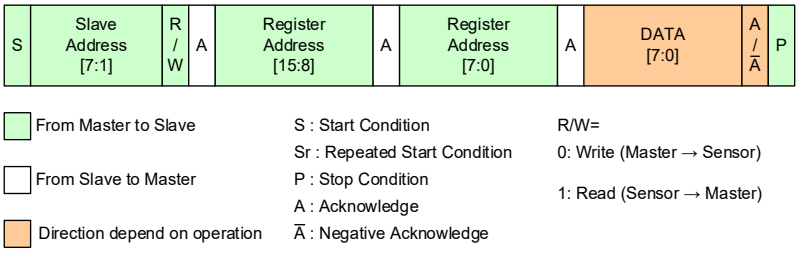
In I^2C communication system, communication can be performed excluding the communication prohibition period (GMRWT + GMTWT (H) period) shown below.
For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. Using REGHOLD function is recommended for register setting using I^2C communication. For REGHOLD function, see “Register Hold Setting” in “Description of Various Functions”.
For GMRWT and GMTWT, refer to the register list of each readout mode.



Communication Timing and Register Reflection Timing

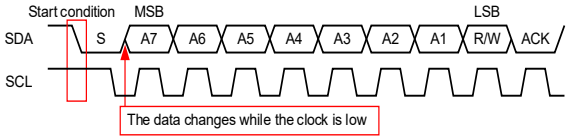
16.6. I²C Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

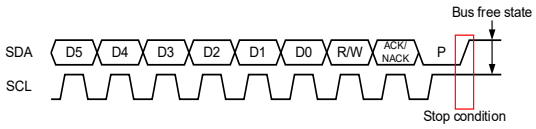


Communication protocol

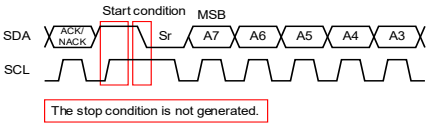
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / Ā (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SCL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start Condition is defined by SDA changing from High to Low while SCL is High. When the Stop Condition is not generated in the previous communication phase and Start Condition for the next communication is generated, that Start Condition is recognized as a Repeated Start Condition.



Start Condition

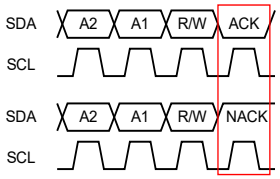


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



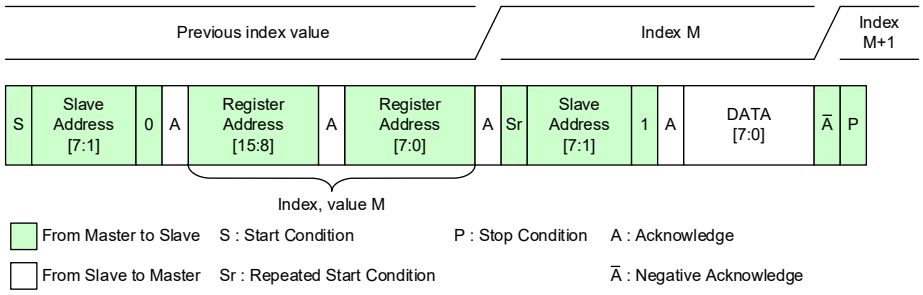
Acknowledge and Negative Acknowledge

16.7. I²C Serial Communication Read/Write Operation

This sensor supports the following four read operations and two write operations.

16.7.1. Single Read from Random Location

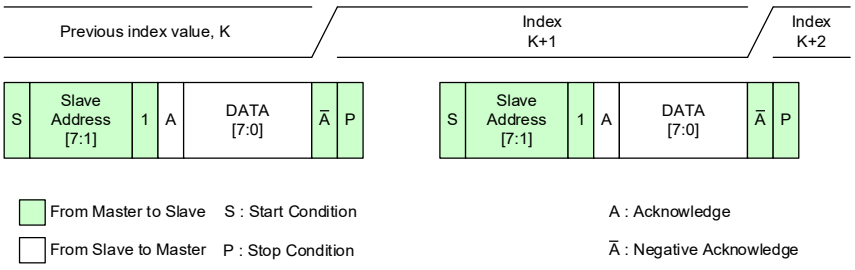
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the Start Condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication.



Single Read from Random Location

16.7.2. Single Read from Current Location

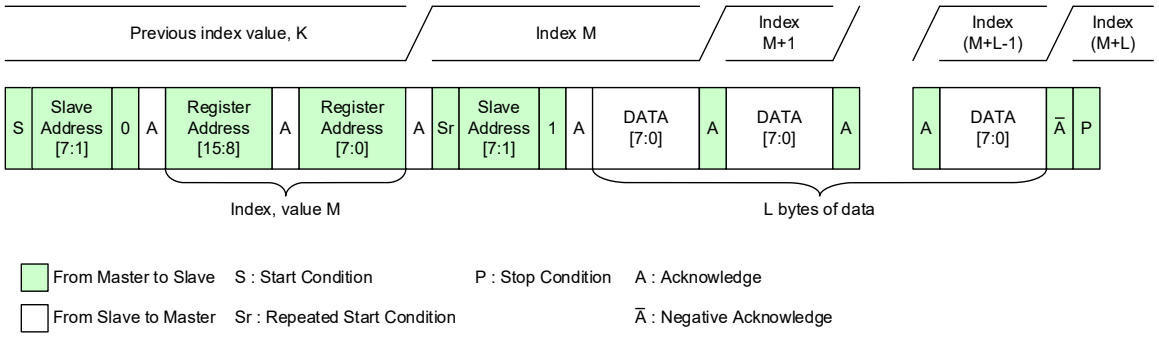
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

16.7.3. Sequential Read Starting from Random Location

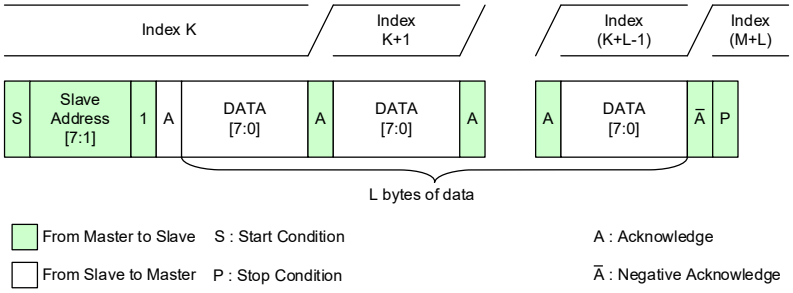
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

16.7.4. Sequential Read Starting from Current Location

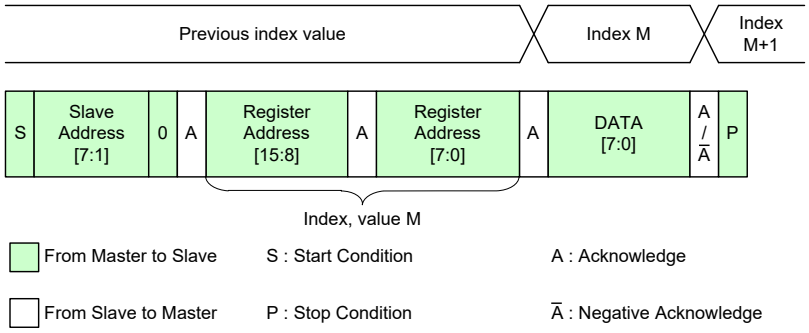
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

16.7.5. Single Write to Random Location

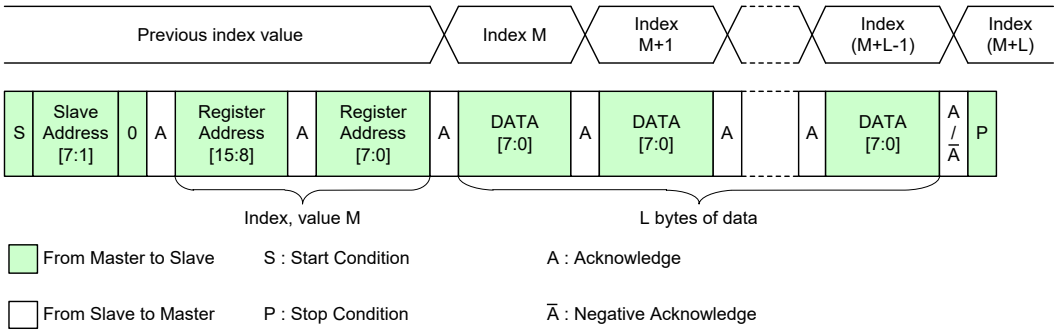
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

16.7.6. Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

17. Register Map

This sensor has a total of 7424 bytes of registers, composed of registers with address 00h to FFh that correspond to Chip ID = 02h to 1Eh. Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 7424 bytes.

There are three different register reflection timings.
About the Reflection timing column of the Register Map, registers noted as "I" are reflected immediately after writing to register, registers noted as "S" are set during standby mode and reflected after standby canceled, registers noted as "V" are reflected at “Fame reflection register reflection timing” on the figure described in the section of “Setting Registers Using Serial Communication”.

Do not perform communication to addresses and setting not listed in the Register Map. Doing so may result in operation errors. However, other registers that requires communication to address not listed may be added, so addresses 00h to FFh should be supported for Chip ID = 02h to 1Eh (In I^2C communication, address; 3000h to 4CFFh)

17.1. Chip ID = 02 (Write: Chip ID = 02h, Read: Chip ID = 82h, I²C: 30**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3000h	0	STANDBY [0]	Standby mode 0: Normal operation 1: Standby	1	01h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
10h	3010h	0	XMSTA [0]	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1	01h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
14h	3014h	0	INCKSEL_ST0 [7:0]	Set according to INCK frequency and drive mode.	0Ah	0Ah	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
15h	3015h	0	INCKSEL_ST1 [7:0]	Set according to INCK frequency and drive mode.	22h	22h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
16h	3016h	0	INCKSEL_ST2 [7:0]	Set according to INCK frequency and drive mode.	B1h	B1h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
18h	3018h	0	INCKSEL_ST3 [7:0]	Set according to INCK frequency and drive mode.	40h	40h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
19h	3019h	0	INCKSEL_ST4 [7:0]	Set according to INCK frequency and drive mode.	04h	04h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
1Bh	301Bh	0	INCKSEL_ST5 [7:0]	Set according to INCK frequency and drive mode.	3Ah	3Ah	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
34h	3034h	0	REGHOLD [0]	Register hold 0: Invalid 1: Valid	0	00h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
3Ch	303Ch	0		Fixed to 0	0	00h	—
		1		Fixed to 1	0		S
		2		Fixed to 0	0		—
		3	HVMODE [1:0]	Drive mode setting of H/V direction 0h: All-pixel 1h: 1/2 Subsampling mode 2h: FD binning 3h: Setting prohibited	0h		S
		4					
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
D0h	30D0h	0	VOPB_VBLK_HWIDTH [12:0]	LSB	1020h	20h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		VOPB effective area and V Blank width setting			
D1h	30D1h	0				10h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
D2h	30D2h	0	FINFO_HWIDTH [12:0]	LSB	04B0h	B0h	S
		1					
		2					
		3					
		4					
		5					
		6		EBD (Embedded data line) width setting			
		7					
D3h	30D3h	0				04h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
D4h	30D4h	0	VMAX [23:0]	LSB	000CD4h	D4h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
D5h	30D5h	0		When sensor master mode vertical span setting. (Number of operation lines count from 1)		0Ch	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
D6h	30D6h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
D8h	30D8h	0	HMAX [15:0]	LSB	0081h	81h	S
		1					
		2					
		3					
		4					
		5					
		6		When sensor master mode and sensor slave mode, horizontal span setting. (Number of operation clocks count from 1)			
		7					
D9h	30D9h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
E2h	30E2h	0 1 2 3 4 5 6 7	GMRWT [7:0]	Refer to the register list in each Readout mode	10h	10h	S
E3h	30E3h	0 1 2 3 4 5 6 7	GMTWT [7:0]	Refer to the register list in each Readout mode	70h	70h	S
E5h	30E5h	0 1 2 3 4 5 6 7	GAINDLY [7:0]	Refer to the register list in each Readout mode	04h	04h	S
E6h	30E6h	0 1 2 3 4 5 6 7	GSDLY [7:0]	Refer to the register list in each Readout mode	30h	30h	S

17.2. Chip ID = 03 (Write: Chip ID = 03h, Read: Chip ID = 83h, I²C: 31**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3100h	0	ROI_MODE [0]	Selection of ROI mode 0: ROI Mode 1: Overlap ROI Mode	0	00h	S
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
04h	3104h	0	FID0_ROIH1ON [0]	The horizontal setting of FID0 ROI area (1, y) (y = 1 to 8) 0: Disable 1: Enable	0	00h	V
		1	FID0_ROIV1ON [0]	The vertical setting of FID0 ROI area (x, 1) (x = 1 to 8) 0: Disable 1: Enable	0		I
		2	FID0_ROIH2ON [0]	The horizontal setting of FID0 ROI area (2, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		3	FID0_ROIV2ON [0]	The vertical setting of FID0 ROI area (x, 2) (x = 1 to 8) 0: Disable 1: Enable	0		I
		4	FID0_ROIH3ON [0]	The horizontal setting of FID0 ROI area (3, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		5	FID0_ROIV3ON [0]	The vertical setting of FID0 ROI area (x, 3) (x = 1 to 8) 0: Disable 1: Enable	0		I
		6	FID0_ROIH4ON [0]	The horizontal setting of FID0 ROI area (4, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		7	FID0_ROIV4ON [0]	The vertical setting of FID0 ROI area (x, 4) (x = 1 to 8) 0: Disable 1: Enable	0		I

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
05h	3105h	0	FID0_ROIH5ON [0]	The horizontal setting of FID0 ROI area (5, y) (y = 1 to 8) 0: Disable 1: Enable	0	00h	V
		1	FID0_ROIV5ON [0]	The vertical setting of FID0 ROI area (x, 5) (x = 1 to 8) 0: Disable 1: Enable	0		I
		2	FID0_ROIH6ON [0]	The horizontal setting of FID0 ROI area (6, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		3	FID0_ROIV6ON [0]	The vertical setting of FID0 ROI area (x, 6) (x = 1 to 8) 0: Disable 1: Enable	0		I
		4	FID0_ROIH7ON [0]	The horizontal setting of FID0 ROI area (7, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		5	FID0_ROIV7ON [0]	The vertical setting of FID0 ROI area (x, 7) (x = 1 to 8) 0: Disable 1: Enable	0		I
		6	FID0_ROIH8ON [0]	The horizontal setting of FID0 ROI area (8, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		7	FID0_ROIV8ON [0]	The vertical setting of FID0 ROI area (x, 8) (x = 1 to 8) 0: Disable 1: Enable	0		I

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
20h	3120h	0	FID0_ROIPH1 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping position for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 8			
21h	3121h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
22h	3122h	0	FID0_ROIPV1 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping position for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8			
23h	3123h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
24h	3124h	0	FID0_ROIWH1 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping size for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 8			
25h	3125h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
26h	3126h	0	FID0_ROIWV1 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8			
27h	3127h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
28h	3128h	0	FID0_ROIPH2 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping position for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 8			
29h	3129h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
2Ah	312Ah	0	FID0_ROIPV2 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping position for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8			
2Bh	312Bh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
2Ch	312Ch	0	FID0_ROIWH2 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping size for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 8			
2Dh	312Dh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
2Eh	312Eh	0	FID0_ROIWV2 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8			
2Fh	312Fh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
30h	3130h	0	FID0_ROIPH3 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping position for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 8			
31h	3131h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
32h	3132h	0	FID0_ROIPV3 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping position for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8			
33h	3133h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
34h	3134h	0	FID0_ROIWH3 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping size for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 8			
35h	3135h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
36h	3136h	0	FID0_ROIWV3 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8			
37h	3137h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
38h	3138h	0	FID0_ROIPH4 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping position for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 8			
39h	3139h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
3Ah	313Ah	0	FID0_ROIPV4 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping position for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8			
3Bh	313Bh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
3Ch	313Ch	0	FID0_ROIWH4 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping size for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 8			
3Dh	313Dh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
3Eh	313Eh	0	FID0_ROIWV4 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8			
3Fh	313Fh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
40h	3140h	0	FID0_ROIPH5 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping position for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 8			
41h	3141h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
42h	3142h	0	FID0_ROIPV5 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping position for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8			
43h	3143h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
44h	3144h	0	FID0_ROIWH5 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping size for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 8			
45h	3145h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
46h	3146h	0	FID0_ROIWV5 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8			
47h	3147h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
48h	3148h	0	FID0_ROIPH6 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping position for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 8			
49h	3149h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
4Ah	314Ah	0	FID0_ROIPV6 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping position for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8			
4Bh	314Bh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
4Ch	314Ch	0	FID0_ROIWH6 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping size for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 8			
4Dh	314Dh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
4Eh	314Eh	0	FID0_ROIWV6 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8			
4Fh	314Fh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
50h	3150h	0	FID0_ROIPH7 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping position for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 8			
51h	3151h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
52h	3152h	0	FID0_ROIPV7 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping position for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8			
53h	3153h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
54h	3154h	0	FID0_ROIWH7 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping size for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 8			
55h	3155h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
56h	3156h	0	FID0_ROIWV7 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8			
57h	3157h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
58h	3158h	0	FID0_ROIPH8 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping position for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 8			
59h	3159h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
5Ah	315Ah	0	FID0_ROIPV8 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping position for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8			
5Bh	315Bh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
5Ch	315Ch	0	FID0_ROIWH8 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping size for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 8			
5Dh	315Dh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
5Eh	315Eh	0	FID0_ROIWV8 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8			
5Fh	315Fh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

17.3. Chip ID = 04 (Write: Chip ID = 04h, Read: Chip ID = 84h, I²C: 32**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3200h	0		Fixed to 1	0	04h	S
		1		Fixed to 0	0		—
		2		Fixed to 1	1		—
		3		Fixed to 0	0		—
		4	ADBIT [1:0]	AD conversion bits setting 0h: 10 bit 1h: 12 bit 2h: 8 bit 3h: Setting prohibited	0h		S
		5					
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
04h	3204h	0	VREVERSE [0]	Vertical (V) direction readout inversion control 0: Normal 1: Inverted	0	00h	V
		1	HREVERSE [0]	Horizontal (H) direction readout inversion control 0: Normal 1: Inverted	0		V
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
1Ch	321Ch	0	INCKSEL_N0 [7:0]	Set according to INCK frequency and drive mode.	80h	80h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
1Dh	321Dh	0	INCKSEL_N1 [7:0]	Set according to INCK frequency and drive mode.	05h	05h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
1Eh	321Eh	0	INCKSEL_N2 [7:0]	Set according to INCK frequency and drive mode.	E0h	E0h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
1Fh	321Fh	0 1 2 3 4 5 6 7	INCKSEL_N3 [7:0]	Set according to INCK frequency and drive mode.	00h	00h	S
20h	3220h	0 1 2 3 4 5 6 7	INCKSEL_S0 [7:0]	Set according to INCK frequency and drive mode.	80h	80h	S
21h	3221h	0 1 2 3 4 5 6 7	INCKSEL_S1 [7:0]	Set according to INCK frequency and drive mode.	05h	05h	S
22h	3222h	0 1 2 3 4 5 6 7	INCKSEL_S2 [7:0]	Set according to INCK frequency and drive mode.	E0h	E0h	S
23h	3223h	0 1 2 3 4 5 6 7	INCKSEL_S3 [7:0]	Set according to INCK frequency and drive mode.	00h	00h	S
24h	3224h	0 1 2 3 4 5 6 7	INCKSEL_D0 [7:0]	Set according to INCK frequency and drive mode.	10h	10h	S

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
25h	3225h	0	INCKSEL_D1 [7:0]	Set according to INCK frequency and drive mode.	14h	14h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
26h	3226h	0	INCKSEL_D2 [7:0]	Set according to INCK frequency and drive mode.	20h	20h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
27h	3227h	0	INCKSEL_D3 [7:0]	Set according to INCK frequency and drive mode.	C0h	C0h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Ch	323Ch	0		Fixed to 1	1	31h	—
		1	LLBLANK [7:0]	LSB Refer to the register list in each Readout mode	18h		S
		2					
		3					
		4					
		5					
		6					
		7					
3Dh	323Dh	0		MSB		00h	
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
3Eh	323Eh	0	VINT_EN [0]	Setting of Interrupt mode in Trigger Mode 0: V interrupt is disable 1: V interrupt is enable	1	5Bh	S
		1	VINT_EN_NOR [0]	Setting of Interrupt mode in Normal Mode 0: V interrupt is disable 1: V interrupt is enable	1		S
		2		Refer to the register list in each Readout mode	16h		S
		3					
		4					
		5					
		6					
		7					

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
40h	3240h	0	SHS [23:0]	LSB	000070h	70h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
41h	3241h	0		Storage time adjustment Designated in line unit		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
42h	3242h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

17.4. Chip ID = 05 (Write: Chip ID = 05h, Read: Chip ID = 85h, I²C: 33**h)

Please refer to the other register map file for the register that has not been described.

17.5. Chip ID = 06 (Write: Chip ID = 06h, Read: Chip ID = 86h, I²C: 34**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3400h	0	TRIGMODE [2:0]	Global shutter mode setting 0h: Normal mode 1h: Sequential Trigger mode 2h: Fast Trigger mode Others: Setting prohibited	0h	00h	I [*1]
		1					
		2					
		3	TRIGTIMING [1:0]	Trigger mode setting 0h: Normal mode 1h: Trigger mode Others: Setting prohibited	0h		I [*1]
		4					
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
30h	3430h	0	ODBIT [1:0]	Number of output bit setting 0h: 10 bit 1h: 12 bit 2h: 8 bit 3h: Setting prohibited	0h	00h	S
		1					
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
35h	3435h	0	TOUT1SEL [1:0]	TOUT1 pin setting 0h: Low fixed 3h: Pulse output Others: Setting prohibited	0h	00h	S
		1					
		2	TOUT2SEL [1:0]	TOUT2 pin setting 0h: Low fixed 3h: Pulse output Others: Setting prohibited	0h		S
		3					
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
36h	3436h	0	TOUT0SEL [2:0]	TOUT0 pin setting 0h: Low fixed 1h: Exposure period monitoring Others: Setting prohibited	0h	00h	S
		1					
		2					
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

[*1] Refer to “Mode Transitions of Global Shutter Operation”

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
3Ah	343Ah	0	TRIG_TOUT1_SEL [3:0]	TOUT1 output setting 0h: Low fixed 1h: Pulse1 output Others: Setting prohibited	0h	00h	S
		1					
		2					
		3					
		4	TRIG_TOUT2_SEL [3:0]	TOUT2 output setting 0h: Low fixed 2h: Pulse2 output Others: Setting prohibited	0h		S
		5					
		6					
		7					
3Ch	343Ch	0		Fixed to 0	0	C0h	—
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4	SYNCSEL [1:0]	XHS, XVS pin setting 0h: Normal Output 3h: Hi-Z Others: Setting prohibited	0h		S
		5					
		6		Fixed to 1	1		—
		7		Fixed to 1	1		—
78h	3478h	0	PULSE1_EN_NOR [0]	Pulse1 output in normal mode 0: Disable 1: Enable	0	00h	S
		1	PULSE1_EN_TRIG [0]	Pulse1 output in trigger mode 0: Disable 1: Enable	0		S
		2	PULSE1_POL [0]	Pulse1 polarity selection 0: High active 1: Low active	0		S
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
79h	3479h	0	PULSE1_UP [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
7Ah	347Ah	0				00h	
		1					
		2		Pulse1 active period start timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)			
		3					
		4					
		5					
		6					
		7					
7Bh	347Bh	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
7Ch	347Ch	0	PULSE1_DN [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
7Dh	347Dh	0				00h	
		1					
		2					
		3		Pulse1 active period end timing setting Designated in line units from readout start (For details, see the “Pulse Output Function”)			
		4					
		5					
		6					
		7					
7Eh	347Eh	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
80h	3480h	0	PULSE2_EN_NOR [0]	Pulse2 output in normal mode 0: Disable 1: Enable	0	00h	S
		1	PULSE2_EN_TRIG [0]	Pulse2 output in trigger mode 0: Disable 1: Enable	0		S
		2	PULSE2_POL [0]	Pulse2 polarity selection 0: High active 1: Low active	0		S
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 1	0		S
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
81h	3481h	0	PULSE2_UP [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
82h	3482h	0		Pulse2 active period end timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
83h	3483h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
84h	3484h	0	PULSE2_DN [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
85h	3485	0		Pulse2 active period end timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
86h	3486h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

17.6. Chip ID = 07 (Write: Chip ID = 07h, Read: Chip ID = 87h, I²C: 35**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
02h	3502h	0 1 2 3 4 5 6 7	GAIN_RTS [7:0]	Setting of Gain Reflection Timing at Normal mode. 08h: Gain reflect at the frame 09h: Gain reflect at the next frame (Same timing as SHS reflecting output.) Others: Setting prohibited	00h	00h	S
14h	3514h	0 1 2 3 4 5 6 7	GAIN [8:0]	LSB Gain setting 0 dB (0d) to 48 dB (480d) 0.1 dB Step (Refer to Address 02h about detail of Reflection Timing.)	000h	00h	V
15h	3515h	0	GAIN [8:0]	MSB		00h	
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
21h	3521h	0 1 2 3 4 5 6 7		Refer to the register list in each Readout mode	A9h	A9h	S
22h	3522h	0 1 2 3 4 5 6 7		Refer to the register list in each Readout mode	B0h	B0h	S
46h	3546h	0 1 2 3 4 5 6 7		Refer to the register list in each Readout mode	2Ah	2Ah	S

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
B4h	35B4h	0	BLKLEVEL [11:0]	LSB	03Ch	3Ch	V
		1					
		2					
		3					
		4		Black level offset value setting Recommended value. 00Fh: 8 bit 03Ch: 10 bit 0F0h: 12 bit			
		5					
		6					
		7					
B5h	35B5h	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

17.7. Chip ID = 08 (Write: Chip ID = 08h, Read: Chip ID = 88h, I²C: 36**h)

Please refer to the other register map file for the register that has not been described.

17.8. Chip ID = 09 (Write: Chip ID = 09h, Read: Chip ID = 89h, I²C: 37**h)

Please refer to the other register map file for the register that has not been described.

17.9. Chip ID = 0A (Write: Chip ID = 0Ah, Read: Chip ID = 8Ah, I²C: 38**h)

Please refer to the other register map file for the register that has not been described.

17.10. Chip ID = 0B (Write: Chip ID = 0Bh, Read: Chip ID = 8Bh, I²C: 39**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
04h	3904h	0	LANESEL [2:0]	Setting of CSI-2 output Lane 2h: 4 Lane 3h: 2 Lane Others: Setting prohibited	0h	00h	S
		1					
		2					
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
42h	3942h	0		Fixed to 1	1	01h	—
		1	EAV_SEL_MIPI [0]	Setting for the packet footer output position in ROI mode 0: CSI-2 v1.2 compliant 1: Immediately after the effective pixel output	0		S
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

17.11. Chip ID = 0C (Write: Chip ID = 0Ch, Read: Chip ID = 8Ch, I²C: 3A**h)

Please refer to the other register map file for the register that has not been described.

17.12. Chip ID = 0D (Write: Chip ID = 0Dh, Read: Chip ID = 8Dh, I²C: 3B**h)

Please refer to the other register map file for the register that has not been described.

17.13. Chip ID = 0E (Write: Chip ID = 0Eh, Read: Chip ID = 8Eh, I²C: 3C**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
A4h	3CA4h	0	TXCLKESC_FREQ [15:0]	LSB	12C0h	C0h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		Set according to INCK frequency and drive mode.			
A5h	3CA5h	0				12h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
B4h	3CB4h	0	THS_PREPARE [15:0]	LSB	004Fh	4Fh	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		Global timing setting			
B5h	3CB5h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
B6h	3CB6h	0	TCLK_POST [15:0]	LSB	008Fh	8Fh	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		Global timing setting			
B7h	3CB7h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
B8h	3CB8h	0	THS_TRAIL [15:0]	LSB	004Fh	4Fh	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		Global timing setting			
B9h	3CB9h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
BAh	3CBAh	0	THS_ZERO [15:0]	LSB	0087h	87h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		Global timing setting			
BBh	3CBBh	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
BCh	3CBCh	0	TCLK_PREPARE [15:0]	LSB	004Fh	4Fh	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		Global timing setting			
BDh	3CBDh	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
BEh	3CBEh	0	TCLK_TRAIL [15:0]	LSB	0047h	47h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		Global timing setting			
BFh	3CBFh	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
C0h	3CC0h	0	TLPX [15:0]	LSB	003Fh	3Fh	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		Global timing setting			
C1h	3CC1h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
C2h	3CC2h	0	TCLK_ZERO [15:0]	LSB	0137h	37h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		Global timing setting			
C3h	3CC3h	0				01h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
C4h	3CC4h	0	TCLK_PRE [15:0]	LSB	000Fh	0Fh	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
C5h	3CC5h	0		Global timing setting		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
C6h	3CC6h	0	THS_EXIT [15:0]	LSB	007Fh	7Fh	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
C7h	3CC7h	0		Global timing setting		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

17.14. Chip ID = 0F (Write: Chip ID = 0Fh, Read: Chip ID = 8Fh, I²C: 3D**h)

Please refer to the other register map file for the register that has not been described.

17.15. Chip ID = 10 (Write: Chip ID = 10h, Read: Chip ID = 90h, I²C: 3E**h)

Please refer to the other register map file for the register that has not been described.

17.16. Chip ID = 11 (Write: Chip ID = 11h, Read: Chip ID = 91h, I²C: 3F**h)

Please refer to the other register map file for the register that has not been described.

17.17. Chip ID = 12 (Write: Chip ID = 12h, Read: Chip ID = 92h, I²C: 40**h)

Please refer to the other register map file for the register that has not been described.

17.18. Chip ID = 13 (Write: Chip ID = 13h, Read: Chip ID = 93h, I²C: 41**h)

Please refer to the other register map file for the register that has not been described.

17.19. Chip ID = 14 (Write: Chip ID = 14h, Read: Chip ID = 94h, I²C: 42**h)

Please refer to the other register map file for the register that has not been described.

17.20. Chip ID = 15 (Write: Chip ID = 15h, Read: Chip ID = 95h, I²C: 43**h)

Please refer to the other register map file for the register that has not been described.

17.21. Chip ID = 16 (Write: Chip ID = 16h, Read: Chip ID = 96h, I²C: 44**h)

Please refer to the other register map file for the register that has not been described.

17.22. Chip ID = 17 (Write: Chip ID = 17h, Read: Chip ID = 97h, I²C: 45**h)

Please refer to the other register map file for the register that has not been described.

17.23. Chip ID = 18 (Write: Chip ID = 18h, Read: Chip ID = 98h, I²C: 46**h)

Please refer to the other register map file for the register that has not been described.

17.24. Chip ID = 19 (Write: Chip ID = 19h, Read: Chip ID = 99h, I²C: 47**h)

Please refer to the other register map file for the register that has not been described.

17.25. Chip ID = 1A (Write: Chip ID = 1Ah, Read: Chip ID = 9Ah, I²C: 48**h)

Please refer to the other register map file for the register that has not been described.

17.26. Chip ID = 1B (Write: Chip ID = 1Bh, Read: Chip ID = 9Bh, I²C: 49**h)

Please refer to the other register map file for the register that has not been described.

17.27. Chip ID = 1C (Write: Chip ID = 1Ch, Read: Chip ID = 9Ch, I²C: 4A**h)

Please refer to the other register map file for the register that has not been described.

17.28. Chip ID = 1D (Write: Chip ID = 1Dh, Read: Chip ID = 9Dh, I²C: 4B**h)

Please refer to the other register map file for the register that has not been described.

17.29. Chip ID = 1E (Write: Chip ID = 1Eh, Read: Chip ID = 9Eh, I²C: 4C**h)

Please refer to the other register map file for the register that has not been described.

18. Readout Drive Modes

The table below lists the operating modes available with this sensor. (Each value is the Max. frame rate of each number of Lane.)

Data rate = 1188 Mbps

Drive mode	CSI-2 Lane[*1]	Data rate [Mbps/Lane]	A/D conversion	Frame rate [frame/s]	Number of recording pixels		Number of INCK in 1 H		
					H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	4	1188	8	62.6	2840	2840	198.0	396.0	288.0
	2	1188		33.2			376.0	752.0	547.0
	4	1188	10	51.3			242.5	485.0	352.8
	2	1188		26.9			465.0	930.0	676.4
	4	1188	12	43.4			287.0	574.0	417.5
	2	1188		22.6			554.5	1109.0	806.6
Vertical / Horizontal 1/2 subsampling	4	1188	8	214.4	1420	1420	109.0	218.0	158.6
	2	1188		121.7			198.0	396.0	288.0
	4	1188	10	180.7			131.0	262.0	190.6
	2	1188		99.9			242.5	485.0	352.8
	4	1188	12	155.4			153.5	307.0	223.3
	2	1188		84.7			287.5	575.0	418.2
2 × 2 FD binning mode	4	1188	8	214.4	1420	1420	109.0	218.0	158.6
	2	1188		121.7			198.0	396.0	288.0
	4	1188	10	180.7			131.0	262.0	190.6
	2	1188		99.9			242.5	485.0	352.8
	4	1188	12	155.4			153.5	307.0	223.3
	2	1188		84.7			287.5	575.0	418.2
ROI	4	1188	8	*2	*3	*3	198.0	396.0	288.0
	2	1188		*2			376.0	752.0	547.0
	4	1188	10	*2			242.5	485.0	352.8
	2	1188		*2			465.0	930.0	676.4
	4	1188	12	*2			287.0	574.0	417.5
	2	1188		*2			554.5	1109.0	806.6

*1 The total data rate is the data rate multiplied by the number of lanes.
Example) In All-pixel 62.6 [frame/s] mode: 1188 [Mbps/Lane] × 4 = 4.752 [Gbps]

*2 See the section of “ROI mode”

*3 Designated cropping area (ROI)

Data rate = 891 Mbps

Drive mode	CSI-2 Lane[*1]	Data rate [Mbps/Lane]	A/D conversion	Frame rate [frame/s]	Number of recording pixels		Number of INCK in 1 H		
					H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	4	891	8	47.5	2840	2840	262.0	524.0	381.1
	2	891		25.1			499.0	998.0	725.9
	4	891	10	38.9			321.0	642.0	467.0
	2	891		20.3			617.0	1234.0	897.5
	4	891	12	32.9			380.0	760.0	552.8
	2	891		17.0			736.0	1472.0	1070.6
Vertical / Horizontal 1/2 subsampling	4	891	8	165.9	1420	1420	143.0	286.0	208.0
	2	891		93.1			261.5	523.0	380.4
	4	891	10	138.6			172.5	345.0	251.0
	2	891		76.3			320.0	640.0	465.5
	4	891	12	119.3			202.0	404.0	293.9
	2	891		64.6			380.0	760.0	552.8
2 × 2 FD binning mode	4	891	8	165.9	1420	1420	143.0	286.0	208.0
	2	891		93.1			261.5	523.0	380.4
	4	891	10	138.6			172.5	345.0	251.0
	2	891		76.3			320.0	640.0	465.5
	4	891	12	119.3			202.0	404.0	293.9
	2	891		64.6			380.0	760.0	552.8
ROI	4	891	8	*2	*3	*3	262.0	524.0	381.1
	2	891		*2			499.0	998.0	725.9
	4	891	10	*2			321.0	642.0	467.0
	2	891		*2			617.0	1234.0	897.5
	4	891	12	*2			380.0	760.0	552.8
	2	891		*2			736.0	1472.0	1070.6

*1 The total data rate is the data rate multiplied by the number of lanes.
Example) In All-pixel 47.5 [frame/s] mode: 891 [Mbps/Lane] × 4 = 3.564 [Gbps]

*2 See the section of “ROI mode”

*3 Designated cropping area (ROI)

Data rate = 594 Mbps

Drive mode	CSI-2 Lane[*1]	Data rate [Mbps/Lane]	A/D conversion	Frame rate [frame/s]	Number of recording pixels		Number of INCK in 1 H		
					H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	4	594	8	32.1	2840	2840	389.0	778.0	565.9
	2	594		16.8			744.5	1489.0	1083.0
	4	594	10	26.2			477.5	955.0	694.6
	2	594		13.6			921.5	1843.0	1340.4
	4	594	12	22.1			566.5	1133.0	824.0
	2	594		11.4			1100.0	2200.0	1600.0
Vertical / Horizontal 1/2 subsampling	4	594	8	114.2	1420	1420	211.0	422.0	307.0
	2	594		63.2			388.5	777.0	565.1
	4	594	10	95.5			255.0	510.0	371.0
	2	594		51.6			476.5	953.0	693.1
	4	594	12	81.5			299.5	599.0	435.7
	2	594		43.4			566.0	1132.0	823.3
2 × 2 FD binning mode	4	594	8	114.2	1420	1420	211.0	422.0	307.0
	2	594		63.2			388.5	777.0	565.1
	4	594	10	95.5			255.0	510.0	371.0
	2	594		51.6			476.5	953.0	693.1
	4	594	12	81.5			299.5	599.0	435.7
	2	594		43.4			566.0	1132.0	823.3
ROI	4	594	8	*2	*3	*3	389.0	778.0	565.9
	2	594		*2			744.5	1489.0	1083.0
	4	594	10	*2			477.5	955.0	694.6
	2	594		*2			921.5	1843.0	1340.4
	4	594	12	*2			566.5	1133.0	824.0
	2	594		*2			1100.0	2200.0	1600.0

*1 The total data rate is the data rate multiplied by the number of lanes.
Example) In All-pixel 32.1 [frame/s] mode: 594 [Mbps/Lane] × 4 = 2.376 [Gbps]

*2 See the section of “ROI mode”

*3 Designated cropping area (ROI)

18.1. Restriction on Image Data Output

If the shutter releases on outputting the image data in this product, blank or Line Blanking is inserted in the imade data because of shutter stabilization wait time. Shutter stabilization wait time depends on the readout mode.
The insertion timing of shutter stabilization wait time changes depending on the shutter release timing.
During the shutter stabilization wait time, Packet Header and Packet Footer is not output.
Refer to Packet Header from the sensor and perform synchronization.

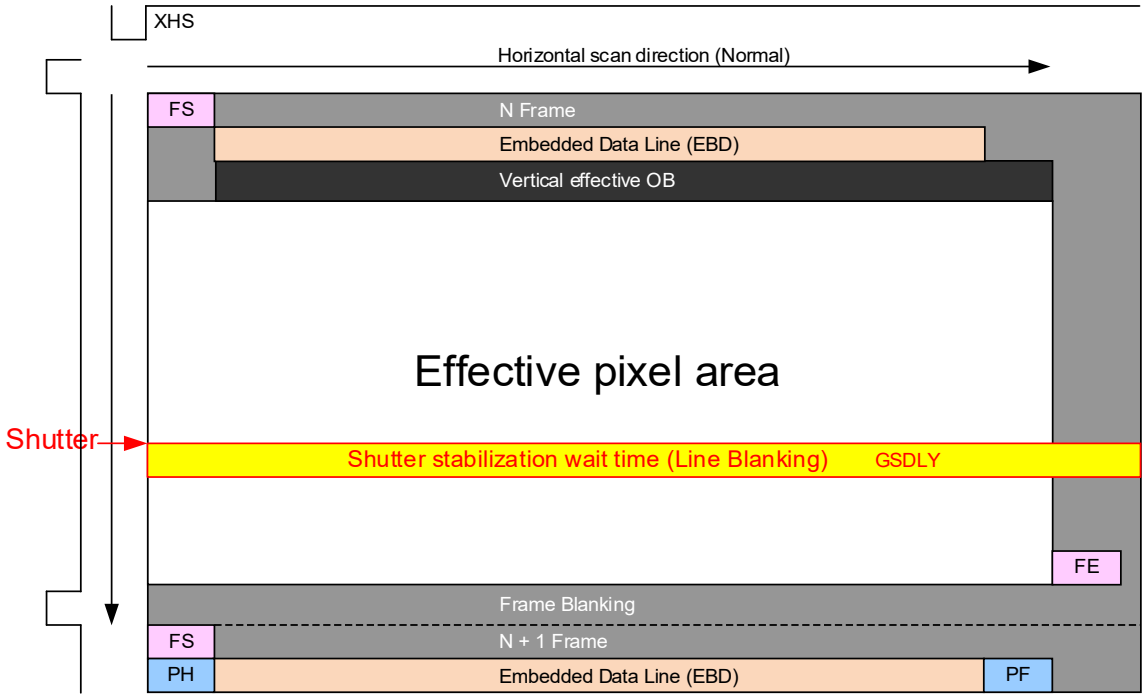


Image Drawing of Sutter stabilization wait time inserted

18.2. Image Data Output Format

18.2.1. CSI-2 Output Format

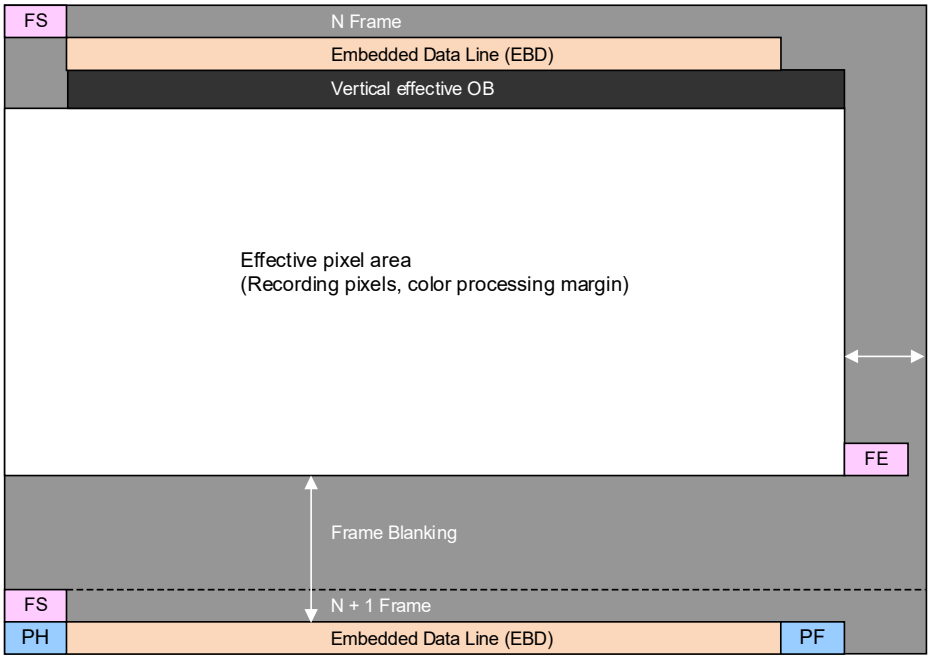
Frame Format

Each line of each image frame is output like the General Frame Format of CSI-2. The settings for each packet header are shown below.

DATA Type

Header [5:0]	Name	Register details			Description
		Chip ID	Address (I^2C)	Register Name	
00h	Frame Start Code	N/A			FS
01h	Frame End Code	N/A			FE
10h	NULL	N/A			Invalid data
12h	Embedded Data	N/A			Embedded data (1st line)
13h	Embedded Data	N/A			Embedded data (2nd to 4th lines)
2Ah	RAW8	06h	30h (3430h)	ODBIT [1:0]	0808h
2Bh	RAW10				0A0Ah
2Ch	RAW12				0C0Ch
37h	OB Data	N/A			Vertical OB line data

Frame Structure

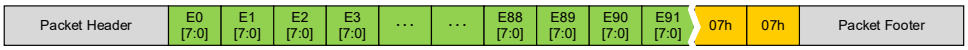


Frame Structure of CSI-2 output

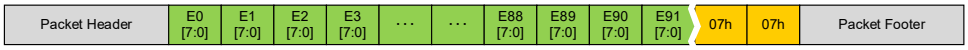
Embedded Data Line

The Embedded data line is output in a line following the FS code.

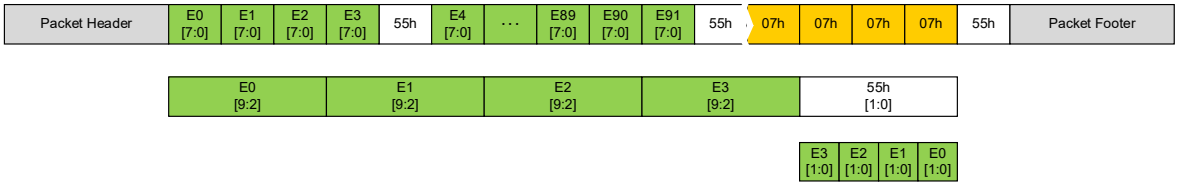
Embedded Data Format



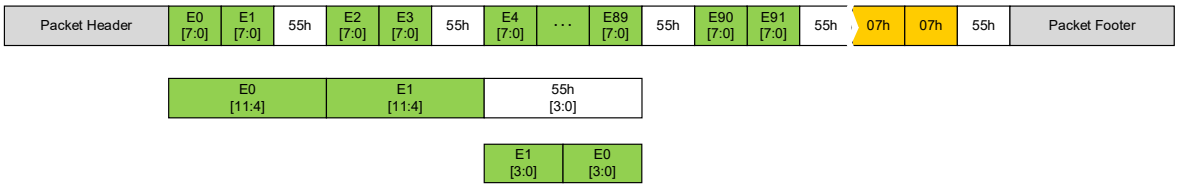
RAW8



RAW10



RAW12



Specific output examples are shown below. (Embedded data (1st line))

Pixel (8 bit)	bit	I²C address [HEX]	Data Byte Description	Description
0 to 5	[7:0]	—	—	ignored
6	[7:6]	—	—	ignored
	[5:4]	303Ch [4:3]	HVMODE [1:0]	
	[3:0]	—	—	ignored
7	[7:0]	—	—	ignored
8	[7:1]	—	—	ignored
	[0]	3100h [0]	ROI_MODE [0]	
9	[7:0]	—	—	ignored
10	[7:5]	—	—	ignored
	[4]	3204h [1]	HREVERSE [0]	
	[3:1]	—	—	ignored
	[0]	3204h [0]	VREVERSE [0]	
11	[7:0]	3242h [7:0]	SHS [23:0]	
12	[7:0]	3241h [7:0]		
13	[7:0]	3240h [7:0]		
14 to 26	[7:0]	—	—	ignored
27	[7:4]	—	—	ignored
	[3:0]	35B5h [3:0]	BLKLEVEL [11:0]	
28	[7:0]	35B4h [7:0]		
29	[7:0]	—	—	ignored
30	[7:6]	—	—	ignored
	[5:4]	3400h [4:3]	TRIGTIMING [1:0]	
	[3:1]	3400h [2:0]	TRIGMODE [2:0]	
	[0]	—	—	ignored
31 to 32	[7:0]	—	—	ignored
33	[7:1]	—	—	ignored
	[0]	3515h [0]	GAIN [8:0]	
34	[7:0]	3514h [7:0]		
35 to 46	[7:0]	—	—	ignored
47	[7:0]	30D6h [7:0]	VMAX [23:0]	
48	[7:0]	30D5h [7:0]		
49	[7:0]	30D4h [7:0]		
50	[7:0]	30D9h [7:0]	HMAX [15:0]	
51	[7:0]	30D8h [7:0]		
52 to 56	[7:0]	—	—	ignored
57	[7:0]	3104h [7:0]	FID0_ROIHxON [0] FID0_ROIVxON [0] x = 1 to 8	
58	[7:0]	3105h [7:0]		
59 to 64	[7:0]	—	—	ignored
65	[7:2]	—	—	ignored
	[1:0]	3200h [5:4]	ADBIT [1:0]	
66	[7:2]	—	—	ignored
	[1:0]	3430h [1:0]	ODBIT [1:0]	
67	[7]	—	—	ignored
	[6:4]	3904h [2:0]	LANESEL [2:0]	
	[3:0]	—	—	ignored
68 to 91	[7:0]	—	—	ignored

Output data is Data [7:0] = 07h from 92 to end pixel.

Specific output examples are shown below. (Embedded data (2nd to 4th lines))

Pixel (8 bit)	bit	I^2C address [HEX]	Data Byte Description	Description
0 to 600	[7:0]	—	—	ignored

Output data is Data [7:0] = 07h from 601 to end pixel.

18.3. Image Data Output Format on each Readout mode

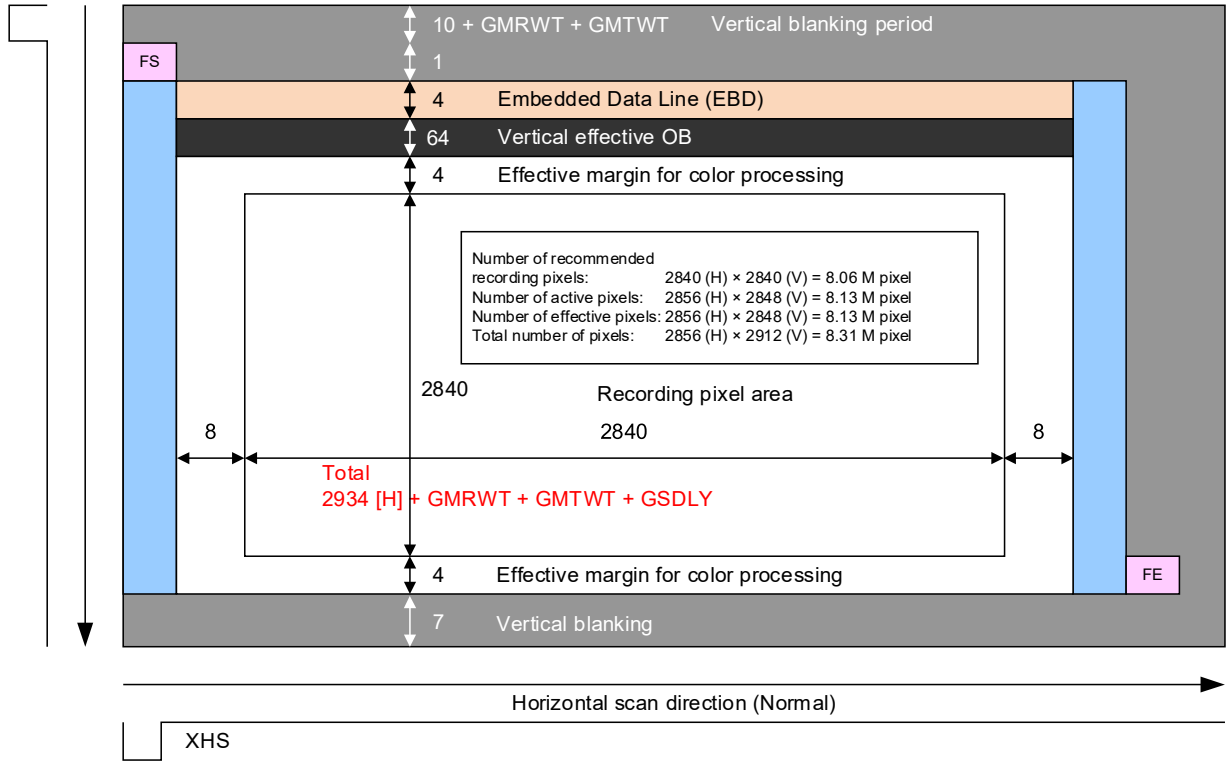
18.3.1. All-pixel scan

Register List of All-pixel scan mode

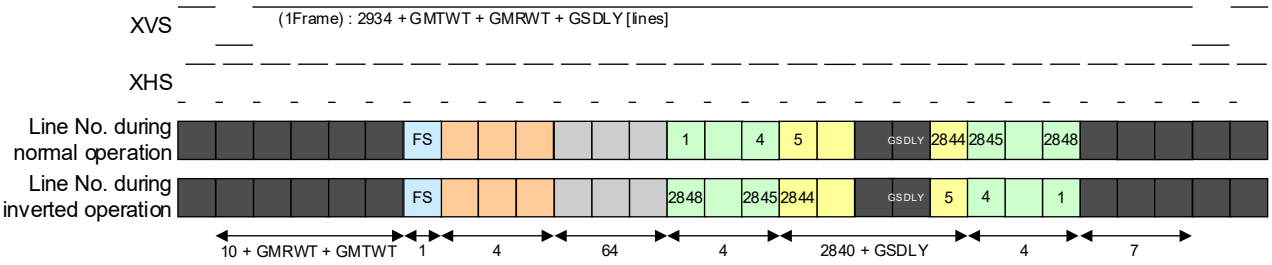
Please refer to the other register map file for the register that has not been described.

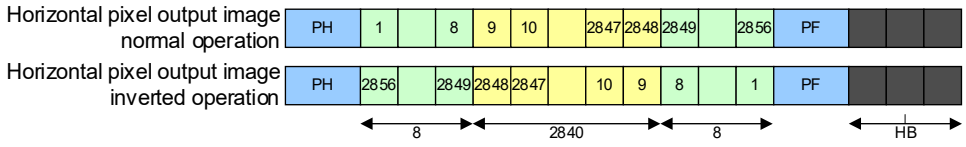
Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				4 Lane	2 Lane	4 Lane	2 Lane	4 Lane	2 Lane	
				62.6 [frame/s]	33.2 [frame/s]	51.3 [frame/s]	26.9 [frame/s]	43.4 [frame/s]	22.6 [frame/s]	1188 Mbps
				47.5 [frame/s]	25.1 [frame/s]	38.9 [frame/s]	20.3 [frame/s]	32.9 [frame/s]	17.0 [frame/s]	891 Mbps
				32.1 [frame/s]	16.8 [frame/s]	26.2 [frame/s]	13.6 [frame/s]	22.1 [frame/s]	11.4 [frame/s]	594 Mbps
Chip ID = 02h										
14h	[7:0]	INCKSEL_ST0	0Ah	INCK = 74.25 MHz: 0Ah INCK = 54 MHz: F0h INCK = 37.125 MHz: 05h						
15h	[7:0]	INCKSEL_ST1	22h	INCK = 74.25 MHz: 22h INCK = 54 MHz: D2h INCK = 37.125 MHz: 91h						
16h	[7:0]	INCKSEL_ST2	B1h	INCK = 74.25 MHz: B1h INCK = 54 MHz: 80h INCK = 37.125 MHz: 50h						
18h	[7:0]	INCKSEL_ST3	40h	INCK = 74.25 MHz: 40h INCK = 54 MHz: 18h INCK = 37.125 MHz: 20h						
19h	[7:0]	INCKSEL_ST4	04h	INCK = 74.25 MHz: 04h INCK = 54 MHz: 03h INCK = 37.125 MHz: 02h						
1Bh	[7:0]	INCKSEL_ST5	3Ah	INCK = 74.25 MHz: 3Ah INCK = 54 MHz: 2Ah INCK = 37.125 MHz: 1Dh						
3Ch	[1]		0	1						
	[4:3]	HVMODE	0h	0h						All-pixel
D0h	[7:0]	VOPB_VBLK_ HWIDTH	1020h	0B28h						
D1h	[4:0]									
D2h	[7:0]	FINFO_ HWIDTH	04B0h	0B28h						
D3h	[4:0]									
D4h	[7:0]	VMAX	000CD4h	BB0h	B98h	BA6h	B92h	BA0h	B8Ch	1188 Mbps
D5h	[7:0]			BA2h	B90h	B9Ah	B8Ah	B96h	B88h	891 Mbps
D6h	[7:0]			B96h	B88h	B92h	B84h	B8Ch	B84h	594 Mbps
D8h	[7:0]	HMAX	0081h	18Ch	2F0h	1E5h	3A2h	23Eh	455h	1188 Mbps
				20Ch	3E6h	282h	4D2h	2F8h	5C0h	891 Mbps
D9h	[7:0]			30Ah	5D1h	3BBh	733h	46Dh	898h	594 Mbps
E2h	[7:0]	GMRWT	10h	06h	04h	04h	04h	04h	02h	1188 Mbps
				04h	02h	04h	02h	04h	02h	891 Mbps
				04h	02h	04h	02h	02h	02h	594 Mbps
E3h	[7:0]	GMTWT	70h	24h	14h	1Eh	10h	1Ah	0Eh	1188 Mbps
				1Ch	10h	16h	0Ch	14h	0Ah	891 Mbps
				14h	0Ah	10h	08h	0Eh	08h	594 Mbps
E5h	[7:0]	GAINDLY	04h	02h						
E6h	[7:0]	GSDLY	30h	10h	0Ah	0Eh	08h	0Ch	06h	1188 Mbps
				0Ch	08h	0Ah	06h	08h	06h	891 Mbps
				08h	06h	08h	04h	06h	04h	594 Mbps
Chip ID = 04h										
00h	[5:4]	ADBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
1Ch	[7:0]	INCKSEL_N0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h						
1Dh	[7:0]	INCKSEL_N1	05h	05h						

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				4 Lane	2 Lane	4 Lane	2 Lane	4 Lane	2 Lane	
				62.6 [frame/s]	33.2 [frame/s]	51.3 [frame/s]	26.9 [frame/s]	43.4 [frame/s]	22.6 [frame/s]	1188 Mbps
				47.5 [frame/s]	25.1 [frame/s]	38.9 [frame/s]	20.3 [frame/s]	32.9 [frame/s]	17.0 [frame/s]	891 Mbps
				32.1 [frame/s]	16.8 [frame/s]	26.2 [frame/s]	13.6 [frame/s]	22.1 [frame/s]	11.4 [frame/s]	594 Mbps
1Eh	[7:0]	INCKSEL_N2	E0h	INCK = 74.25 MHz: E0h INCK = 54 MHz: 34h INCK = 37.125 MHz: E0h						
1Fh	[7:0]	INCKSEL_N3	00h	INCK = 74.25 MHz: 00h INCK = 54 MHz: 01h INCK = 37.125 MHz: 00h						
20h	[7:0]	INCKSEL_S0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h						
21h	[7:0]	INCKSEL_S1	05h	05h						
22h	[7:0]	INCKSEL_S2	E0h	INCK = 74.25 MHz: E0h INCK = 54 MHz: 34h INCK = 37.125 MHz: E0h						
23h	[7:0]	INCKSEL_S3	00h	INCK = 74.25 MHz: 00h INCK = 54 MHz: 01h INCK = 37.125 MHz: 00h						
24h	[7:0]	INCKSEL_D0	10h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h						
25h	[7:0]	INCKSEL_D1	14h	14h						
26h	[7:0]	INCKSEL_D2	20h	INCK = 74.25 MHz: 80h INCK = 54 MHz: B0h INCK = 37.125 MHz: 80h						1188 Mbps / 594 Mbps
				INCK = 74.25 MHz: C0h INCK = 54 MHz: 08h INCK = 37.125 MHz:C0h						891 Mbps
27h	[7:0]	INCKSEL_D3	C0h	80h						1188 Mbps
				INCK = 74.25 MHz: D0h INCK = 54 MHz: D1h INCK = 37.125 MHz: D0h						891 Mbps
				90h						594 Mbps
3Ch 3Dh	[7:1] [0]	LLBLANK	18h	0Ch						
3Eh	[7:2]		16h	0Ch						
Chip ID = 06h										
30h	[1:0]	ODBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
Chip ID = 07h										
21h	[7:0]		A9h	7Dh						
46h	[7:0]		2Ah	1Fh						
B4h B5h	[7:0] [3:0]	BLKLEVEL	03Ch	00Fh		03Ch		0F0h		Recommended value
Chip ID = 0Bh										
04h	[2:0]	LANESEL	0h	2h	N/A	2h	N/A	2h	N/A	4 Lane CSI-2
				N/A	3h	N/A	3h	N/A	3h	2 Lane CSI-2
Chip ID = 0Eh										
A4h A5h	[7:0] [7:0]	TXCLKESC_ FREQ	12C0h	INCK = 74.25 MHz: 12C0h INCK = 54 MHz: 0D80h INCK = 37.125 MHz: 0980h						
B4h to C7h	[7:0] [7:0]	Global Timing registers	–	Refer to Global Timing Register Setting						



Pixel Array Image Drawing in All-pixel scan Mode
(CSI-2 output Shutter stabilization wait time is not included)





* It outputs in the format of RAW8, RAW10 or RAW12.

: FS/FE
: Embedded data line
: Effective OB
: Blanking
: Packet Header / Packet Footer
: Color processing margin
: Recording pixel area
HB : Horizontal blanking

Drive Timing Chart for Serial Output in All-pixel Scan Mode (CSI-2 output)

18.3.2. ROI mode

This Sensor has ROI function that signals are cut out and read out in multi arbitrary positions.
Cropping position can set maximum 64 areas that specified by horizontal 8 points and vertical 8 points, regarding effective pixel start position as origin (0, 0) in all pixel scan mode. Cropping is available from All-pixel scan mode and horizontal period are fixed to the value for this mode.
These cropped areas by horizontal cropping setting (ROI (1, y) to ROI (8, y)) are output with left justified and that extends the horizontal blanking period. In vertical cropping area (ROI (x, 1) to ROI (x, 8)), the number of image data is also output from cropping start line and the frame rate can be adjusted by changing the number of input XVS lines in slave mode or changing register VMAX in master mode.
One invalid frame is generated when the ROI area changing size or cropping address.
ROI image is shown in the figure below.
In case of Vertical / Horizontal 1/2 subsampling mode, this sensor doesn't support ROI mode.
This sensor supports ROI + 2 × 2 FD binning mode.
The horizontal output width of Embedded data line be set by FINFO_HWIDTH register.
The horizontal output width of Vertical OB and Vertical blanking can be set by VOPB_VBLK_HWIDTH register.
The output position of the packet footer can be changed by EAV_SEL_MIPI register.
This section is written in case of all-pixel scan mode for example on this document.

Register List of the packet footer output position setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
EAV_SEL_MIPI [0]	0Bh	42h (3942h)	[1]	0	0: CSI-2 v1.2 compliant 1: Immediately after the effective pixel output

Before ROI processing

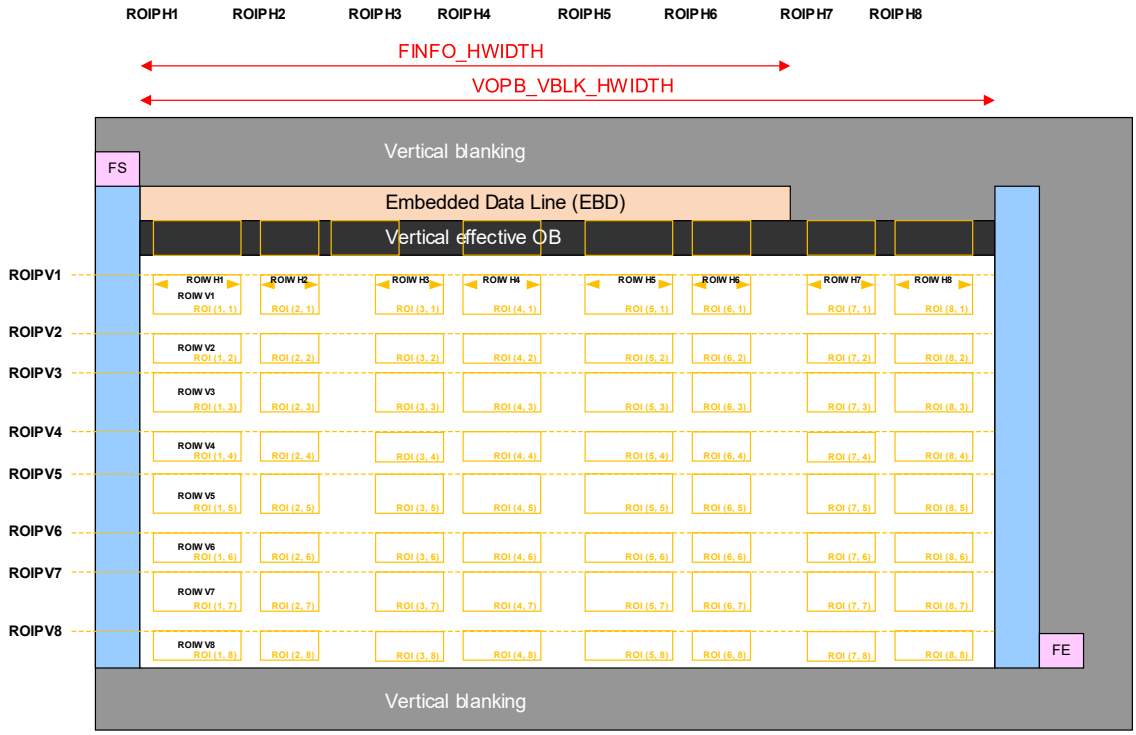
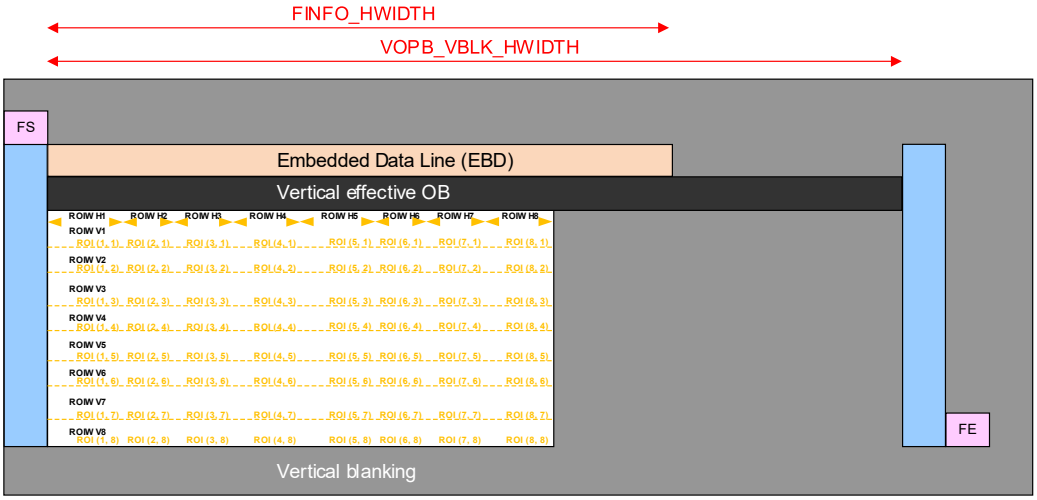


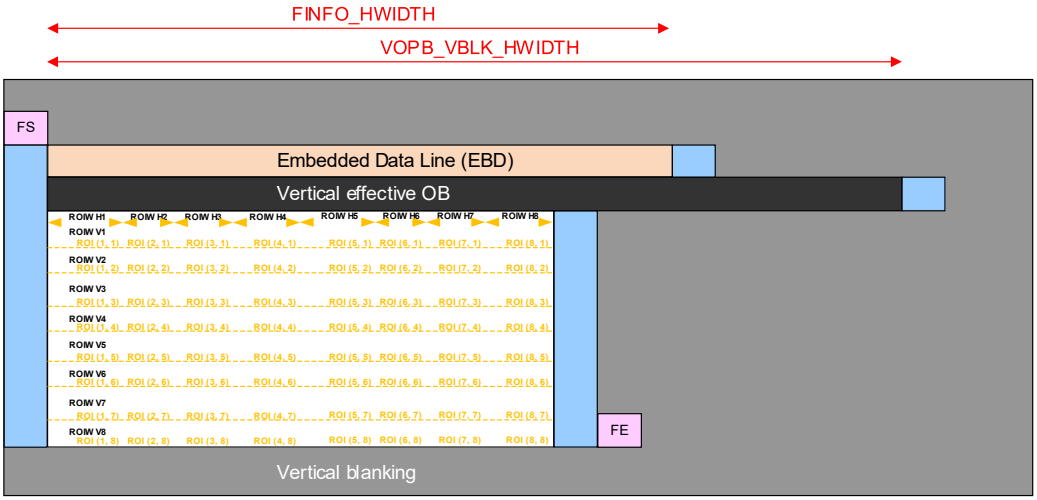
Image Drawing of Designated Areas in ROI Mode

After ROI processing (EAV_SEL_MIPI = 0)　* CSI-2 v1.2 compliant



Details of Image Drawing (EAV_SEL_MIPI = 0)

After ROI processing (EAV_SEL_MIPI = 1)



Details of Image Drawing (EAV_SEL_MIPI = 1)

Register List of ROI mode

Please set All-pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				4 Lane	2 Lane	4 Lane	2 Lane	4 Lane	2 Lane	
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
Chip ID = 02h										
14h	[7:0]	INCKSEL_ST0	0Ah	INCK = 74.25 MHz: 0Ah INCK = 54 MHz: F0h INCK = 37.125 MHz: 05h						
15h	[7:0]	INCKSEL_ST1	22h	INCK = 74.25 MHz: 22h INCK = 54 MHz: D2h INCK = 37.125 MHz: 91h						
16h	[7:0]	INCKSEL_ST2	B1h	INCK = 74.25 MHz: B1h INCK = 54 MHz: 80h INCK = 37.125 MHz: 50h						
18h	[7:0]	INCKSEL_ST3	40h	INCK = 74.25 MHz: 40h INCK = 54 MHz: 18h INCK = 37.125 MHz: 20h						
19h	[7:0]	INCKSEL_ST4	04h	INCK = 74.25 MHz: 04h INCK = 54 MHz: 03h INCK = 37.125 MHz: 02h						
1Bh	[7:0]	INCKSEL_ST5	3Ah	INCK = 74.25 MHz: 3Ah INCK = 54 MHz: 2Ah INCK = 37.125 MHz: 1Dh						
3Ch	[1]		0	1						
	[4:3]	HVMODE	0h	0h						All-pixel
D0h	[7:0]	VOPB_VBLK_ HWIDTH	1020h	VOPB effective area and V Blank width setting *Set the value of multiple of 8						
D1h	[4:0]									
D2h	[7:0]	FINFO_ HWIDTH	04B0h	EBD width setting *Set the value of multiple of 16						
D3h	[4:0]									
D4h	[7:0]	VMAX	000CD4h	*1	*2	*3	*4	*5	*6	
D5h	[7:0]									
D6h	[7:0]									
D8h	[7:0]	HMAX	0081h	18Ch	2F0h	1E5h	3A2h	23Eh	455h	1188 Mbps
				20Ch	3E6h	282h	4D2h	2F8h	5C0h	891 Mbps
D9h	[7:0]			30Ah	5D1h	3BBh	733h	46Dh	898h	594 Mbps
E2h	[7:0]	GMRWT	10h	06h	04h	04h	04h	04h	02h	1188 Mbps
				04h	02h	04h	02h	04h	02h	891 Mbps
				04h	02h	04h	02h	02h	02h	594 Mbps
E3h	[7:0]	GMTWT	70h	24h	14h	1Eh	10h	1Ah	0Eh	1188 Mbps
				1Ch	10h	16h	0Ch	14h	0Ah	891 Mbps
				14h	0Ah	10h	08h	0Eh	08h	594 Mbps
E5h	[7:0]	GAINDLY	04h	02h						
E6h	[7:0]	GSDLY	30h	10h	0Ah	0Eh	08h	0Ch	06h	1188 Mbps
				0Ch	08h	0Ah	06h	08h	06h	891 Mbps
				08h	06h	08h	04h	06h	04h	594 Mbps

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				4 Lane	2 Lane	4 Lane	2 Lane	4 Lane	2 Lane	
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
Chip ID = 03h										
04h	[0]	FID0_ROIH1ON	0	The horizontal setting of FID0 ROI area (1, y) (y = 1 to 8) 0: Disable 1: Enable						
	[1]	FID0_ROIV1ON	0	The vertical setting of FID0 ROI area (x, 1) (x = 1 to 8) 0: Disable 1: Enable						
	[2]	FID0_ROIH2ON	0	The horizontal setting of FID0 ROI area (2, y) (y = 1 to 8) 0: Disable 1: Enable						
	[3]	FID0_ROIV2ON	0	The vertical setting of FID0 ROI area (x, 2) (x = 1 to 8) 0: Disable 1: Enable						
	[4]	FID0_ROIH3ON	0	The horizontal setting of FID0 ROI area (3, y) (y = 1 to 8) 0: Disable 1: Enable						
	[5]	FID0_ROIV3ON	0	The vertical setting of FID0 ROI area (x, 3) (x = 1 to 8) 0: Disable 1: Enable						
	[6]	FID0_ROIH4ON	0	The horizontal setting of FID0 ROI area (4, y) (y = 1 to 8) 0: Disable 1: Enable						
	[7]	FID0_ROIV4ON	0	The vertical setting of FID0 ROI area (x, 4) (x = 1 to 8) 0: Disable 1: Enable						
05h	[0]	FID0_ROIH5ON	0	The horizontal setting of FID0 ROI area (5, y) (y = 1 to 8) 0: Disable 1: Enable						
	[1]	FID0_ROIV5ON	0	The vertical setting of FID0 ROI area (x, 5) (x = 1 to 8) 0: Disable 1: Enable						
	[2]	FID0_ROIH6ON	0	The horizontal setting of FID0 ROI area (6, y) (y = 1 to 8) 0: Disable 1: Enable						
	[3]	FID0_ROIV6ON	0	The vertical setting of FID0 ROI area (x, 6) (x = 1 to 8) 0: Disable 1: Enable						
	[4]	FID0_ROIH7ON	0	The horizontal setting of FID0 ROI area (7, y) (y = 1 to 8) 0: Disable 1: Enable						
	[5]	FID0_ROIV7ON	0	The vertical setting of FID0 ROI area (x, 7) (x = 1 to 8) 0: Disable 1: Enable						
	[6]	FID0_ROIH8ON	0	The horizontal setting of FID0 ROI area (8, y) (y = 1 to 8) 0: Disable 1: Enable						
	[7]	FID0_ROIV8ON	0	The vertical setting of FID0 ROI area (x, 8) (x = 1 to 8) 0: Disable 1: Enable						
20h	[7:0]	FID0_ROIPH1	0000h	Designation of horizontal cropping position for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 8						
21h	[4:0]									
22h	[7:0]	FID0_ROIPV1	0000h	Designation of vertical cropping position for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8						
23h	[4:0]									
24h	[7:0]	FID0_ROIWH1	0000h	Designation of horizontal cropping size for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 8						
25h	[4:0]									
26h	[7:0]	FID0_ROIWV1	0000h	Designation of vertical cropping size for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8						
27h	[4:0]									
28h	[7:0]	FID0_ROIPH2	0000h	Designation of horizontal cropping position for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 8						
29h	[4:0]									
2Ah	[7:0]	FID0_ROIPV2	0000h	Designation of vertical cropping position for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8						
2Bh	[4:0]									
2Ch	[7:0]	FID0_ROIWH2	0000h	Designation of horizontal cropping size for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 8						
2Dh	[4:0]									
2Eh	[7:0]	FID0_ROIWV2	0000h	Designation of vertical cropping size for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8						
2Fh	[4:0]									
30h	[7:0]	FID0_ROIPH3	0000h	Designation of horizontal cropping position for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 8						
31h	[4:0]									
32h	[7:0]	FID0_ROIPV3	0000h	Designation of vertical cropping position for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8						
33h	[4:0]									
34h	[7:0]	FID0_ROIWH3	0000h	Designation of horizontal cropping size for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 8						
35h	[4:0]									
36h	[7:0]	FID0_ROIWV3	0000h	Designation of vertical cropping size for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8						
37h	[4:0]									

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				4 Lane	2 Lane	4 Lane	2 Lane	4 Lane	2 Lane	
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
38h	[7:0]	FID0_ROIPH4	0000h	Designation of horizontal cropping position for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 8						
39h	[4:0]									
3Ah	[7:0]	FID0_ROIPV4	0000h	Designation of vertical cropping position for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8						
3Bh	[4:0]									
3Ch	[7:0]	FID0_ROIWH4	0000h	Designation of horizontal cropping size for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 8						
3Dh	[4:0]									
3Eh	[7:0]	FID0_ROIWV4	0000h	Designation of vertical cropping size for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8						
3Fh	[4:0]									
40h	[7:0]	FID0_ROIPH5	0000h	Designation of horizontal cropping position for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 8						
41h	[4:0]									
42h	[7:0]	FID0_ROIPV5	0000h	Designation of vertical cropping position for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8						
43h	[4:0]									
44h	[7:0]	FID0_ROIWH5	0000h	Designation of horizontal cropping size for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 8						
45h	[4:0]									
46h	[7:0]	FID0_ROIWV5	0000h	Designation of vertical cropping size for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8						
47h	[4:0]									
48h	[7:0]	FID0_ROIPH6	0000h	Designation of horizontal cropping position for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 8						
49h	[4:0]									
4Ah	[7:0]	FID0_ROIPV6	0000h	Designation of vertical cropping position for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8						
4Bh	[4:0]									
4Ch	[7:0]	FID0_ROIWH6	0000h	Designation of horizontal cropping size for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 8						
4Dh	[4:0]									
4Eh	[7:0]	FID0_ROIWV6	0000h	Designation of vertical cropping size for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8						
4Fh	[4:0]									
50h	[7:0]	FID0_ROIPH7	0000h	Designation of horizontal cropping position for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 8						
51h	[4:0]									
52h	[7:0]	FID0_ROIPV7	0000h	Designation of vertical cropping position for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8						
53h	[4:0]									
54h	[7:0]	FID0_ROIWH7	0000h	Designation of horizontal cropping size for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 8						
55h	[4:0]									
56h	[7:0]	FID0_ROIWV7	0000h	Designation of vertical cropping size for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8						
57h	[4:0]									
58h	[7:0]	FID0_ROIPH8	0000h	Designation of horizontal cropping position for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 8						
59h	[4:0]									
5Ah	[7:0]	FID0_ROIPV8	0000h	Designation of vertical cropping position for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8						
5Bh	[4:0]									
5Ch	[7:0]	FID0_ROIWH8	0000h	Designation of horizontal cropping size for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 8						
5Dh	[4:0]									
5Eh	[7:0]	FID0_ROIWV8	0000h	Designation of vertical cropping size for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8						
5Fh	[4:0]									
Chip ID = 04h										
00h	[5:4]	ADBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
1Ch	[7:0]	INCKSEL_N0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h						
1Dh	[7:0]	INCKSEL_N1	05h	05h						
1Eh	[7:0]	INCKSEL_N2	E0h	INCK = 74.25 MHz: E0h INCK = 54 MHz: 34h INCK = 37.125 MHz: E0h						
1Fh	[7:0]	INCKSEL_N3	00h	INCK = 74.25 MHz: 00h INCK = 54 MHz: 01h INCK = 37.125 MHz: 00h						

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				4 Lane	2 Lane	4 Lane	2 Lane	4 Lane	2 Lane	
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
20h	[7:0]	INCKSEL_S0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h						
21h	[7:0]	INCKSEL_S1	05h	05h						
22h	[7:0]	INCKSEL_S2	E0h	INCK = 74.25 MHz: E0h INCK = 54 MHz: 34h INCK = 37.125 MHz: E0h						
23h	[7:0]	INCKSEL_S3	00h	INCK = 74.25 MHz: 00h INCK = 54 MHz: 01h INCK = 37.125 MHz: 00h						
24h	[7:0]	INCKSEL_D0	10h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h						
25h	[7:0]	INCKSEL_D1	14h	14h						
26h	[7:0]	INCKSEL_D2	20h	INCK = 74.25 MHz: 80h INCK = 54 MHz: B0h INCK = 37.125 MHz: 80h						1188 Mbps / 594 Mbps
				INCK = 74.25 MHz: C0h INCK = 54 MHz: 08h INCK = 37.125 MHz:C0h						891 Mbps
27h	[7:0]	INCKSEL_D3	C0h	80h						1188 Mbps
				INCK = 74.25 MHz: D0h INCK = 54 MHz: D1h INCK = 37.125 MHz: D0h						891 Mbps
				90h						594 Mbps
3Ch	[7:1]	LLBLANK	18h	0Ch						
3Dh	[0]									
3Eh	[7:2]		16h	0Ch						
Chip ID = 06h										
30h	[1:0]	ODBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
Chip ID = 07h										
21h	[7:0]		A9h	7Dh						
46h	[7:0]		2Ah	1Fh						
B4h	[7:0]	BLKLEVEL	03Ch	00Fh		03Ch		0F0h		Recommended value
B5h	[3:0]									
Chip ID = 0Bh										
04h	[2:0]	LANESEL	0h	2h	N/A	2h	N/A	2h	N/A	4 Lane CSI-2
				N/A	3h	N/A	3h	N/A	3h	2 Lane CSI-2
42h	[1]	EAV_SEL_MIPI	0	0: CSI-2 v1.2 compliant 1: Immediately after the effective pixel output						
Chip ID = 0Eh										
A4h	[7:0]	TXCLKESC_ FREQ	12C0h	INCK = 74.25 MHz: 12C0h INCK = 54 MHz: 0D80h INCK = 37.125 MHz: 0980h						
A5h	[7:0]									
B4h	[7:0]	Global Timing Registers	–	Refer to Global Timing Register Setting						
to										
C7h	[7:0]									

Restrictions on ROI mode

The register settings should satisfy following conditions:

* Do not designate area like be overlap.
ROIPH1 + ROIWH1 ≤ ROIPH2
ROIPH2 + ROIWH2 ≤ ROIPH3
ROIPH3 + ROIWH3 ≤ ROIPH4
…
ROIPH8 + ROIWH8 ≤ 2856d

ROIPV1 + ROIWV1 ≤ ROIPV2
ROIPV2 + ROIWV2 ≤ ROIPV3
ROIPV3 + ROIWV3 ≤ ROIPV4
…
ROIPV8 + ROIWV8 ≤ 2848d

* Set the ROIPHx and ROIWHx (x = 1 to 8) registers in multiple of 8.
* Set the ROIPVx and ROIWVx (x = 1 to 8) registers in multiple of 8.
* Set the VOPB_VBLK_HWIDTH register in multiple of 8.
* Set the FINFO_HWIDTH register in multiple of 16.

* The range of horizontal output width is as below.
10 / 12 bit mode
608d ≤ ROIWH1 + ROIWH2 + ROIWH3 + …. + ROIWH8 ≤ 2856d

8 bit mode
1200d ≤ ROIWH1 + ROIWH2 + ROIWH3 + …. + ROIWH8 ≤ 2856d

* The range of vertical output width is as below.
8 / 10 / 12 bit mode
8d ≤ ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 ≤ 2848d

* The range of output width for Vertical OB and Vertical blanking is as below.
1188 Mbps/Lane
344d ≤ VOPB_VBLK_HWIDTH ≤ 2856d
891 Mbps/Lane
392d ≤ VOPB_VBLK_HWIDTH ≤ 2856d
594 Mbps/Lane
472d ≤ VOPB_VBLK_HWIDTH ≤ 2856d

* The range of output width for Embedded data line is as below.
10 / 12 bit mode
608d ≤ FINFO_HWIDTH ≤ 2856d

8 bit mode
1200d ≤ FINFO_HWIDTH ≤ 2856d

Frame rate on ROI mode

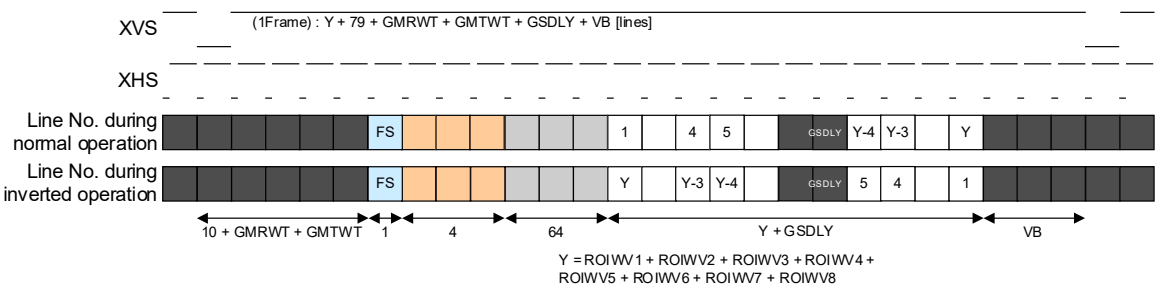
Frame rate [frame/s] = 1 / ((“Number of lines per frame” or VMAX) × (1 H period))

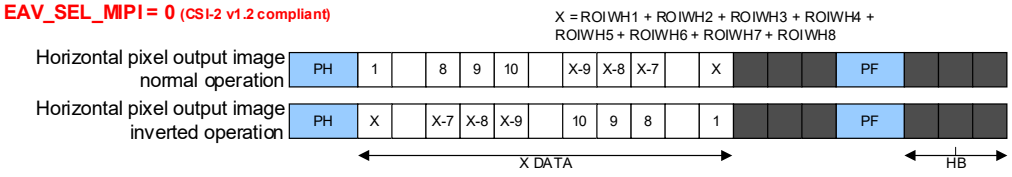
* Number of lines per frame or VMAX
V_{TR} = ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 + GMRWT + GMTWT + GSDLY + 86
For GMRWT, GMTWT and GSDLY, refer to the register list of each readout mode.
* 1H period: Change according to the data rate settings and the number of CSI-2 Lanes.
Calculate by number of INCK in 1 H and the period of INCK.

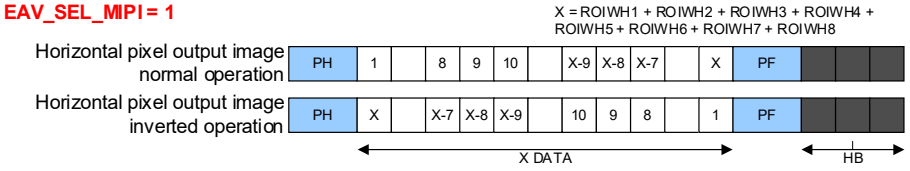
The example of ROI setting is shown below.
ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 = 640
ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 = 8 (minimum value)

Frame rate List of each setting

Register settings No. in register list	1 H period [µs]			Frame rate [frame/s]					
				Total number of ROI: 640 [line]			Total number of ROI: 8 [line]		
	Data rate 1188 Mbps	Data rate 891 Mbps	Data rate 594 Mbps	1188 Mbps	891 Mbps	594 Mbps	1188 Mbps	891 Mbps	594 Mbps
*1	5.34	7.06	10.48	239.15	184.02	125.90	1233.55	1026.80	757.43
*2	10.13	13.45	20.06	129.91	98.93	67.02	771.38	619.98	445.22
*3	6.54	8.65	12.87	197.79	151.77	103.11	1078.11	889.64	637.28
*4	12.53	16.62	24.83	105.88	80.65	54.44	654.41	527.80	373.03
*5	7.74	10.24	15.26	168.43	128.88	87.61	951.14	775.37	564.94
*6	14.94	19.83	29.63	89.50	67.79	45.60	577.17	450.37	312.50







* It outputs in the format of RAW8, RAW10 or RAW12.

: FS/FE
: Embedded data line
: Effective OB
: Blanking
: Packet Header / Packet Footer
: ROI pixel area
HB : Horizontal blanking

Drive Timing Chart for Serial Output in ROI Mode (CSI-2 output)

18.3.3. Overlap ROI mode

This Sensor has ROI function that signals are cut out and read out in multi arbitrary positions.
Cropping position can set maximum 8 areas, regarding effective pixel start position as origin (0, 0) in all pixel scan mode. Cropping is available from All-pixel scan mode and horizontal period are fixed to the value for this mode.
These cropped areas by horizontal cropping setting (ROI (1, y) to ROI (8, y)) are output with left justified and that extends the horizontal blanking period. In vertical cropping area (ROI (x, 1) to ROI (x, 8)), the number of image data is also output from cropping start line and the frame rate can be adjusted by changing the number of input XVS lines in slave mode or changing register VMAX in master mode.
One invalid frame is generated when the ROI area changing size or cropping address.
ROI image is shown in the figure below.
In case of Vertical / Horizontal 1/2 subsampling mode, this sensor doesn't support ROI mode.
This sensor support ROI + 2 × 2 FD binning mode.
The horizontal output width of Embedded data line be set by FINFO_HWIDTH register.
The horizontal output width of Vertical OB and Vertical blanking can be set by VOPB_VBLK_HWIDTH register.
The output position of the packet footer can be changed by EAV_SEL_MIPI register.
This section is written in case of all-pixel scan mode for example on this document.

Register List of the packet footer output position setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I^2C	bit		
EAV_SEL_MIPI [0]	0Bh	42h (3942h)	[1]	0	0: CSI-2 v1.2 compliant 1: Immediately after the effective pixel output

Before Overlap ROI processing

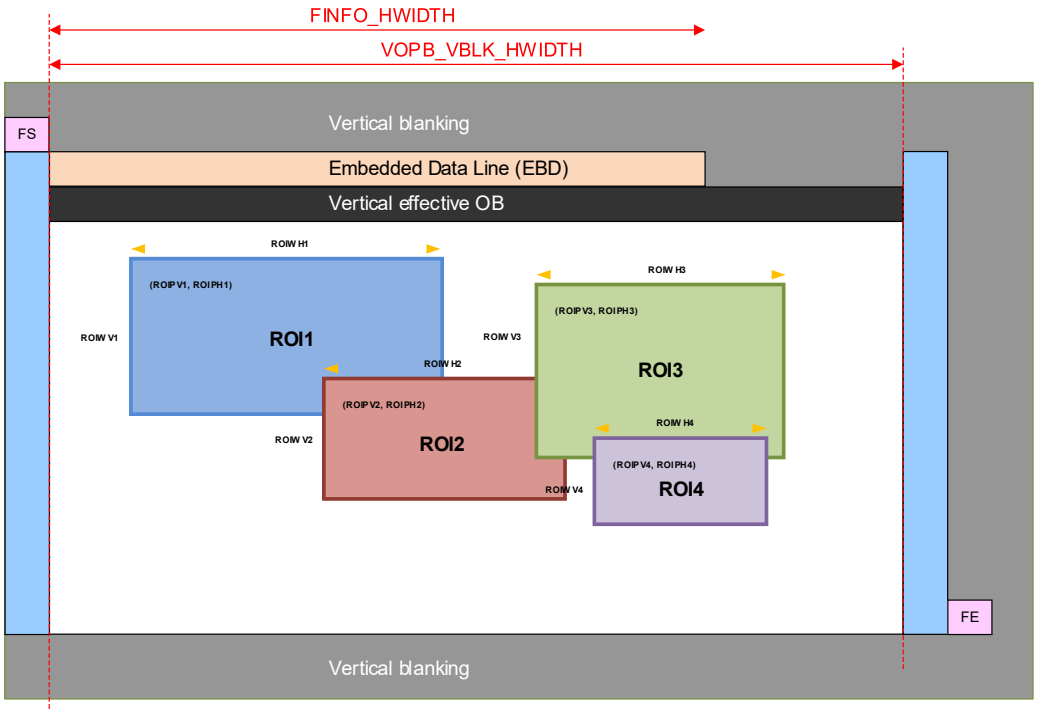
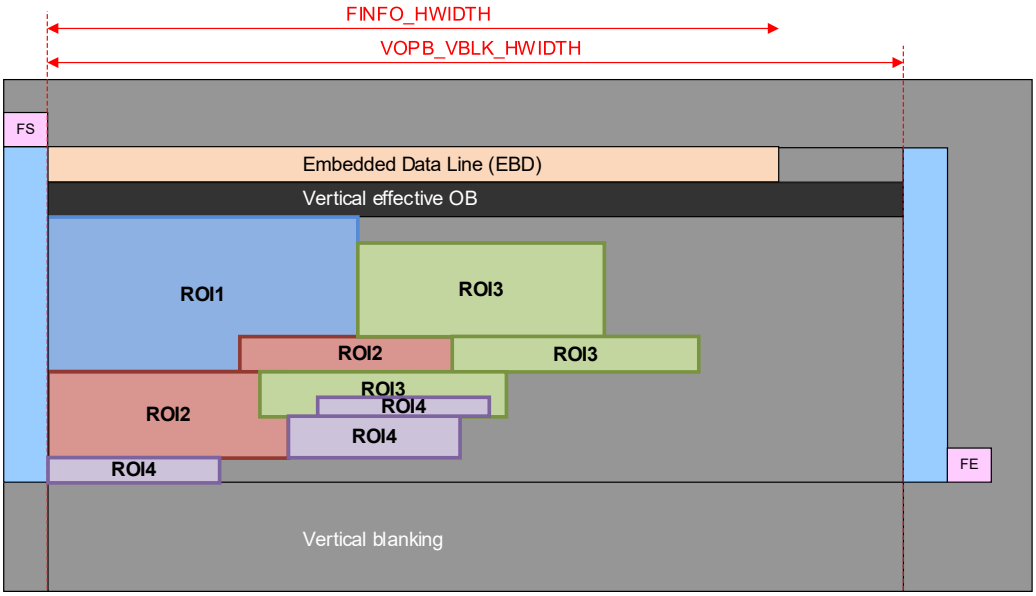


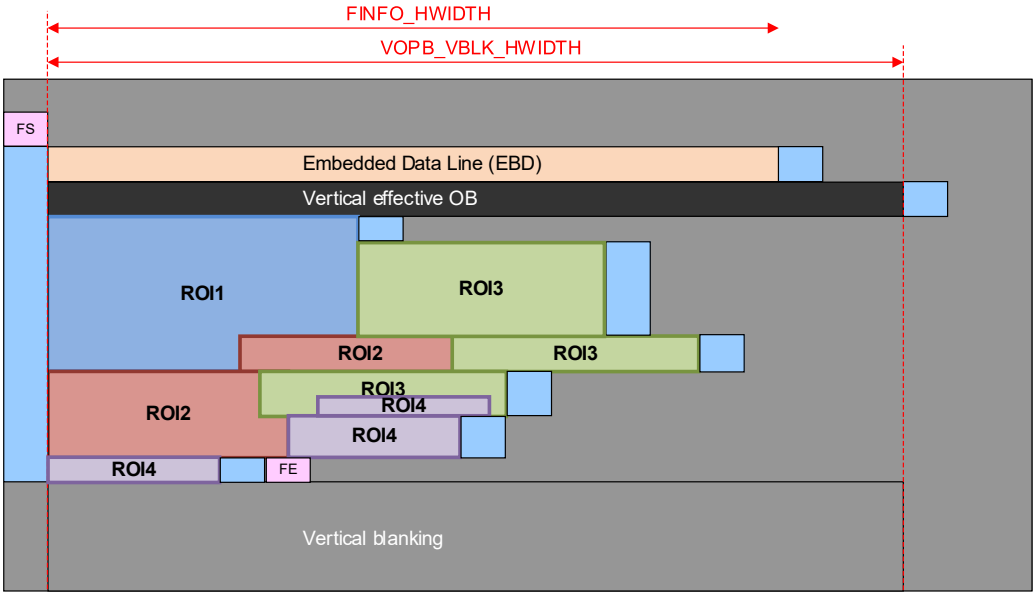
Image Drawing of Designated Areas in Overlap ROI Mode (CSI-2 output)

After Overlap ROI processing (EAV_SEL_MIPI = 0)　* CSI-2 v1.2 compliant



Details of Image Drawing (EAV_SEL_MIPI = 0)

After Overlap ROI processing (EAV_SEL_MIPI = 1)



Details of Image Drawing (EAV_SEL_MIPI = 1)

Register List of Overlap ROI mode

Please set ROI mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				4 Lane	2 Lane	4 Lane	2 Lane	4 Lane	2 Lane	
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
Chip ID = 02h										
D0h	[7:0]	VOPB_VBLK_ HWIDTH	1020h	VOPB effective area and V Blank width setting *Set the value of multiple of 8						
D1h	[4:0]									
D2h	[7:0]	FINFO_HWIDTH	04B0h	EBD width setting *Set the value of multiple of 16						
D3h	[4:0]									
Chip ID = 03h										
00h	[0]	ROI_MODE	0	1						
Chip ID = 0Bh										
42h	[1]	EAV_SEL_MIPI	0	0: CSI-2 v1.2 compliant 1: Immediately after the effective pixel output						

Restrictions on Overlap ROI mode

The register settings should satisfy following conditions:

ROIPH1 + ROIWH1 ≤ 2856d
ROIPH2 + ROIWH2 ≤ 2856d
ROIPH3 + ROIWH3 ≤ 2856d
…
ROIPH8 + ROIWH8 ≤ 2856d

ROIPV1 + ROIWV1 ≤ 2848d
ROIPV2 + ROIWV2 ≤ 2848d
ROIPV3 + ROIWV3 ≤ 2848d
…
ROIPV8 + ROIWV8 ≤ 2848d

* Set the ROIPHx and ROIWHx (x = 1 to 8) registers in multiple of 8.
* Set the ROIPVx and ROIWVx (x = 1 to 8) registers in multiple of 8.
* Set the VOPB_VBLK_HWIDTH register in multiple of 8.
* Set the FINFO_HWIDTH register in multiple of 16.

* The range of horizontal output width is as below.
 10 / 12 bit mode
  ROIWH1 ≥ 8d, ROIWH2 ≥ 8d, ROIWH3 ≥ 8d, …. ROIWH8 ≥ 8d
  “Minimum horizontal output width after ROI operation” ≥ 608d
  “Maximum horizontal output width after ROI operation” ≤ 2856d

 8 bit mode
  ROIWH1 ≥ 8d, ROIWH2 ≥ 8d, ROIWH3 ≥ 8d, …. ROIWH8 ≥ 8d
  “Minimum horizontal output width after ROI operation” ≥ 1200d
  “Maximum horizontal output width after ROI operation” ≤ 2856d

* The range of vertical output width is as below.
 8 / 10 / 12 bit mode
  ROIWV1 ≥ 8d, ROIWV2 ≥ 8d, ROIWV3 ≥ 8d, … ROIWV8 ≥ 8d
  “Minimum vertical output width after ROI operation” ≥ 8d
  “Maximum vertical output width after ROI operation” ≤ 2848d

* The range of output width for Vertical OB and Vertical blanking is as below.
 1188 Mbps/Lane
  344d ≤ VOPB_VBLK_HWIDTH ≤ 2856d
 891 Mbps/Lane
  392d ≤ VOPB_VBLK_HWIDTH ≤ 2856d
 594 Mbps/Lane
  472d ≤ VOPB_VBLK_HWIDTH ≤ 2856d

* The range of output width for Embedded data line is as below.
 10 / 12 bit mode
  608d ≤ FINFO_HWIDTH ≤ 2856d

 8 bit mode
  1200d ≤ FINFO_HWIDTH ≤ 2856d

Frame rate on Overlap ROI mode

Frame rate [frame/s] = 1 / ((“Number of lines per frame” or VMAX) × (1 H period))
When the vertical output width is 640 or 8 lines, refer to ROI mode.

18.3.4. Vertical / Horizontal 1/2 Subsampling mode

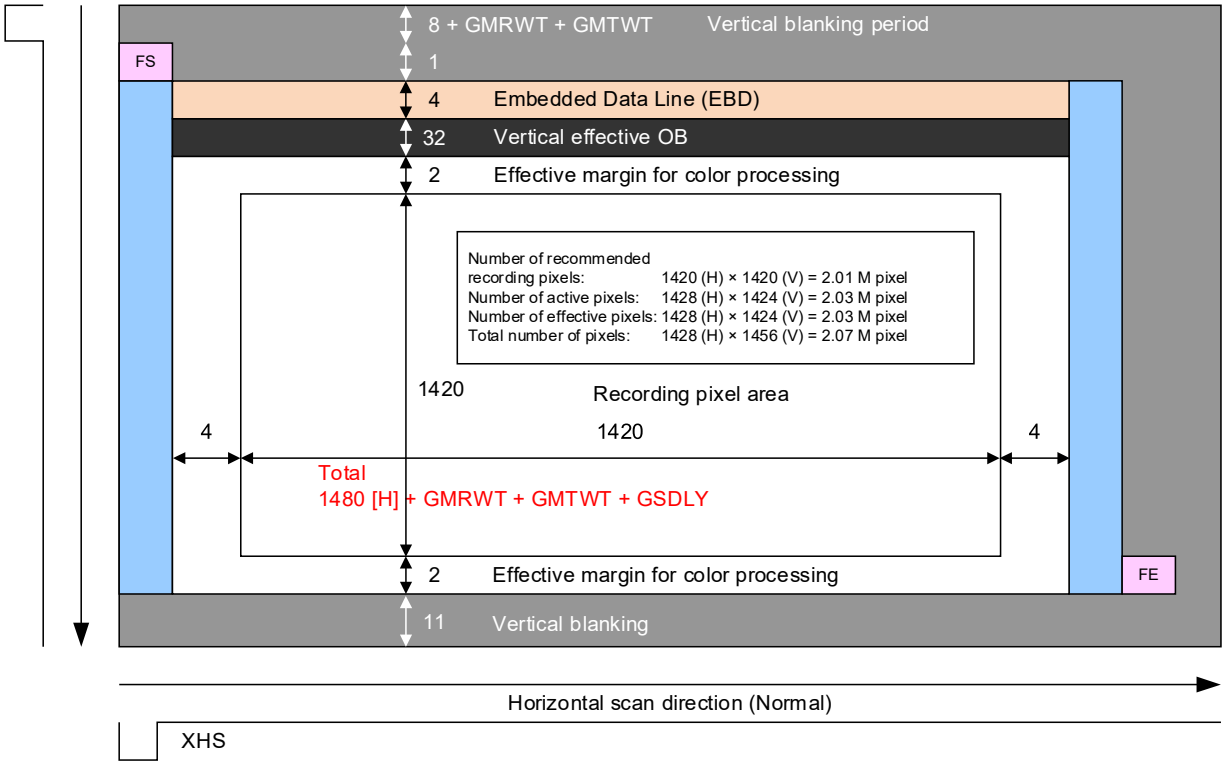
By setting Vertical / Horizontal 1/2 Subsampling mode, the frame rate becomes faster than All-pixel mode.

Register List of Vertical / Horizontal 1/2 subsampling mode

Please set All-pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				4 Lane	2 Lane	4 Lane	2 Lane	4 Lane	2 Lane	
				214.4 [frame/s]	121.7 [frame/s]	180.7 [frame/s]	99.9 [frame/s]	155.4 [frame/s]	84.7 [frame/s]	1188 Mbps
				165.9 [frame/s]	93.1 [frame/s]	138.6 [frame/s]	76.3 [frame/s]	119.3 [frame/s]	64.6 [frame/s]	891 Mbps
				114.2 [frame/s]	63.2 [frame/s]	95.5 [frame/s]	51.6 [frame/s]	81.5 [frame/s]	43.4 [frame/s]	594 Mbps
Chip ID = 02h										
14h	[7:0]	INCKSEL_ST0	0Ah	INCK = 74.25 MHz: 0Ah INCK = 54 MHz: F0h INCK = 37.125 MHz: 05h						
15h	[7:0]	INCKSEL_ST1	22h	INCK = 74.25 MHz: 22h INCK = 54 MHz: D2h INCK = 37.125 MHz: 91h						
16h	[7:0]	INCKSEL_ST2	B1h	INCK = 74.25 MHz: B1h INCK = 54 MHz: 80h INCK = 37.125 MHz: 50h						
18h	[7:0]	INCKSEL_ST3	40h	INCK = 74.25 MHz: 40h INCK = 54 MHz: 18h INCK = 37.125 MHz: 20h						
19h	[7:0]	INCKSEL_ST4	04h	INCK = 74.25 MHz: 04h INCK = 54 MHz: 03h INCK = 37.125 MHz: 02h						
1Bh	[7:0]	INCKSEL_ST5	3Ah	INCK = 74.25 MHz: 3Ah INCK = 54 MHz: 2Ah INCK = 37.125 MHz: 1Dh						
3Ch	[1]		0	1						
	[4:3]	HVMODE	0h	1h						1/2 Subsampling
D0h	[7:0]	VOPB_VBLK_HWIDTH	1020h	0594h						
D1h	[4:0]									
D2h	[7:0]	FINFO_HWIDTH	04B0h	0594h						
D3h	[4:0]									
D4h	[7:0]	VMAX	000CD4h	634h	604h	620h	5FCh	614h	5F4h	1188 Mbps
D5h	[7:0]			61Ch	5F4h	610h	5F0h	604h	5E8h	891 Mbps
D6h	[7:0]			604h	5E8h	5F4h	5E4h	5F0h	5E4h	594 Mbps
D8h	[7:0]	HMAX	0081h	DAh	18Ch	106h	1E5h	133h	23Fh	1188 Mbps
				11Eh	20Bh	159h	280h	194h	2F8h	891 Mbps
D9h	[7:0]			1A6h	309h	1FEh	3B9h	257h	46Ch	594 Mbps
E2h	[7:0]	GMRWT	10h	0Ch	08h	08h	04h	08h	04h	1188 Mbps
				08h	04h	08h	04h	08h	04h	891 Mbps
				08h	04h	04h	04h	04h	04h	594 Mbps
E3h	[7:0]	GMTWT	70h	44h	24h	38h	20h	30h	1Ch	1188 Mbps
				34h	1Ch	2Ch	18h	24h	14h	891 Mbps
				24h	14h	1Ch	10h	18h	10h	594 Mbps
E5h	[7:0]	GAINDLY	04h	04h						
E6h	[7:0]	GSDLY	30h	1Ch	10h	18h	10h	14h	0Ch	1188 Mbps
				18h	0Ch	14h	0Ch	10h	08h	891 Mbps
				10h	08h	0Ch	08h	0Ch	08h	594 Mbps
Chip ID = 04h										
00h	[5:4]	ADBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
1Ch	[7:0]	INCKSEL_N0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h						
1Dh	[7:0]	INCKSEL_N1	05h	05h						

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				4 Lane	2 Lane	4 Lane	2 Lane	4 Lane	2 Lane	
				214.4 [frame/s]	121.7 [frame/s]	180.7 [frame/s]	99.9 [frame/s]	155.4 [frame/s]	84.7 [frame/s]	1188 Mbps
				165.9 [frame/s]	93.1 [frame/s]	138.6 [frame/s]	76.3 [frame/s]	119.3 [frame/s]	64.6 [frame/s]	891 Mbps
				114.2 [frame/s]	63.2 [frame/s]	95.5 [frame/s]	51.6 [frame/s]	81.5 [frame/s]	43.4 [frame/s]	594 Mbps
1Eh	[7:0]	INCKSEL_N2	E0h	INCK = 74.25 MHz: E0h INCK = 54 MHz: 34h INCK = 37.125 MHz: E0h						
1Fh	[7:0]	INCKSEL_N3	00h	INCK = 74.25 MHz: 00h INCK = 54 MHz: 01h INCK = 37.125 MHz: 00h						
20h	[7:0]	INCKSEL_S0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h						
21h	[7:0]	INCKSEL_S1	05h	05h						
22h	[7:0]	INCKSEL_S2	E0h	INCK = 74.25 MHz: E0h INCK = 54 MHz: 34h INCK = 37.125 MHz: E0h						
23h	[7:0]	INCKSEL_S3	00h	INCK = 74.25 MHz: 00h INCK = 54 MHz: 01h INCK = 37.125 MHz: 00h						
24h	[7:0]	INCKSEL_D0	10h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h						
25h	[7:0]	INCKSEL_D1	14h	14h						
26h	[7:0]	INCKSEL_D2	20h	INCK = 74.25 MHz: 80h INCK = 54 MHz: B0h INCK = 37.125 MHz: 80h						1188 Mbps / 594 Mbps
				INCK = 74.25 MHz: C0h INCK = 54 MHz: 08h INCK = 37.125 MHz:C0h						891 Mbps
27h	[7:0]	INCKSEL_D3	C0h	80h						1188 Mbps
				INCK = 74.25 MHz: D0h INCK = 54 MHz: D1h INCK = 37.125 MHz: D0h						891 Mbps
				90h						594 Mbps
3Ch 3Dh	[7:1] [0]	LLBLANK	18h	0Ch						
3Eh	[7:2]		16h	0Ah						
Chip ID = 06h										
30h	[1:0]	ODBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
Chip ID = 07h										
21h	[7:0]		A9h	41h						
46h	[7:0]		2Ah	10h						
B4h B5h	[7:0] [3:0]	BLKLEVEL	03Ch	00Fh		03Ch		0F0h		Recommended value
Chip ID = 0Bh										
04h	[2:0]	LANESEL	0h	2h	N/A	2h	N/A	2h	N/A	4 Lane CSI-2
				N/A	3h	N/A	3h	N/A	3h	2 Lane CSI-2
Chip ID = 0Eh										
A4h A5h	[7:0] [7:0]	TXCLKESC_ FREQ	12C0h	INCK = 74.25 MHz: 12C0h INCK = 54 MHz: 0D80h INCK = 37.125 MHz: 0980h						
B4h to C7h	[7:0] [7:0]	Global Timing Registers	–	Refer to Global Timing Register Setting						



Pixel Array Image Drawing in Vertical / Horizontal 1/2 subsampling mode
(CSI-2 output Shutter stabilization wait time is not included)

18.3.5. 2 × 2 FD binning mode

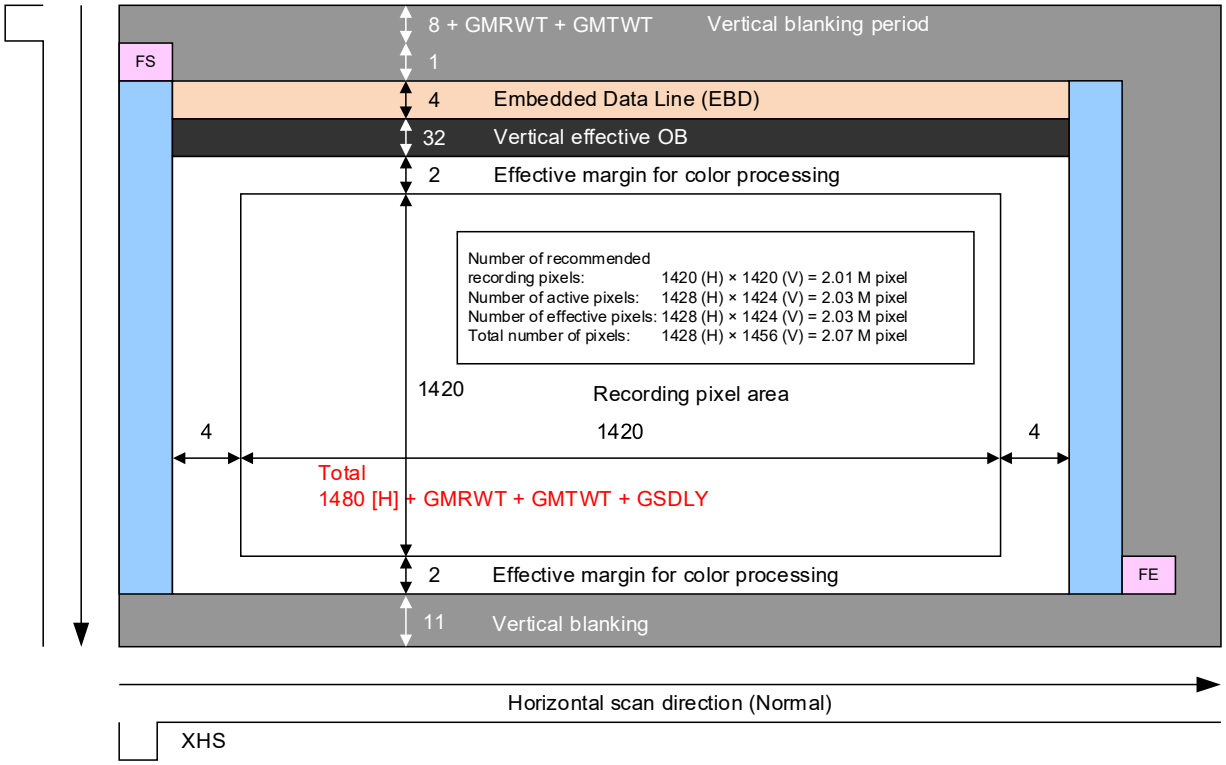
By setting 2 × 2 FD binning mode, the frame rate becomes faster than All-pixel mode.

Register List of 2 × 2 FD binning mode

Please set All-pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				4 Lane	2 Lane	4 Lane	2 Lane	4 Lane	2 Lane	
				214.4 [frame/s]	121.7 [frame/s]	180.7 [frame/s]	99.9 [frame/s]	155.4 [frame/s]	84.7 [frame/s]	1188 Mbps
				165.9 [frame/s]	93.1 [frame/s]	138.6 [frame/s]	76.3 [frame/s]	119.3 [frame/s]	64.6 [frame/s]	891 Mbps
				114.2 [frame/s]	63.2 [frame/s]	95.5 [frame/s]	51.6 [frame/s]	81.5 [frame/s]	43.4 [frame/s]	594 Mbps
Chip ID = 02h										
14h	[7:0]	INCKSEL_ST0	0Ah	INCK = 74.25 MHz: 0Ah INCK = 54 MHz: F0h INCK = 37.125 MHz: 05h						
15h	[7:0]	INCKSEL_ST1	22h	INCK = 74.25 MHz: 22h INCK = 54 MHz: D2h INCK = 37.125 MHz: 91h						
16h	[7:0]	INCKSEL_ST2	B1h	INCK = 74.25 MHz: B1h INCK = 54 MHz: 80h INCK = 37.125 MHz: 50h						
18h	[7:0]	INCKSEL_ST3	40h	INCK = 74.25 MHz: 40h INCK = 54 MHz: 18h INCK = 37.125 MHz: 20h						
19h	[7:0]	INCKSEL_ST4	04h	INCK = 74.25 MHz: 04h INCK = 54 MHz: 03h INCK = 37.125 MHz: 02h						
1Bh	[7:0]	INCKSEL_ST5	3Ah	INCK = 74.25 MHz: 3Ah INCK = 54 MHz: 2Ah INCK = 37.125 MHz: 1Dh						
3Ch	[1]		0	1						
	[4:3]	HVMODE	0h	2h						2×2 FD binning
D0h	[7:0]	VOPB_VBLK_ HWIDTH	1020h	0594h						
D1h	[4:0]									
D2h	[7:0]	FINFO_ HWIDTH	04B0h	0594h						
D3h	[4:0]									
D4h	[7:0]	VMAX	000CD4h	634h	604h	620h	5FCh	614h	5F4h	1188 Mbps
D5h	[7:0]			61Ch	5F4h	610h	5F0h	604h	5E8h	891 Mbps
D6h	[7:0]			604h	5E8h	5F4h	5E4h	5F0h	5E4h	594 Mbps
D8h	[7:0]	HMAX	0081h	DAh	18Ch	106h	1E5h	133h	23Fh	1188 Mbps
				11Eh	20Bh	159h	280h	194h	2F8h	891 Mbps
D9h	[7:0]			1A6h	309h	1FEh	3B9h	257h	46Ch	594 Mbps
E2h	[7:0]	GMRWT	10h	0Ch	08h	08h	04h	08h	04h	1188 Mbps
				08h	04h	08h	04h	08h	04h	891 Mbps
				08h	04h	04h	04h	04h	04h	594 Mbps
E3h	[7:0]	GMTWT	70h	44h	24h	38h	20h	30h	1Ch	1188 Mbps
				34h	1Ch	2Ch	18h	24h	14h	891 Mbps
				24h	14h	1Ch	10h	18h	10h	594 Mbps
E5h	[7:0]	GAINDLY	04h	04h						
E6h	[7:0]	GSDLY	30h	1Ch	10h	18h	10h	14h	0Ch	1188 Mbps
				18h	0Ch	14h	0Ch	10h	08h	891 Mbps
				10h	08h	0Ch	08h	0Ch	08h	594 Mbps
Chip ID = 04h										
00h	[5:4]	ADBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
1Ch	[7:0]	INCKSEL_N0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h						
1Dh	[7:0]	INCKSEL_N1	05h	05h						

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				4 Lane	2 Lane	4 Lane	2 Lane	4 Lane	2 Lane	
				214.4 [frame/s]	121.7 [frame/s]	180.7 [frame/s]	99.9 [frame/s]	155.4 [frame/s]	84.7 [frame/s]	1188 Mbps
				165.9 [frame/s]	93.1 [frame/s]	138.6 [frame/s]	76.3 [frame/s]	119.3 [frame/s]	64.6 [frame/s]	891 Mbps
				114.2 [frame/s]	63.2 [frame/s]	95.5 [frame/s]	51.6 [frame/s]	81.5 [frame/s]	43.4 [frame/s]	594 Mbps
1Eh	[7:0]	INCKSEL_N2	E0h	INCK = 74.25 MHz: E0h INCK = 54 MHz: 34h INCK = 37.125 MHz: E0h						
1Fh	[7:0]	INCKSEL_N3	00h	INCK = 74.25 MHz: 00h INCK = 54 MHz: 01h INCK = 37.125 MHz: 00h						
20h	[7:0]	INCKSEL_S0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h						
21h	[7:0]	INCKSEL_S1	05h	05h						
22h	[7:0]	INCKSEL_S2	E0h	INCK = 74.25 MHz: E0h INCK = 54 MHz: 34h INCK = 37.125 MHz: E0h						
23h	[7:0]	INCKSEL_S3	00h	INCK = 74.25 MHz: 00h INCK = 54 MHz: 01h INCK = 37.125 MHz: 00h						
24h	[7:0]	INCKSEL_D0	10h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h						
25h	[7:0]	INCKSEL_D1	14h	14h						
26h	[7:0]	INCKSEL_D2	20h	INCK = 74.25 MHz: 80h INCK = 54 MHz: B0h INCK = 37.125 MHz: 80h						1188 Mbps / 594 Mbps
				INCK = 74.25 MHz: C0h INCK = 54 MHz: 08h INCK = 37.125 MHz:C0h						891 Mbps
27h	[7:0]	INCKSEL_D3	C0h	80h						1188 Mbps
				INCK = 74.25 MHz: D0h INCK = 54 MHz: D1h INCK = 37.125 MHz: D0h						891 Mbps
				90h						594 Mbps
3Ch 3Dh	[7:1] [0]	LLBLANK	18h	0Ch						
3Eh	[7:2]		16h	0Ah						
Chip ID = 06h										
30h	[1:0]	ODBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
Chip ID = 07h										
21h	[7:0]		A9h	41h						
46h	[7:0]		2Ah	10h						
B4h B5h	[7:0] [3:0]	BLKLEVEL	03Ch	00Fh		03Ch		0F0h		Recommended value
Chip ID = 0Bh										
04h	[2:0]	LANESEL	0h	2h	N/A	2h	N/A	2h	N/A	4 Lane CSI-2
				N/A	3h	N/A	3h	N/A	3h	2 Lane CSI-2
Chip ID = 0Eh										
A4h A5h	[7:0] [7:0]	TXCLKESC_ FREQ	12C0h	INCK = 74.25 MHz: 12C0h INCK = 54 MHz: 0D80h INCK = 37.125 MHz: 0980h						
B4h to C7h	[7:0] [7:0]	Global Timing Registers	–	Refer to Global Timing Register Setting						



Pixel Array Image Drawing in 2 × 2 FD binning mode
(CSI-2 output Shutter stabilization wait time is not included)

19. Description of Various Functions

19.1. Standby mode

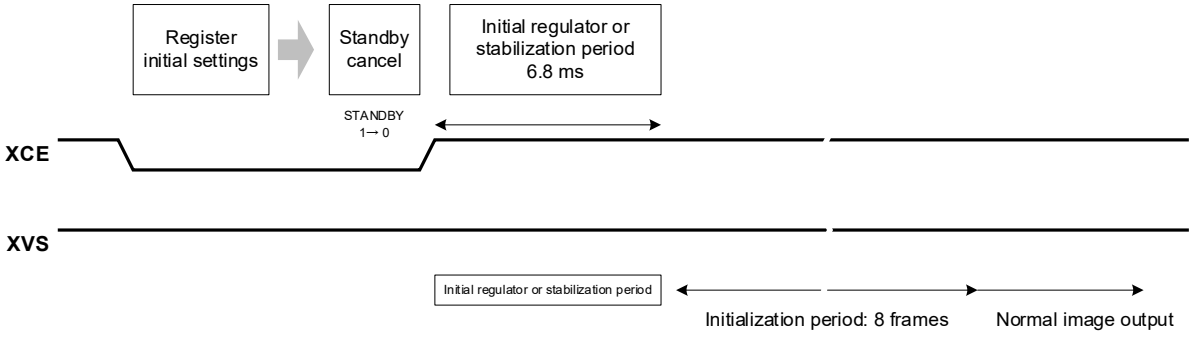
This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

Register List of Standby setting

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I²C	bit			
STANDBY [0]	02h	00h (3000h)	[0]	1	1: Standby 0: Operating	Register communication is executed even in standby mode.

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to “0”. Some time is required for sensor internal circuit stabilization after standby mode is canceled. For details on the sequence of setting and cancel of standby mode, see the section of “Sensor Setting Flow”.

After standby mode is canceled, a normal image is output from the 9 frames after internal regulator stabilization (6.8 ms or more).



Sequence from Standby Cancel to Stable Image Output

19.2. Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode.
The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this pin status during operation.)

Slave Mode (XMASTER = 1h)

Input a vertical sync signal to XVS and input a horizontal sync signal to XHS. For sync signal interval, input data lines to output for vertical sync signal and 1 H period designated in each operating mode for horizontal sync signal. See the section of "Readout Drive Modes" for the number of output data line and 1 H period.
In this sensor, the low-power consumption function is always ON, so be sure to set HMAX [15:0] even in slave mode. The setting value of HMAX [15:0] can be calculated using the following.

HMAX [15:0] = “Number of INCK in 1H” × 74.25 / INCK Frequency

Master Mode (XMASTER = 0h)

Set “XMSTA = 0” in order to start the operation. In addition, set the count number of sync signal in vertical direction by the VMAX [23:0] register and the clock number in horizontal direction by the HMAX [15:0] register. See the description of operation mode for details of the section of “Readout Drive Modes”.
In master mode, it is possible to output horizontal / vertical sync signals from XHS pin / XVS pin by setting register: SYNCSEL [1:0].

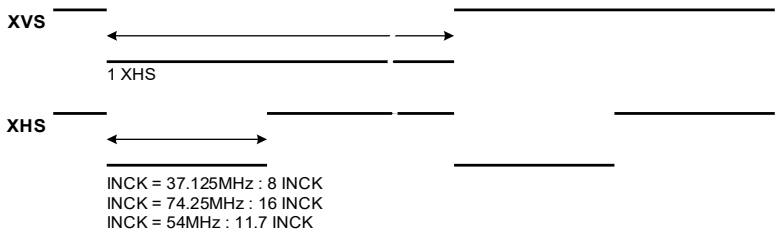
Pin Processing

Pin name	Pin processing	Operation mode	Remarks
XMASTER pin	Low fixed	Master mode	High: OV_{DD} Low: GND
	High fixed	Slave mode	

Register List of Slave Mode and Master Mode

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I^2C	Bit			
XMSTA [0]	02h	10h (3010h)	[0]	1	1: Master operation ready (Initial value) 0: Master operation start	The master operation starts by setting 0.
VMAX [23:0]		D4h (30D4h)	[7:0]	000CD4h	See the item of each drive mode	Line number per frame designated (Master mode and Slave mode common setting.)
		D5h (30D5h)	[7:0]			
		D6h (30D6h)	[7:0]			
HMAX [15:0]		D8h (30D8h)	[7:0]	0081h	See the item of each drive mode	Clock number per line designated (Master mode and Slave mode common setting.)
		D9h (30D9h)	[7:0]			
SYNCSEL [1:0]	06h	3Ch (343Ch)	[5:4]	0h	0h: Normal Output 3h: Hi-Z	XHS, XVS pin setting in Master mode

XVS / XHS Output in Master Mode



The XVS and XHS are output in timing that set “XMSTA = 0” after standby is released. The XVS and XHS are output asynchronous with other input or output signals. In addition, the output signals are output with an undefined latency time (system delay) relative to the XHS. Therefore, refer to the packet headers output from the sensor and perform synchronization.

19.3. Gain Adjustment Function

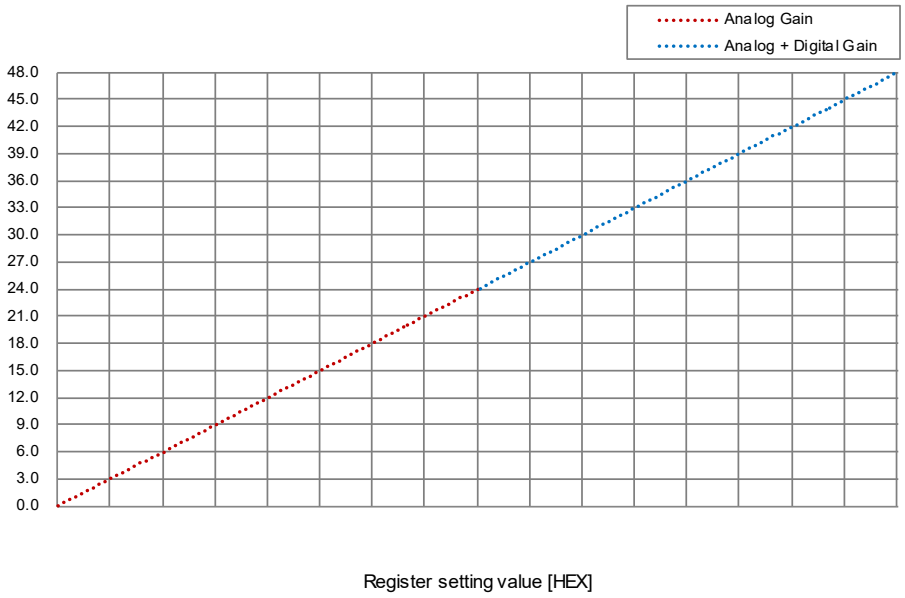
PGC

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block.
The total of analog gain and digital gain can be set up to 48 dB by the GAIN [8:0] register setting.

The value which is ten times the gain is set to register. (0.1 dB step)

Example)
When set to 6 dB:

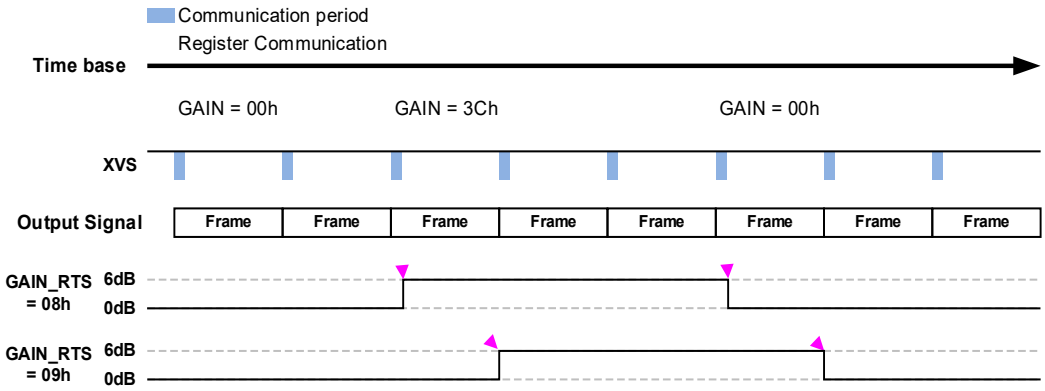
6 × 10 = 60d, GAIN = 03Ch



Register List of Gain setting

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I²C	bit		Setting range	
GAIN_RTS [7:0]	07h	02h (3502h)	[7:0]	00h	08h or 09h	08h: Gain reflect at the frame 09h: Gain reflect at the next frame
GAIN [8:0]		14h (3514h)	[7:0]	000h	000h to 1E0h (0d to 480d)	Setting value: Gain [dB] × 10
		15h (3515h)	[0]			

Gain Reflection Timing is changed by the set value of the GAIN_RTS [7:0] register as shown below.



Gain Reflection Timing

19.4. Black Level Adjustment Function

The black level offset (offset variable range: 000h to FFFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [11:0] register. When the BLKLEVEL [11:0] setting is increased by 1 LSB, the black level is increased by 1 LSB.

* Use with values shown below is recommended.
  8 bit output: 00Fh (15d)
  10 bit output: 03Ch (60d)
  12 bit output: 0F0h (240d)

Register List of Black level adjustment

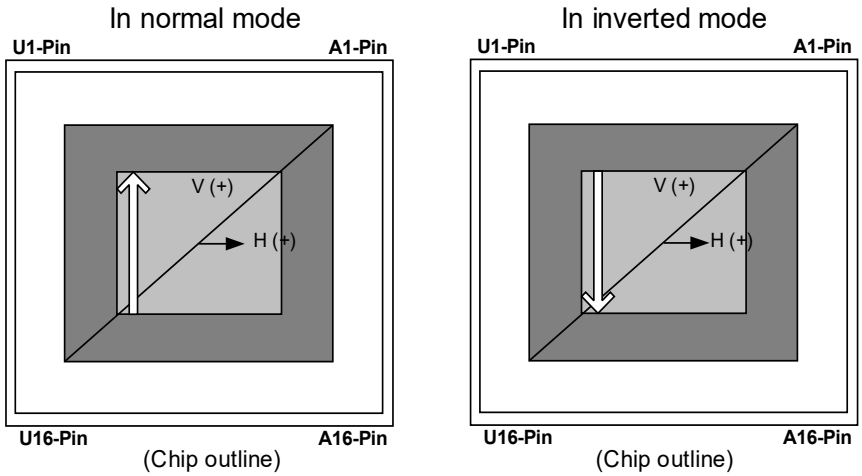
Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I^2C	bit		
BLKLEVEL [11:0]	07h	B4h (35B4h)	[7:0]	03Ch	000h to FFFh
		B5h (35B5h)	[3:0]		

19.5. Horizontal / Vertical Normal Operation and Inverted Operation

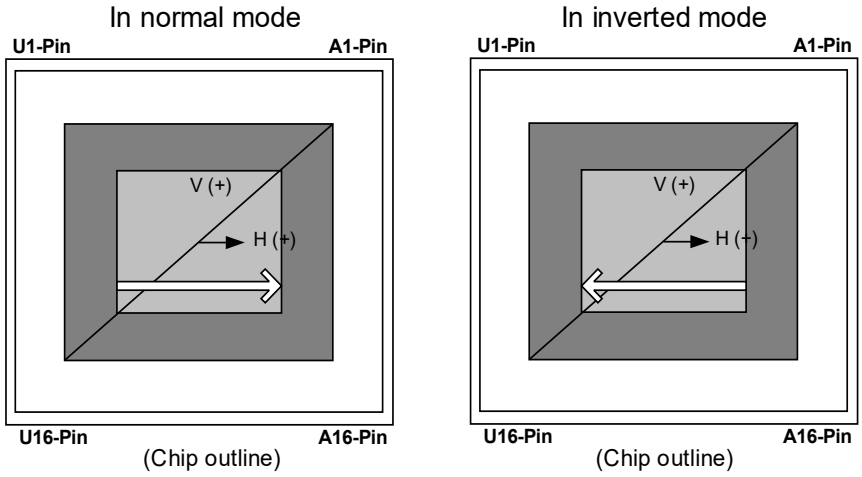
The sensor readout direction (normal / inverted) in vertical direction can be switched by the VREVERSE register setting and sensor readout direction (normal / inverted) in horizontal direction can be switched by the HREVERSE register setting. See the section of “Readout Drive Modes” for the order of readout lines in normal and inverted modes.
One invalid frame is generated when reading immediately after the readout vertical direction change in order to switch the normal operation and inversion between frames.

Register List of Readout Drive Direction setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
VREVERSE [0]	04h	04h (3204h)	[0]	0	0: Normal (Initial value) 1: Inverted
HREVERSE [0]			[1]	0	0: Normal (Initial value) 1: Inverted



Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

19.6. Shutter and Exposure Time Settings

This sensor has a global shutter function that integrates to all line collectively by using memory in each pixel. This sensor has a variable electronic shutter function that can control the exposure time in line units for adjust the exposure time. This sensor transferred signal to memory in pixel after the exposure (memory transfer), then this sensor performs output in which readout operation is performed sequentially for each line in sync with the XHS signal. This sensor has trigger mode that can be controlled exposure start timing and memory transfer timing by trigger.

Note) For exposure time control, an image which reflects the setting is output from the frame after the setting changes.

In this item, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

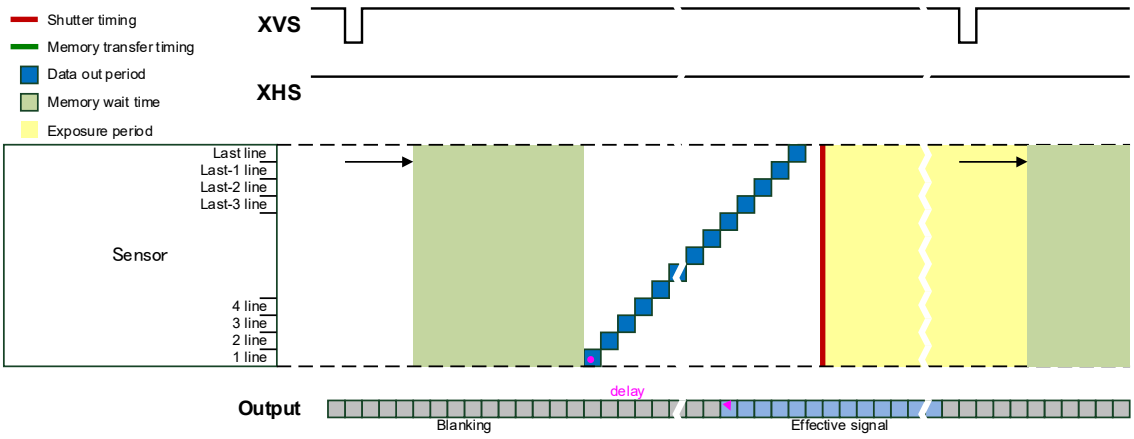


Image Drawing of Global Shutter (Normal mode) Operation

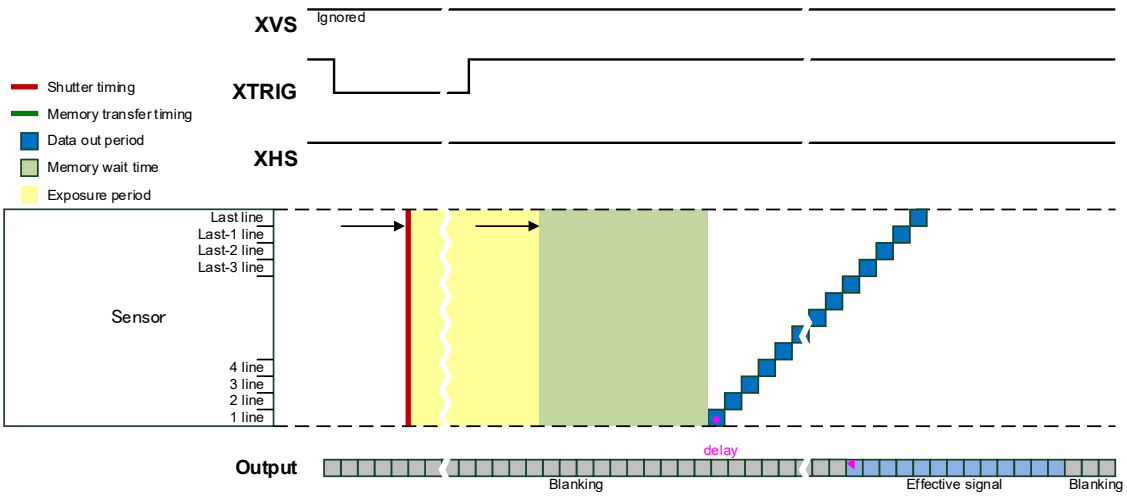


Image Drawing of Global Shutter (Sequential Trigger mode) Operation

19.6.1. Global Shutter (Normal Mode) Operation

The exposure time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the exposure time is controlled by the SHS [23:0] register. For setting value of SHS [23:0], see the table “List of Exposure Setting”. When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit. When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX [23:0] register. The number of lines per frame differs according to the readout mode.
When XVS is input at intervals shorter than the recommended setting value of VMAX [23:0] in each readout mode, interrupt operation is performed.

Calculation Formula of Exposure Time

Exposure time [µs] = (1 H period [µs]) × (Number of lines per frame - SHS) + 2.47 [µs][*1]
[*1]: Exposure time error (t_{OFFSET})

Register List of Shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I^2C	bit		
VMAX [23:0]	02h	D4h (30D4h)	[7:0]	000CD4h	Set the number of lines per frame (only in master mode)
		D5h (30D5h)	[7:0]		
		D6h (30D6h)	[7:0]		
GMRWT [7:0]		E2h (30E2h)	[7:0]	10h	For setting, refer to the register list of each readout mode
GMTWT [7:0]		E3h (30E3h)	[7:0]	70h	For setting, refer to the register list of each readout mode
GSDLY [7:0]		E6h (30E6h)	[7:0]	30h	For setting, refer to the register list of each readout mode
VINT_EN_NOR [0]	04h	3Eh (323Eh)	[1]	1	Setting of Interrupt mode in Normal Mode 0: V interrupt is disable 1: V interrupt is enable
SHS [23:0]		40h (3240h)	[7:0]	000070h	Sets the shutter sweep time. (memory wait time (GMTWT value) + 4) to (Number of lines per frame - 1)
		41h (3241h)	[7:0]		
		42h (3242h)	[7:0]		

When set VMAX [23:0] to a number of V lines or more than that noted for each operating mode, the imaging characteristics are not guaranteed.

List of Exposure Setting

Drive mode	Memory transfer stabilization wait time [H]	Number of lines per frame [DEC]	SHS Setting value [DEC]	Exposure Setting value [H]	AD 12 bit, 1188 Mbps/Lane, 4 Lane output (Maximum frame rate)	
					Frame rate [frame/s]	Actual exposure [ms][*3]
All-pixel	26 (GMTWT[*1])	2976 (VMAX)	2975	1	43.4	0.010
			2974	2		0.018
			…	…		…
			31	2945		22.769
			30	2946		22.777
1/2 Subsampling, 2 × 2 FD binning	48 (GMTWT[*1])	1556 (VMAX)	1555	1	155.4	0.007
			1554	2		0.011
			…	…		…
			53	1503		6.217
			52	1504		6.221
ROI Overlap ROI	All-pixel (GMTWT[*1])	V_{TR}[*2]	V_{TR}-1	1	[*2]	0.010
			V_{TR}-2	2		0.018
			…	…		…
			31	V_{TR}-31		[*4]
			30	V_{TR}-30		

[*1] For GMTWT, refer to the register list of each readout mode.
[*2] V_{TR} and the frame rate, refer to the section “ROI mode” in “Readout Drive Modes”.
[*3] INCK frequency is input by typical value. and t_{OFFSET} (2.47 [µs]) is included.
[*4] Conform to the calculation formula of exposure time. (Number of lines per frame = V_{TR})

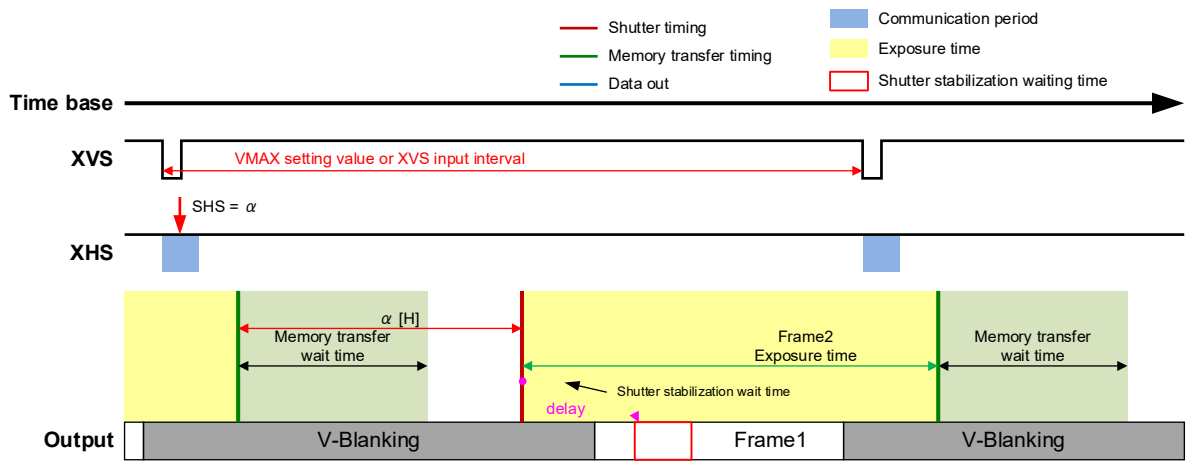


Image Drawing of Global Shutter (Normal Mode)

Interrupt Operation

In case of “VINT_EN_NOR = 1h”, the image drawing when the interrupt operation is generated is shown below. When the next XVS is input during read of the frame (Frame 1 in the figure below), Frame 1 becomes an invalid frame. XVS input timing of interrupt generating corresponds to recommended setting value of VMAX [23:0] in each readout mode.
In case of "VINT_EN_NOR = 0h", XVS input at intervals shorter than the recommended setting value of VMAX [23:0] is invalid.

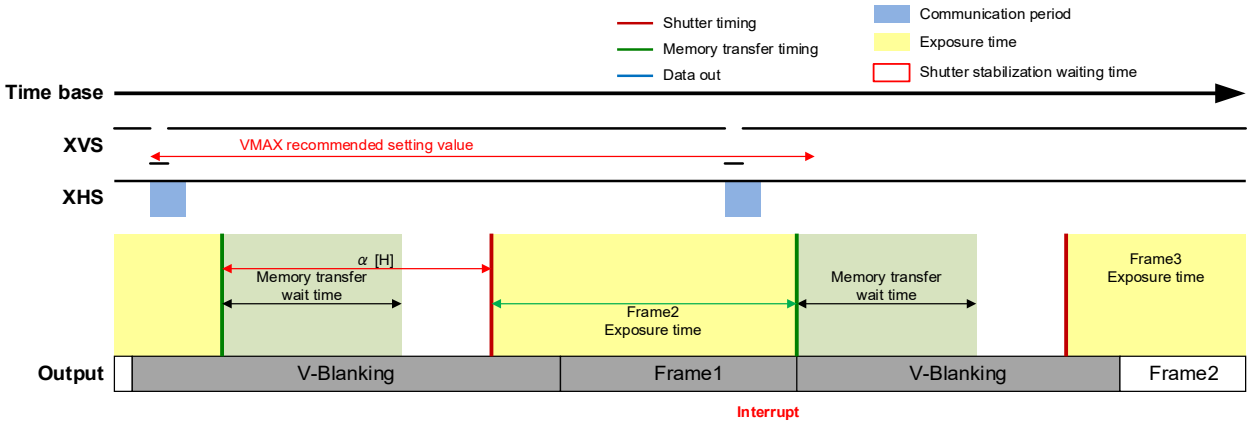


Image Drawing of Interrupt Operation in Global Shutter (Normal Mode)

19.6.2. Global Shutter (Sequential Trigger Mode) Operation

The exposure time can be controlled by varying the pulse width that is input to XTRIG1 pin. The pulse width designated in XHS unit [H]. For the transition from normal mode to Sequential trigger mode, set 1 to the register TRIGMODE [2:0]. The XVS input signal is ignored during Sequential trigger mode operating. In case of inputting trigger continuously, there are period which prohibit the trigger rise input (t_{TGPD}) and fall input (t_{TGES}) based on the previous trigger rise.
When the trigger rise is input before the rise input prohibited period (t_{TGPD}), interrupt operation starts.
This function is slave mode only. The number of lines per frame differs according to the operating mode.
XTRIG2 pin is set Open (Hi-Z) or fixed to High after power-on sequence.

Calculation Formula of Exposure Time

Exposure time [µs] = (1 H period [µs]) × (XTRIG low level pulse width [H][*2]) + 2.47 [µs][*1]
[*1]: Exposure time error (t_{OFFSET})
[*2]: Low level pulse width is counted by XHS pulse.

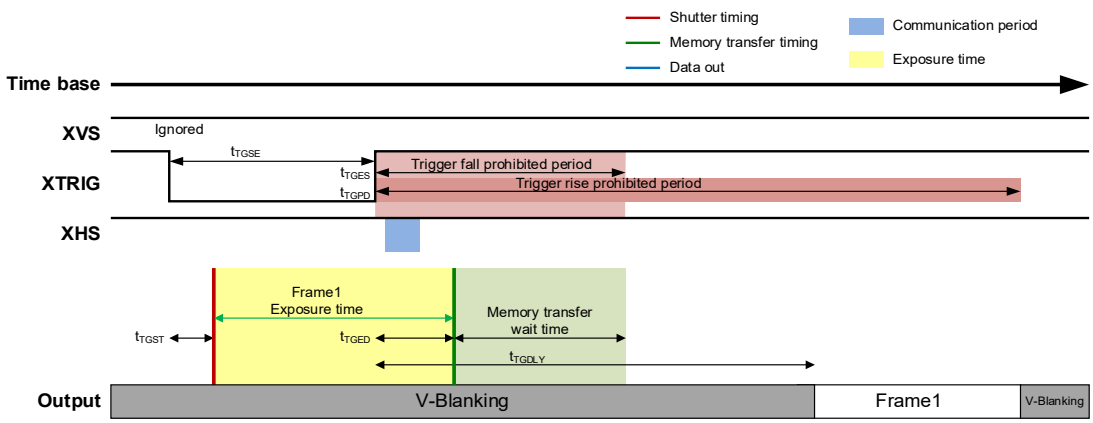
Register List of Shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
XMSTA [0]	02h	10h (3010h)	[0]	1	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop
VINT_EN [0]	04h	3Eh (323Eh)	[0]	1	Setting of Interrupt mode in Trigger Mode 0: V interrupt is disable 1: V interrupt is enable
TRIGMODE [2:0]	06h	00h (3400h)	[2:0]	0h	Global shutter mode setting 0h: Normal mode 1h: Sequential Trigger mode 2h: Fast Trigger mode
TRIGTIMING [1:0]	06h	00h (3400h)	[4:3]	0h	Trigger mode setting 0h: Normal mode 1h: Trigger mode Others: Setting prohibited

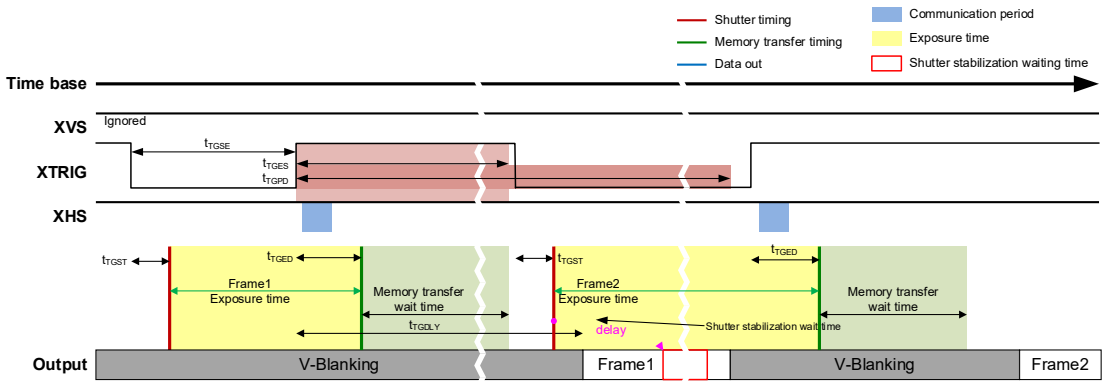
Parameter List of Global Shutter (Sequential Trigger Mode)

Item	Symbol	Min.	Typ.	Max.	Unit
Integration start delay (All-pixel / ROI / 1/2 Subsampling / 2 x 2 FD binning)	t_{TGST}	4 + GMRWT[*1]	—	5 + GMRWT[*1]	H
Integration end delay (All-pixel / ROI / 1/2 Subsampling / 2 x 2 FD binning)	t_{TGED}	4 + GMRWT[*1] + t_{OFFSET}	—	5 + GMRWT[*1] + t_{OFFSET}	H
Pulse width	t_{TGSE}	1	—	—	H
Next trigger fall prohibited period (All-pixel, ROI, 1/2 Subsampling, 2 × 2 FD binning)	t_{TGES}	5 + GMRWT[*1] + GMTWT[*1]	—	—	H
Next trigger rise prohibited period (All-pixel / 1/2 Subsampling / 2 × 2 FD binning)	t_{TGPD}	VMAX	—	—	H
Next trigger rise prohibited period (ROI)		V_{TR}[*2]	—	—	
Data output delay (All-pixel / ROI)	t_{TGDLY}	—	15 + GMRWT[*1] + GMTWT[*1]	—	H
Data output delay (1/2 Subsampling / 2 × 2 FD binning))		—	13 + GMRWT[*1] + GMTWT[*1]	—	

[*1] For GMRWT and GMTWT, refer to the register list of each readout mode.
[*2] V_{TR} (See the section “ROI mode” in “Readout Drive Modes”)



Single shutter Image Drawing of Global Shutter (Sequential Trigger Mode)



Multi shutter image Drawing of Global Shutter (Sequential Trigger Mode)

Interrupt Operation

In case of “VINT_EN = 1h”, the image drawing when the interrupt operation is generated is shown below. When the trigger is raised again and the next frame is output during read of the frame for which read was started by a trigger rise (Frame 1 in the figure below), Frame 1 becomes an invalid frame. Trigger timing of interrupt generating corresponds to t_{TGPD} in Parameter List of Global Shutter (Trigger Mode)
In case of “VINT_EN = 0h”, both of the rising edge and the falling edge of the trigger signal are ignored in t_{TGPD} (Prohibit period).

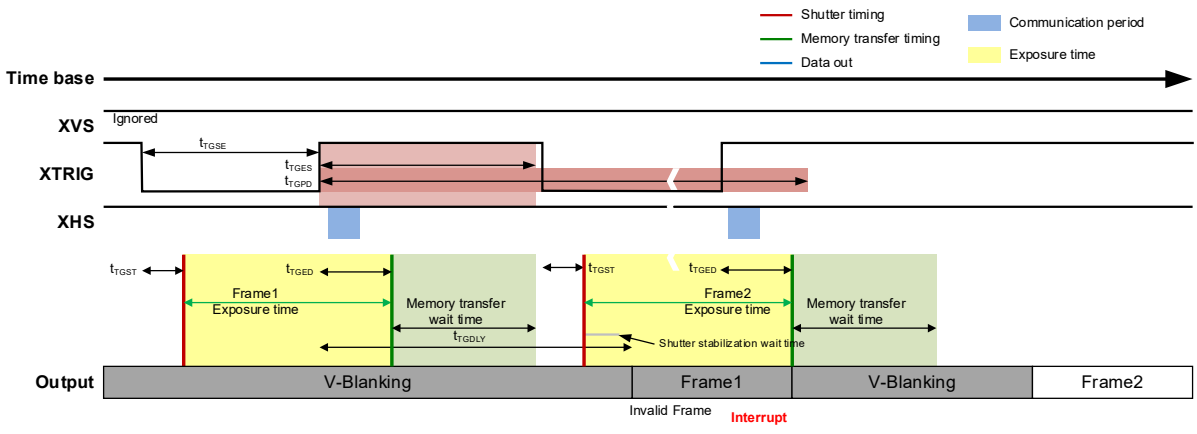


Image Drawing of Interrupt Operation in Global Shutter (Sequential Trigger Mode)

19.6.3. Global Shutter (Fast Trigger Mode) Operation

Fast trigger mode is the trigger mode that starts exposure at fall of XTRIG1 immediately.
In the Fast trigger mode, set the register TRIGMODE [2:0] to 2h at standby state, and then release standby. In the Fast trigger mode, the image size can not be changed during the operation.
This mode supports Master mode only.
XTRIG2 pin is set Open (Hi-Z) or fixed to High after power-on sequence.

Calculation Formula of Exposure Time

Exposure time [µs] = (XTRIG low level pulse width [µs]) + (GMRWT [H] × 1 H period [µs]) + 2.53 [µs][*1]
[*1]: Exposure time error (t_{OFFSET})

Register List of Shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I^2C	bit		
XMSTA [0]	02h	10h (3010h)	[0]	1	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop
TRIGMODE [2:0]	06h	00h (3400h)	[2:0]	0h	Global shutter mode setting 0h: Normal mode 1h: Sequential Trigger mode 2h: Fast Trigger mode
TRIGTIMING [1:0]	06h	00h (3400h)	[4:3]	0h	Trigger mode setting 0h: Normal mode 1h: Trigger mode Others: Setting prohibited

Parameter List of Global Shutter (Fast Trigger Mode)

Item	Symbol	Min.	Typ.	Max.	Unit
Integration start delay (All-pixel / ROI / 1/2 Subsampling / 2 x 2 FD binning)	t_{TGST}	—	—	0.1	µs
Integration end delay (All-pixel / ROI / 1/2 Subsampling / 2 x 2 FD binning)	t_{TGED}	—	—	0.1 + GMRWT[*1] + t_{OFFSET}	µs
Pulse width	t_{TGSE}	0.05	—	—	µs
Next trigger rise / fall prohibited period (All-pixel / 1/2 Subsampling / 2 × 2 FD binning)	t_{TGPD}	VMAX	—	—	H
Next trigger rise / fall prohibited period (ROI)		V_{TR}[*2]	—	—	
Data output delay (All-pixel / ROI)	t_{TGDLY}	—	11 + GMRWT[*1] + GMTWT[*1]	—	H
Data output delay (1/2 Subsampling / 2 × 2 FD binning))		—	9 + GMRWT[*1] + GMTWT[*1]	—	

[*1] For GMRWT and GMTWT, refer to the register list of each readout mode.
[*2] V_{TR} (see the section “ROI mode” in “Readout Drive Modes”).

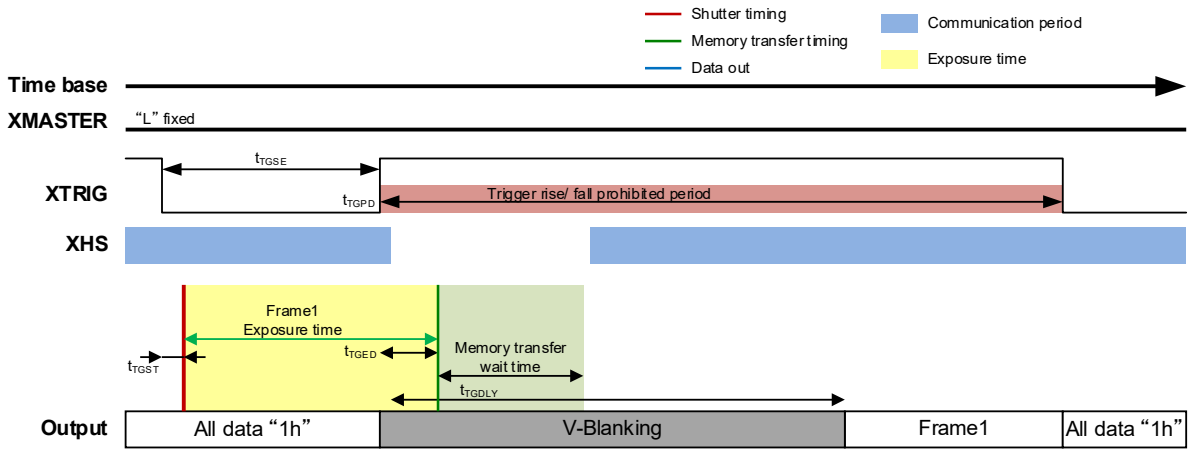


Image Drawing of Global Shutter (Fast Trigger Mode) (4-wire)

19.6.4. Mode Transitions of Global Shutter Operation

The sensor can be switched between normal mode and trigger mode in global shutter operation by setting the register TRIGMODE [2:0]. The sensor will transition to normal mode or trigger mode “GMRWT [7:0] (H) + GMTWT [7:0] (H)” after the register TRIGMODE [2:0] is set.
(The XVS and XTRIG input during transition are prohibited.)
In case of Fast Trigger mode, the mode transition must be done via sensor standby.

Transition from Normal Mode to Sequential Trigger Mode

The sensor will transition from normal mode to Sequential trigger mode after setting “TRIGMODE [2:0] = 1h”. The XVS input is ignored after transition to trigger mode. Trigger input is prohibited for a “GMRWT [7:0] (H) + GMTWT [7:0] (H)” period after the register TRIGMODE [2:0] is set. When TRIGMODE [2:0] is set during data read, read operation is stopped and that frame becomes an invalid frame.

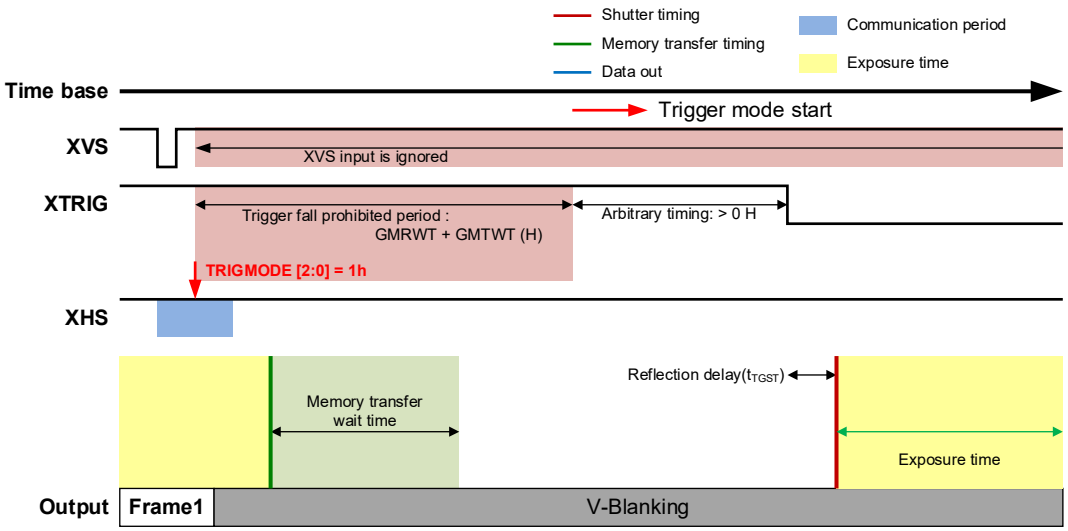


Image Drawing of Transition from Normal Mode to Sequential Trigger Mode

Transition from Sequential Trigger Mode to Normal Mode

The sensor will transition from trigger mode to normal mode after setting “TRIGMODE [2:0] = 0h”. Start XVS input after transition to normal mode. Set TRIGMODE [2:0] after Next trigger rise prohibited period (t_{TGPD}) has passed. When TRIGMODE [2:0] is set before t_{TGPD}, read operation is stopped and that frame becomes an invalid frame.

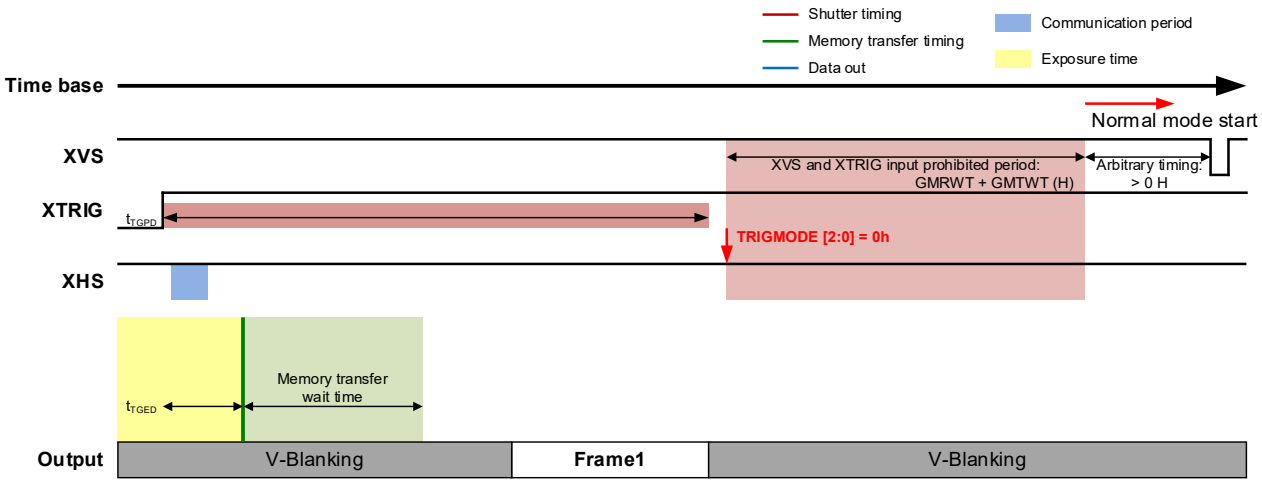


Image Drawing of Transition from Sequential Trigger Mode to Normal Mode

19.6.5. Pulse Output Function

This sensor has a pulse output function that indicates each state of shutter operation.

TOUT0 pin: The monitor output for Exposure period
TOUT1 pin: Programmable pulse
TOUT2 pin: Programmable pulse

(1) Exposure period control signal

This function is to output the actual exposure period control signal from the TOUT0 pin by setting the following registers.
This function can also be used in Fast trigger mode.

Register List of Pulse Output Function

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
TOUT0SEL [2:0]	06h	36h (3436h)	[2:0]	0h	TOUT0 pin setting 0h: Low fixed 1h: The monitor output for Exposure period

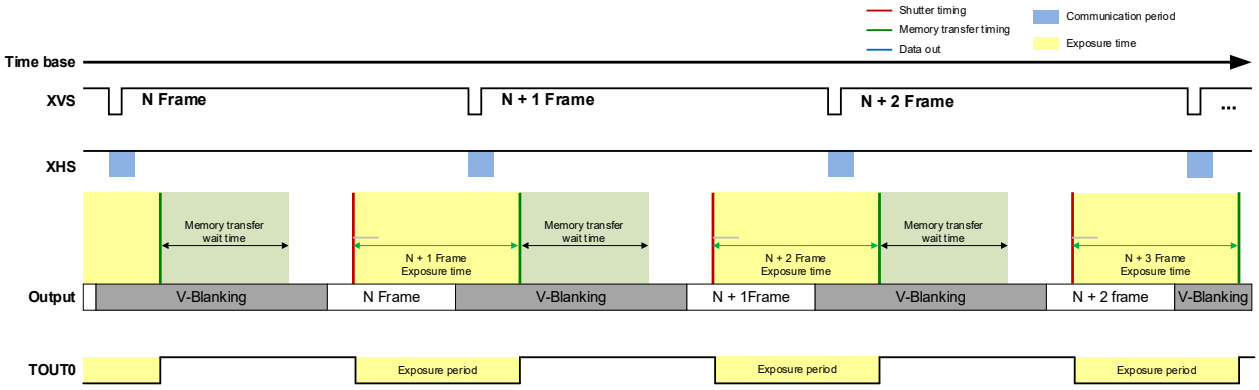


Image Drawing of the monitor output for Exposure period in Global Shutter (Normal Mode)

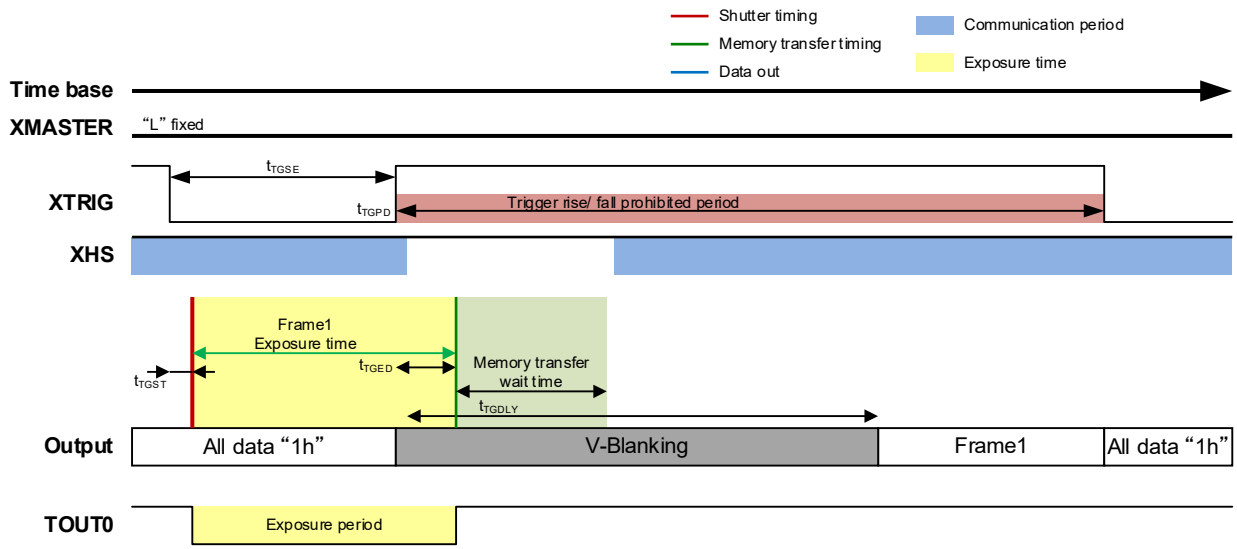


Image Drawing of the monitor output for Exposure period in Global Shutter (Fast Trigger Mode)

(2) Programmable Pulse signal

This function outputs programmable pulses from the TOUT1 and TOUT2 pins. The rise timing and fall timing of programmable pulse are set by registers, so user can generate the flexible pulses. For the reference point (The timing when register value set to 0) to be set, see the table “List of Reference point". The programmable pulse is output asynchronously with other signals on the basis of the sensor internal timing shown in the table “List of Reference point".
This function doesn't support Fast Trigger mode.

Register List of Pulse Output Function

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
TOUT1SEL [1:0]	06h	35h (3435h)	[1:0]	0h	TOUT1 pin setting 0h: Low fixed 3h: Pulse output
TOUT2SEL [1:0]			[3:2]	0h	TOUT2 pin setting 0h: Low fixed 3h: Pulse output
TRIG_TOUT1_SEL [3:0]		3Ah (343Ah)	[3:0]	0h	TOUT1 pin output selection 0h: Low fixed 1h: Pulse1 output
TRIG_TOUT2_SEL [3:0]			[7:4]	0h	TOUT2 pin output selection 0h: Low fixed 2h: Pulse2 output
PULSE1_EN_NOR [0]		78h (3478h)	[0]	0	Pulse1 enable in normal mode 0: disable 1: enable
PULSE1_EN_TRIG [0]			[1]	0	Pulse1 enable in trigger mode 0: disable 1: enable
PULSE1_POL [0]			[2]	0	Pulse1 polarity selection 0: High active 1: Low active
PULSE1_UP [23:0]		79h (3479h)	[7:0]	000000h	Pulse1 active period start timing setting Designated in line units from reference point
		7Ah (347Ah)	[7:0]		
		7Bh (347Bh)	[7:0]		
PULSE1_DN [23:0]		7Ch (347Ch)	[7:0]	000000h	Pulse1 active period end timing setting Designated in line units from reference point
		7Dh (347Dh)	[7:0]		
		7Eh (347Eh)	[7:0]		
PULSE2_EN_NOR [0]		80h (3480h)	[0]	0	Pulse2 enable in normal mode 0: disable 1: enable
PULSE2_EN_TRIG [0]			[1]	0	Pulse2 enable in trigger mode 0: disable 1: enable
PULSE2_POL [0]			[2]	0	Pulse2 polarity selection 0: High active 1: Low active
			[5]	0	Fixed to 1
PULSE2_UP [23:0]		81h (3481h)	[7:0]	000000h	Pulse2 active period start timing setting Designated in line units from reference point
		82h (3482h)	[7:0]		
		83h (3483h)	[7:0]		
PULSE2_DN [23:0]		84h (3484h)	[7:0]	000000h	Pulse2 active period end timing setting Designated in line units from reference point
		85h (3485h)	[7:0]		
		86h (3486h)	[7:0]		

List of Reference Point

	Normal mode	Trigger mode
Reference point of Pulse1	XVS fall edge in N frame	Fall edge of input trigger
Reference point of Pulse2	XVS fall edge in N +1 frame	Rise edge of input trigger

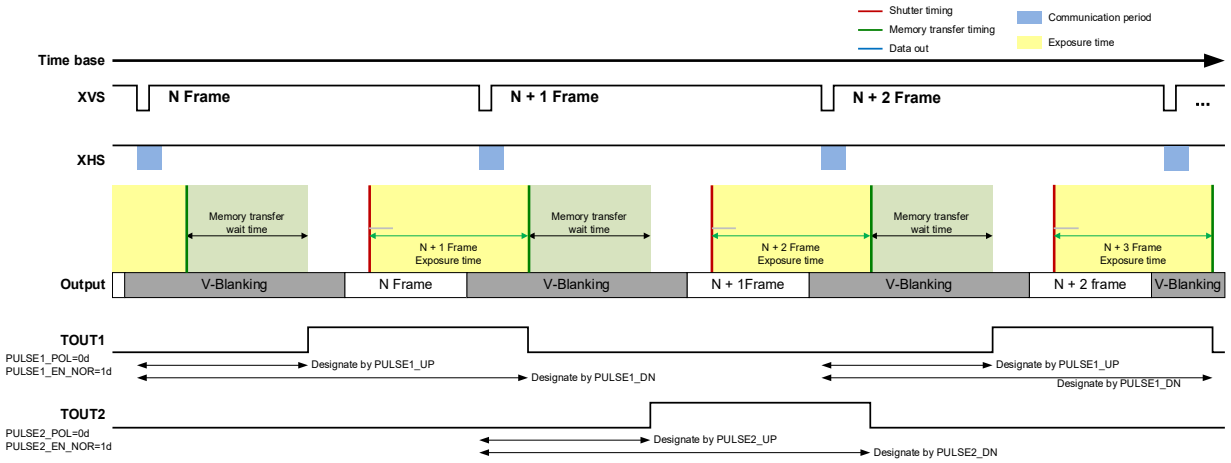


Image Drawing of Pulse Output Function in Global Shutter (Normal Mode)

In normal mode, TOUT1 and TOUT2 are output alternately each time inputting XVS.

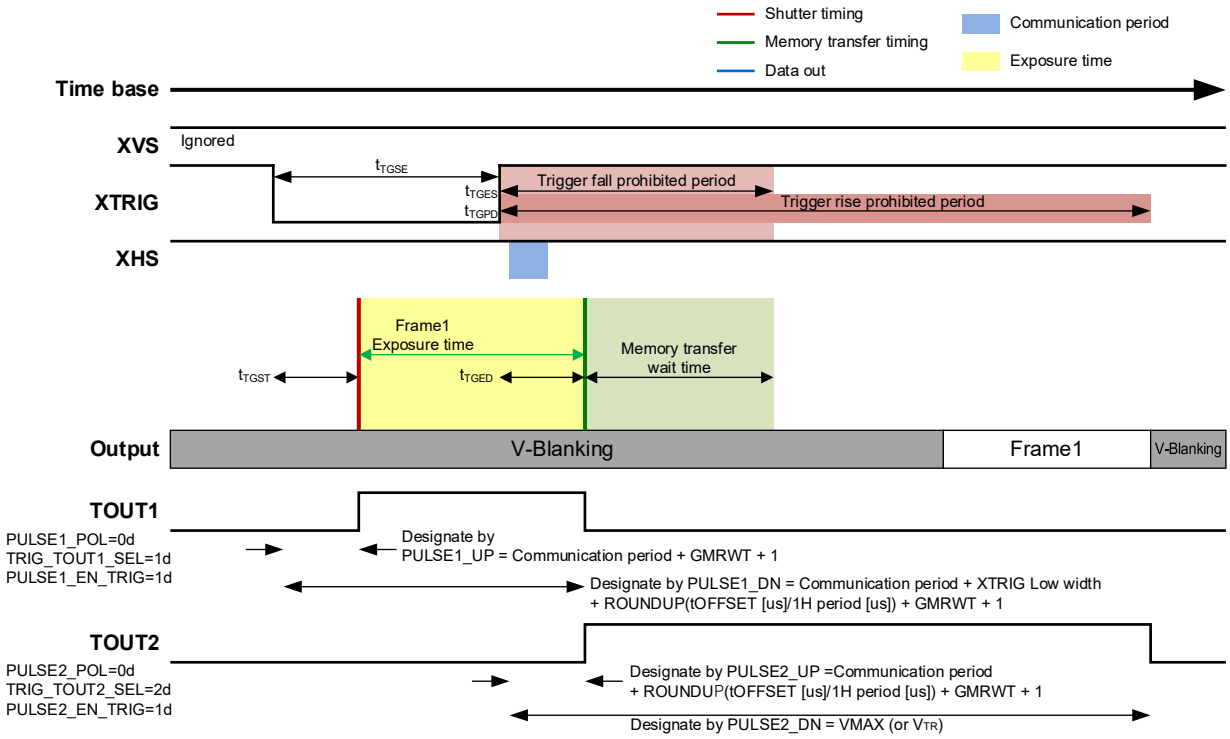


Image Drawing of Pulse Output Function in Global Shutter (Sequential Trigger Mode)

19.7. Signal Output

19.7.1. Output Pin Settings

The output formats of this sensor support the following modes.

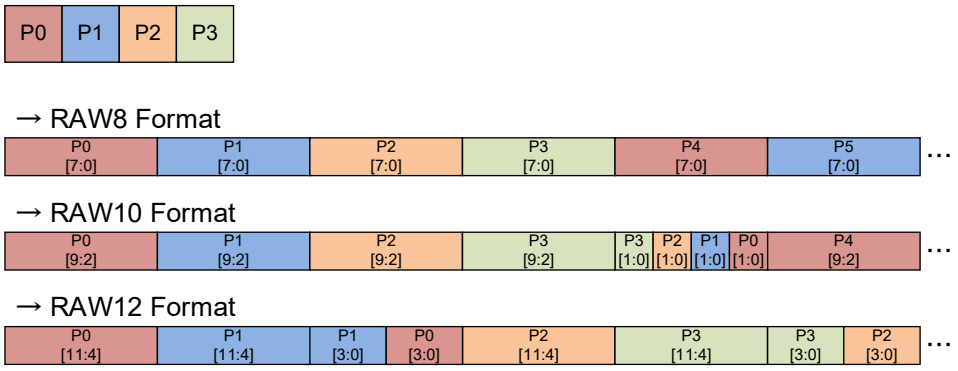
CSI-2 serial 2 Lane / 4 Lane, RAW8 / RAW10 / RAW12

The 2 Lane / 4 Lane serial signal output method using this sensor is described below.
Complied with the CSI-2, data is output using 2 Lane / 4 Lane. The image data is output from the CSI-2 output pin.
The DOP0 / DOM0 are called the Lane1 data signal, the DOP1 / DOM1 are called the Lane2 data signal, the DOP2 / DOM2 are called the Lane3 data signal, the DOP3 / DOM3 are called the Lane4 data signal. In addition, the clock signals are output from DCKP / DCKM of the CSI-2 pins.
In 2 Lane mode, data is output from Lane1 and Lane2. In 4 Lane mode, data is output from Lane1, Lane2, Lane3 and Lane4.
The value of maximum data rate is 1188 Mbps/Lane.
The select of RAW8, RAW10 or RAW12 is set by the register: ODBIT [1:0]. The number of output lanes is set by the register: LANESEL [2:0].
Unused lanes output signals conformed to MIPI standard.

Register List of Output Settings

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
ODBIT [1:0]	06h	30h (3430h)	[1:0]	0h	0h: 10 bit 1h: 12 bit 2h: 8 bit
LANESEL [2:0]	0Bh	04h (3904h)	[2:0]	0h	CSI-2 IF Output Lane selection 2h: 4 Lane 3h: 2 Lane

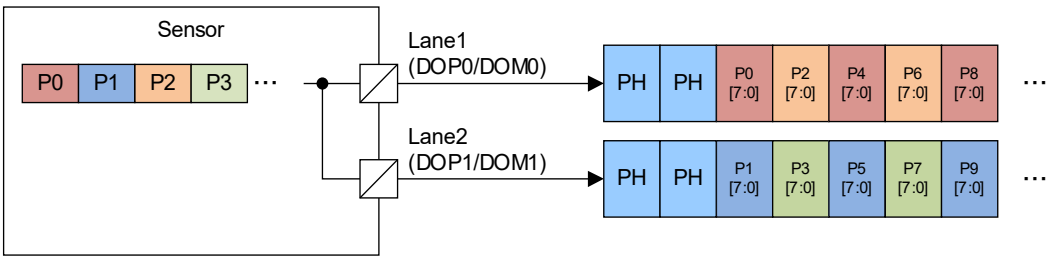
The formats of RAW8, RAW10 and RAW12 are shown below.



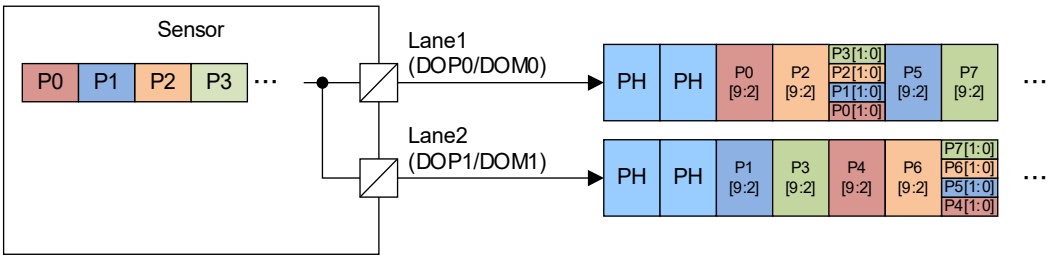
The Example of Format of RAW8 / RAW10 / RAW12

The each formal of 2 Lane and 4 Lane are shown below.

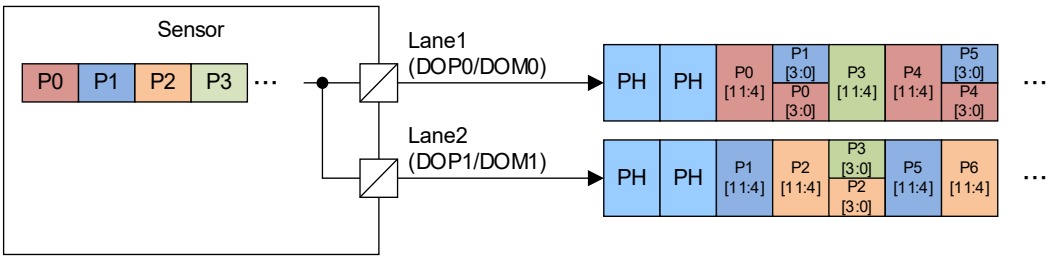
a) 2 Lane-RAW8



b) 2 Lane-RAW10

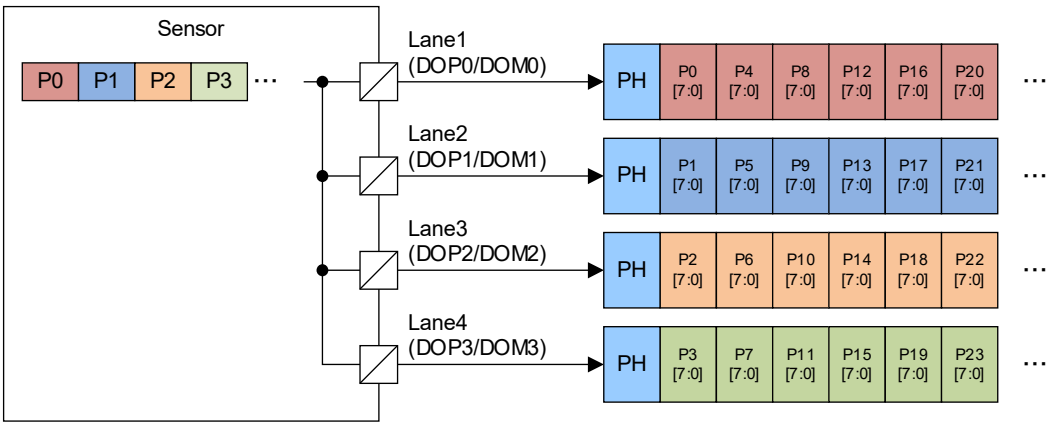


C) 2 Lane-RAW12

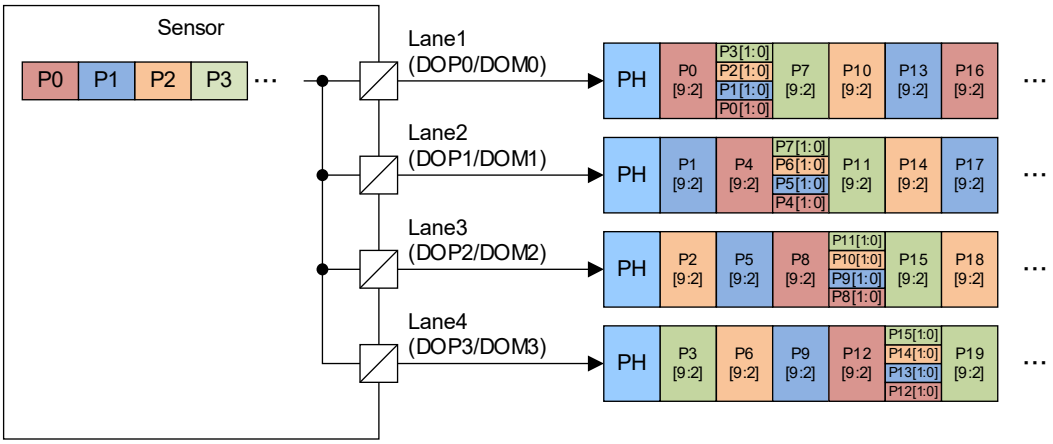


2 Lane Output Format

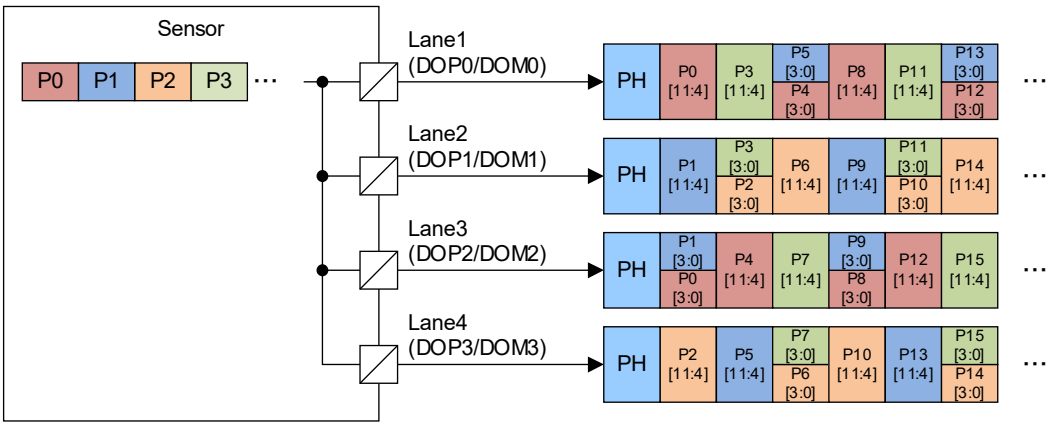
d) 4 Lane-RAW8



e) 4 Lane-RAW10



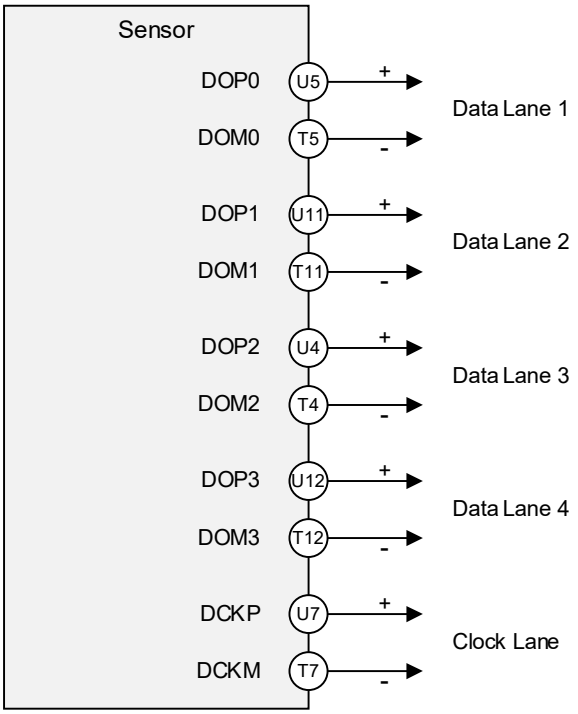
f) 4 Lane-RAW12



4 Lane Output Format

19.7.2. MIPI Transmitter

Output pins (DOP0, DOM0, DOP1, DOM1, DOP2, DOM2, DOP3, DOM3, DCKP, DCKM) are described in this section.

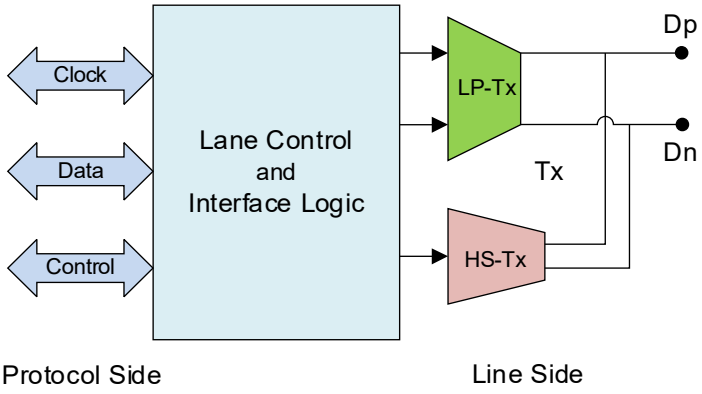


Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.
See the MIPI Standard

- MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2) Version 1.2
- MIPI Alliance Specification for D-PHY Version 1.2

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, as close as possible to the Receiver. The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The maximum bit rate of each Lane is 1188 Mbps/Lane.



19.7.3. Output Pin Bit Width Selection

The number of internal A/D conversion bits can be selected from 8 bit, 10 bit or 12 bit by the register ADBIT [1:0]. See the section of “Readout Drive Modes” for the correspondence with each mode.

Register List of Bit Width Selection

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ) : I^2C	bit			
ADBIT [1:0]	04h	00h (3200h)	[5:4]	0h	0h: 10 bit 1h: 12 bit 2h: 8 bit	Set same value to both ADBIT and ODBIT

19.7.4. Output Signal Range

In CSI-2 output mode, the sensor output has either a 8 bit, 10 bit or 12 bit gradation, and the maximum output value is the FFh (8 bit output), 3FFh value (10 bit output) and the FFFh one (12 bit output).
The output range for each output gradation is shown in the table below.

Output Gradation and Output Range

Output gradation	Output value	
	Min.	Max.
8 bit	00h	FFh
10 bit	000h	3FFh
12 bit	000h	FFFh

19.8. Global Timing Register Setting

The setting values of the Global Timing register are shown below.

Global Timing Register Setting

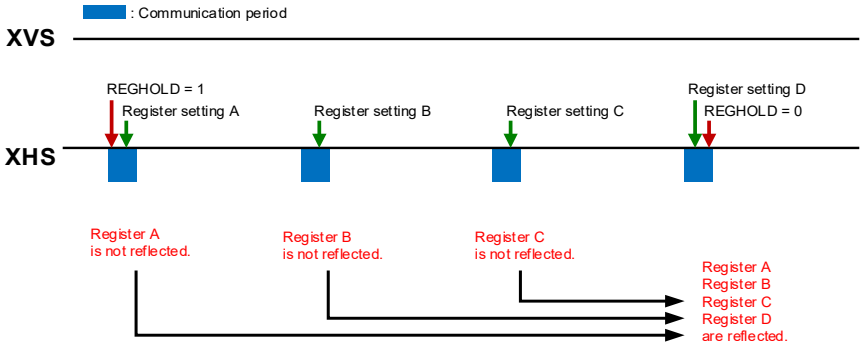
Register	Register details			Initial value	Setting value		
	Chip ID	Address ( ): I²C	bit		1188 Mbps	891 Mbps	594 Mbps
THS_PREPARE [15:0]	0Eh	B4h (3CB4h)	[7:0]	004Fh	004Fh	003Fh	002Fh
		B5h (3CB5h)	[7:0]				
TCLK_POST [15:0]		B6h (3CB6h)	[7:0]	008Fh	008Fh	007Fh	0067h
		B7h (3CB7h)	[7:0]				
THS_TRAIL [15:0]		B8h (3CB8h)	[7:0]	004Fh	004Fh	003Fh	002Fh
		B9h (3CB9h)	[7:0]				
THS_ZERO [15:0]		BAh (3CBAh)	[7:0]	0087h	0087h	006Fh	004Fh
		BBh (3CBBh)	[7:0]				
TCLK_PREPARE [15:0]		BCh (3CBCh)	[7:0]	004Fh	004Fh	0037h	0027h
		BDh (3CBDh)	[7:0]				
TCLK_TRAIL [15:0]		BEh (3CBEh)	[7:0]	0047h	0047h	0037h	0027h
		BFh (3CBFh)	[7:0]				
TLPX [15:0]		C0h (3CC0h)	[7:0]	003Fh	003Fh	002Fh	0027h
		C1h (3CC1h)	[7:0]				
TCLK_ZERO [15:0]		C2h (3CC2h)	[7:0]	0137h	0137h	00F7h	00B7h
		C3h (3CC3h)	[7:0]				
TCLK_PRE [15:0]		C4h (3CC4h)	[7:0]	000Fh	000Fh	000Fh	000Fh
		C5h (3CC5h)	[7:0]				
THS_EXIT [15:0]		C6h (3CC6h)	[7:0]	007Fh	007Fh	005Fh	0047h
		C7h (3CC7h)	[7:0]				

19.9. Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD. Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register.

Register List of Register Hold

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
REGHOLD [0]	02h	34h (3034h)	[0]	0	0: Invalid 1: Valid (Register hold)



Register Hold Setting

19.10. Mode Transition

The Mode transition between operations is shown below. These examples shown in case that setting is completed within one communication timing.

List of Mode Transition

Transition			State
Operation mode			
Normal mode (Sensor Slave mode)	→	Sequential Trigger mode	Via the standby state is unnecessary Invalid frame: 1
Sequential Trigger mode	→	Normal mode (Sensor Slave mode)	
Normal mode (Sensor Master mode)	→	Fast Trigger mode	Via the standby state is necessary
Fast Trigger mode	→	Normal mode (Sensor Master mode)	
Readout mode (Normal mode or Sequential Trigger mode)			
All-pixel	→	ROI	Via the standby state is unnecessary Invalid frame: 0
ROI	→	All-pixel	
ROI	→	ROI	
Readout mode (Fast Trigger mode)			
All-pixel	→	ROI	Via the standby state is necessary
ROI	→	All-pixel	
ROI	→	ROI	
- Transition between modes other than the above - Change the input frequency of INCK[*1] - Change the register setting noted “S” in the reflection timing column of the Register Map			Via the standby state is necessary

[*1] When changing input INCK frequency, care should be taken not to be input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

19.11. Other Function

This sensor has the function as below. About detail, refer to each application note.

- Multi Frame Set Output mode (2 / 4 frame)
- Multi Exposure Trigger mode
- Multi Frame ROI (Multi Exposure + ROI) mode
- Low Power Consumption (Low power consumption function is always ON)
- Thermometer
- Gradation Compression
- Dual Trigger
- Self Trigger
- Short Interval Shutter function
- Tracking ROI
- Pattern Generator (Refer to Support Package)

19.12. Extension Function

Use these functions after enough checks and evaluation.

- Black Level Auto Adjust Off
- Short Exposure Mode

20. Power-on and Power-off Sequence

20.1. Power-on sequence

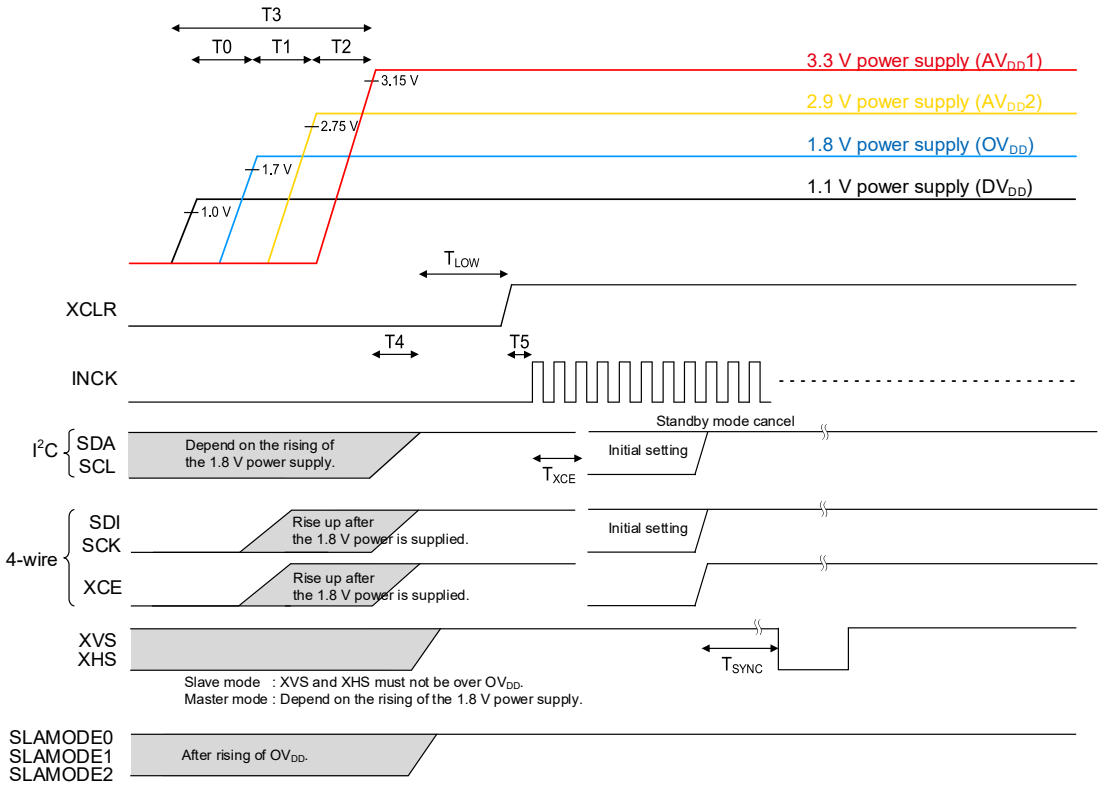
Follow the sequence below to turn on the power supplies.

(1) Turn on the power supplies so that the power supplies rise in order of 1.1 V power supply (DV_{DD}) →1.8 V power supply (OV_{DD}) → 2.9 V power supply ($AV_{DD}2$) → 3.3 V power supply ($AV_{DD}1$). In addition, all power supplies should finish rising within 200 ms. Each digital input terminal (INCK, XCE, SCK, SDI, XCLR, XMASTER, XTRIG1, XTRIG2, SLAMODE0, SLAMODE1, SLAMODE2 and XVS, XHS) set 0V or Hi – Z.

(2) The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}), so hold XCE at High level until INCK is input.

(3) Start the input of INCK after turning the level of XCLR into the high.

(4) Make the sensor setting by register communication after stabilizing the master clock (INCK).

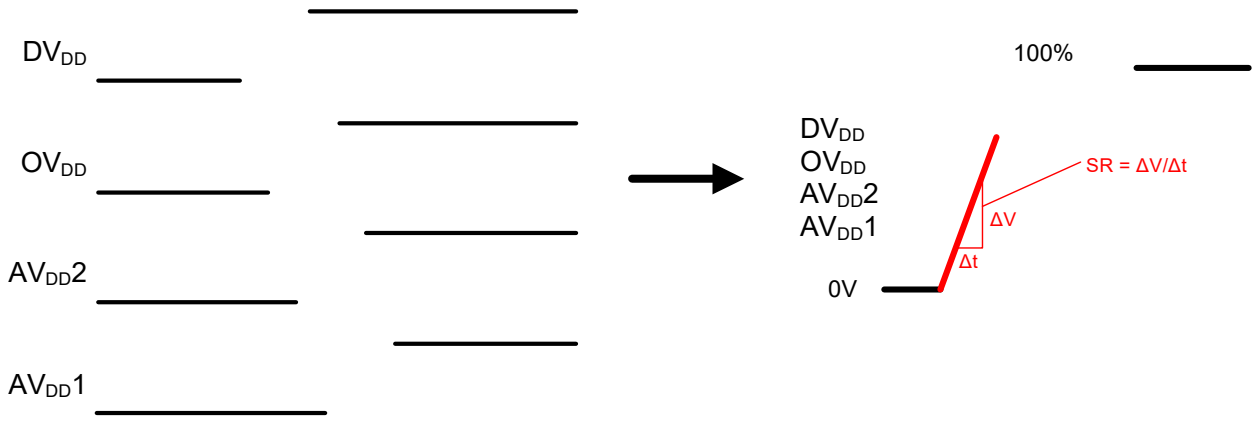


Power-on Sequence

Item	Symbol	Min.	Max.	Unit
1.1 V power supply rising to 1.8 V power supply rising	T0	0	–	ms
1.8 V power supply rising to 2.9 V power supply rising	T1	0	–	ms
2.9 V power supply rising to 3.3 V power supply rising	T2	0	–	ms
Rising time of all power supplies	T3	–	200	ms
All power supplies rising to XCE High	T4	0	–	ms
XCE High to Clear OFF	T_{LOW}	0.5	–	µs
Clear OFF to INCK rising	T5	1	–	µs
INCK rising to Communication start	T_{XCE}	20	–	µs
Standby OFF (communication) to External input XHS, XVS (slave mode only)	T_{SYNC}	6.8	–	ms

20.2. Slew Rate Limitation of Power-on Sequence

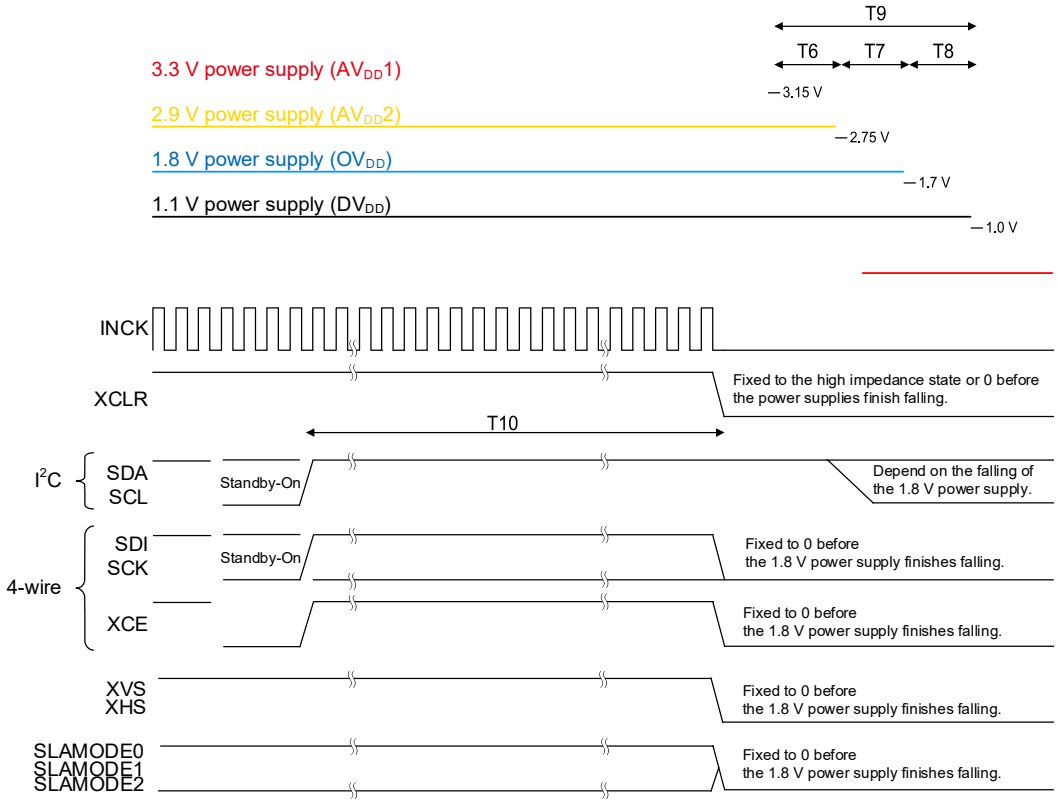
Conform the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	DV_{DD} (1.1 V)	—	25	mV/μs	
		OV_{DD} (1.8 V)	—	25	mV/μs	
		$AV_{DD}2$ (2.9 V)	—	25	mV/μs	
		$AV_{DD}1$ (3.3 V)	—	25	mV/μs	

20.3. Power-off Sequence

Turn off the power supplies so that the power supplies fall in order of 3.3 V power supply ($AV_{DD}1$) → 2.9 V power supply ($AV_{DD}2$) → 1.8 V power supply (OV_{DD}) → 1.1 V power supply (DV_{DD}). In addition, all power supplies should finish falling within 200 ms.
Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, XTRIG1, XTRIG2, SLAMODE0, SLAMODE1, SLAMODE2, XVS, XHS) to 0 V or high impedance before the 1.8 V power supply (OV_{DD}) falls.



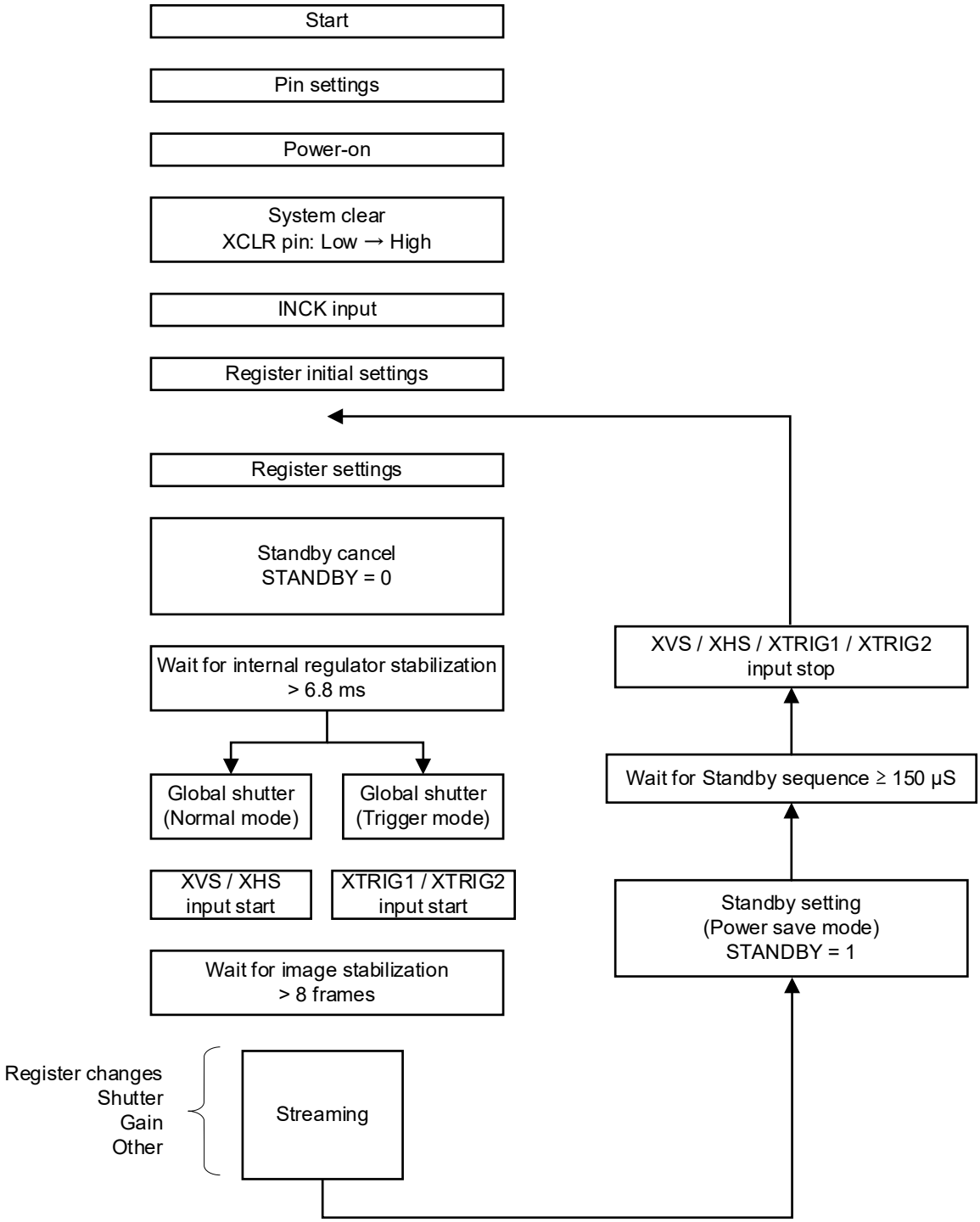
Power-off Sequence

Item	Symbol	Min.	Max.	Unit
3.3 V power supply fall to 2.9 V power supply fall	T6	0	–	ms
2.9 V power supply fall to 1.8 V power supply fall	T7	0	–	ms
1.8 V power supply fall to 1.1 V power supply fall	T8	0	–	ms
Fall time of all power supplies	T9	–	200	ms
“Standby-On” to “Set 0 V or Hi-z each digital input pin”	T10	150	–	µs

21. Sensor Setting Flow

21.1. Setting Flow in Sensor Slave Mode

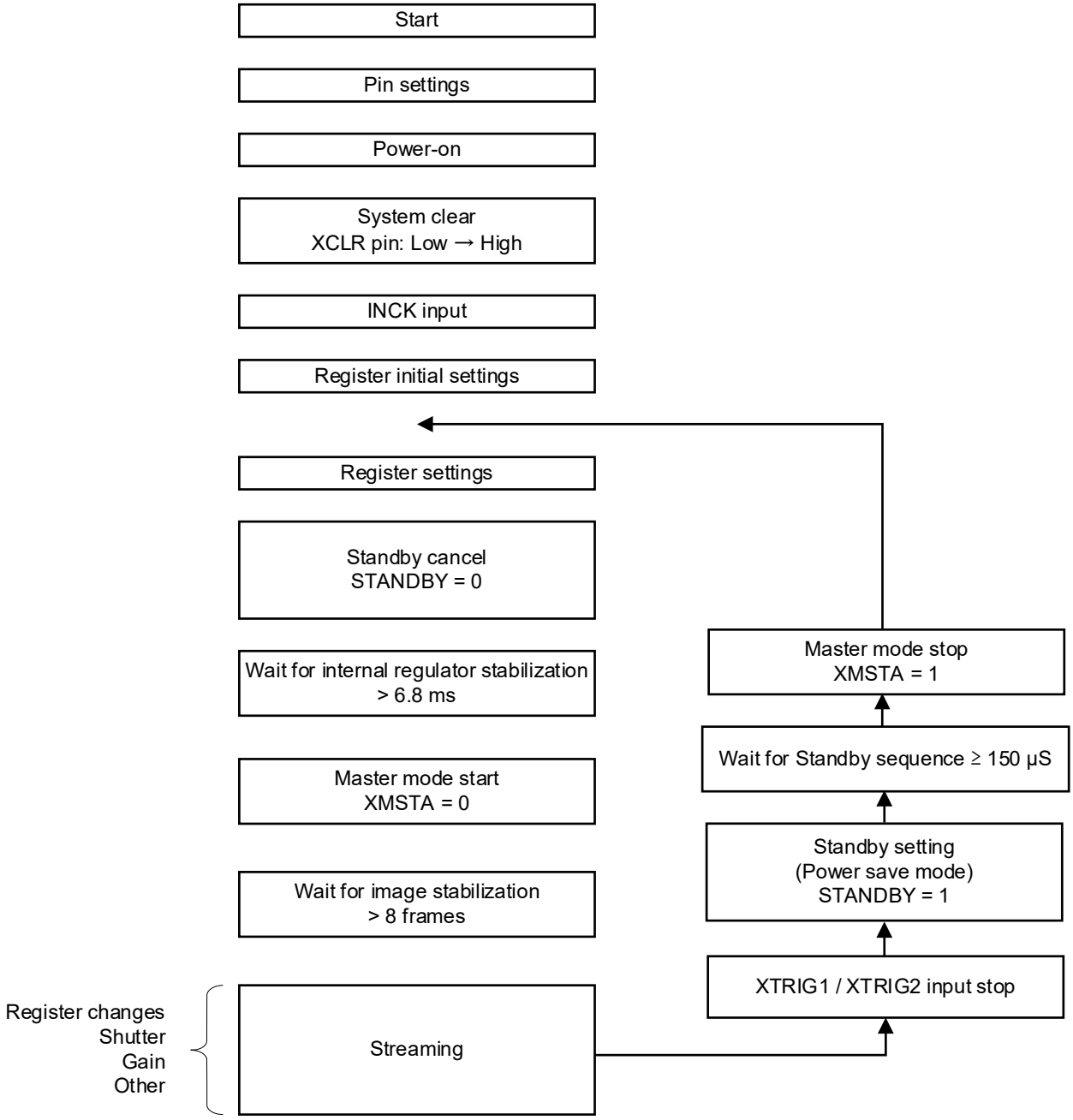
The figure below shows the operation flow in sensor slave mode.
For details from “Power-on” to “System clear”, see section “Power-on sequence”. For details from “Standby cancel” to “Wait for image stabilization”, see section “Standby mode”. “Standby setting (Power save mode)” can be made by setting the STANDBY register to “1” during “Streaming”.



Sensor Setting Flow (Sensor Slave Mode)

21.2. Setting Flow in Sensor Master Mode

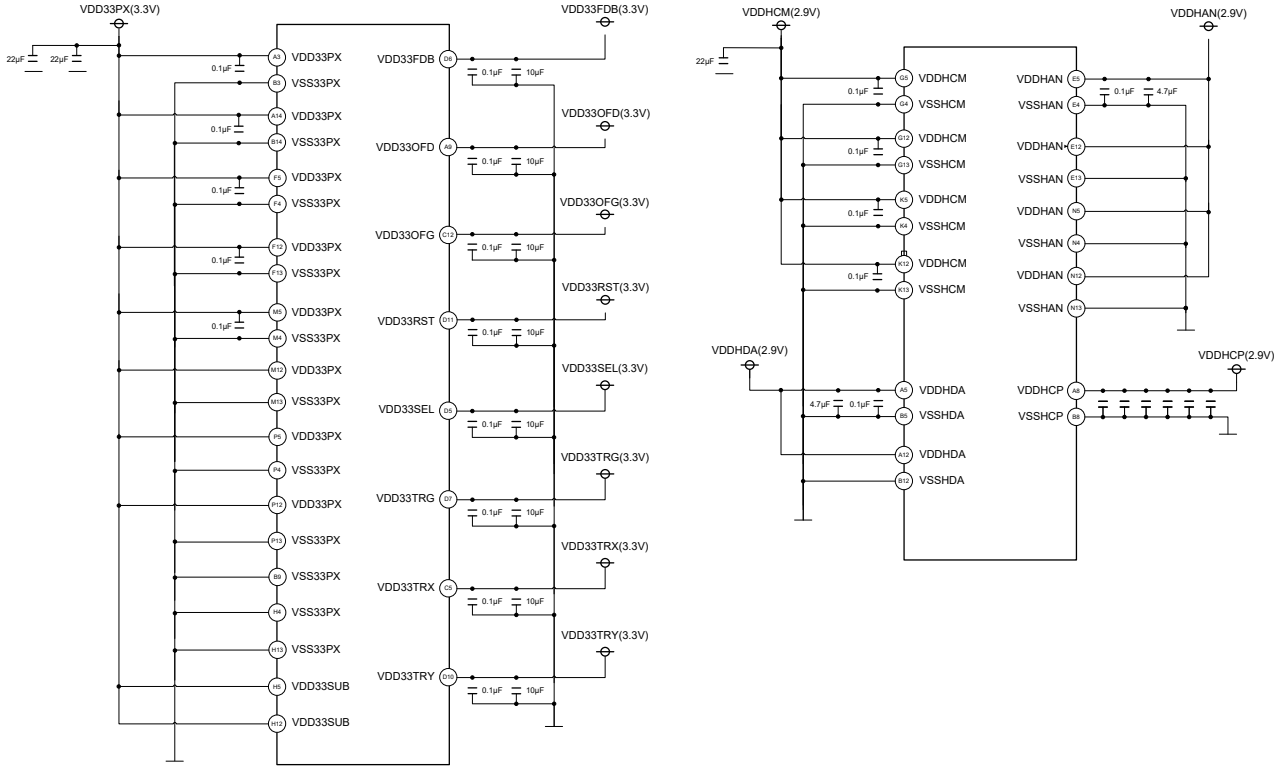
The figure below shows the operation flow in sensor master mode.
For details from “Power-on” to “System clear”, see section “Power-on sequence”. For details from “Standby cancel” to “Wait for image stabilization”, see section “Standby mode”. In master mode, “Master mode start” by setting the master mode start register XMSTA to “0” after “Wait for internal regulator stabilization”.
“Standby setting (Power save mode)” can be made by setting the STANDBY register to “1” during “Streaming”. At this time, set “Master mode stop” by setting XMSTA to “1”.



Sensor Setting Flow (Sensor Master Mode)

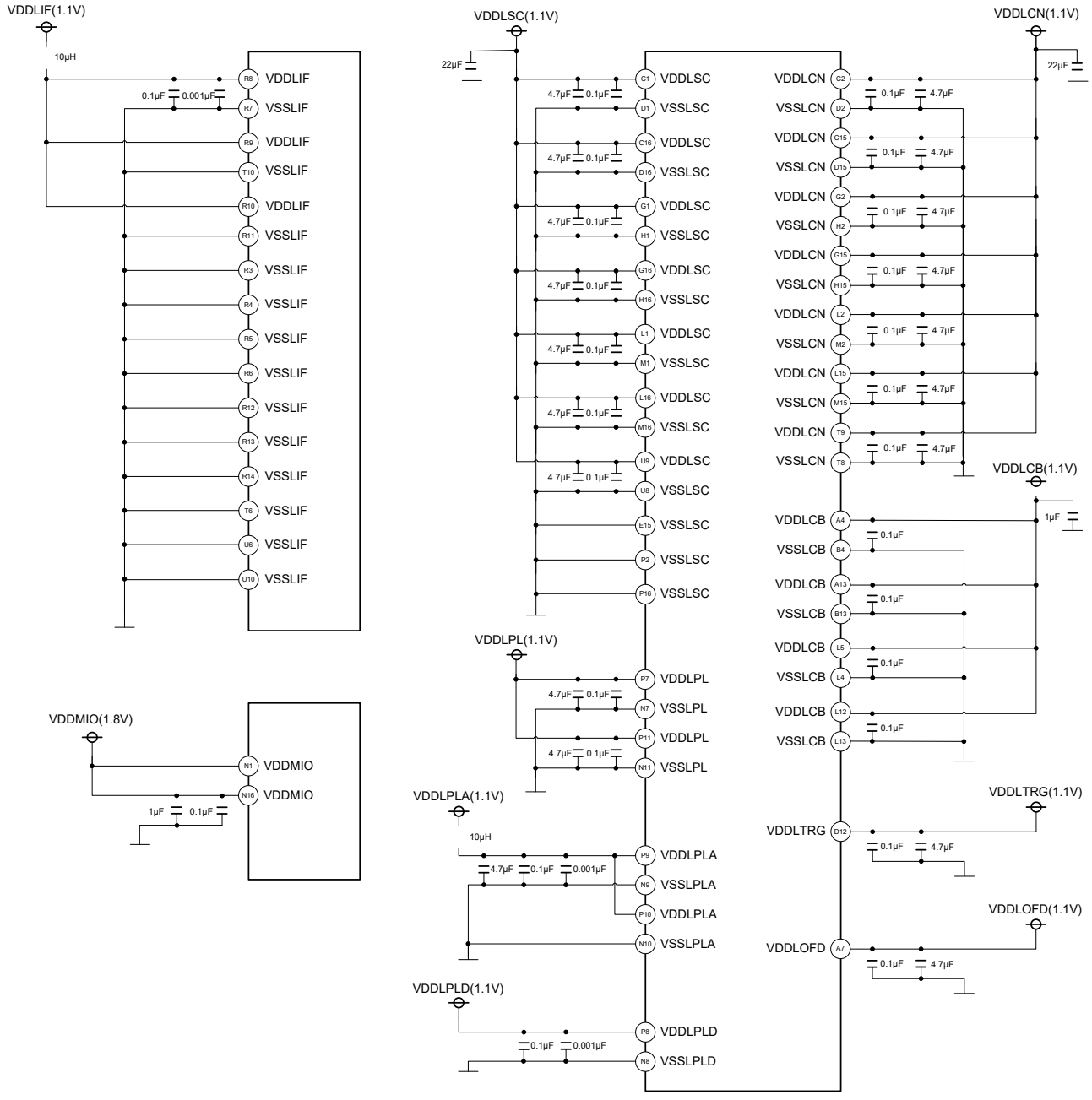
22. Peripheral Circuit

22.1. Analog Power Pins



Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

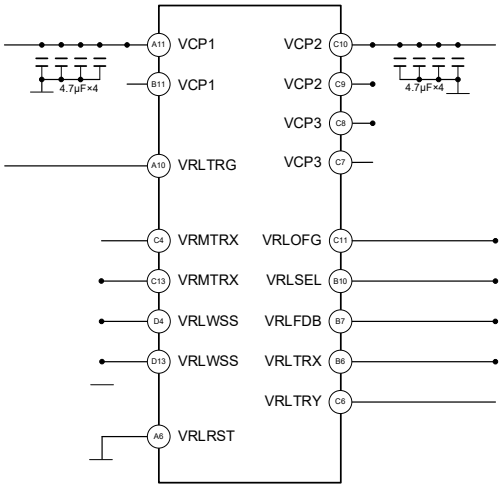
22.2. Digital Power Pins



Pin A4, A13, L5, L12, A7 and D12 are analog power pins. But these pins can be connected to the digital power pins. So, it describes on this page. These pins can be separated from the digital power pins.

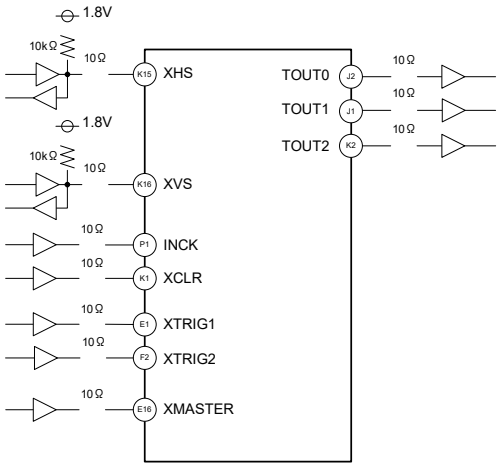
Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

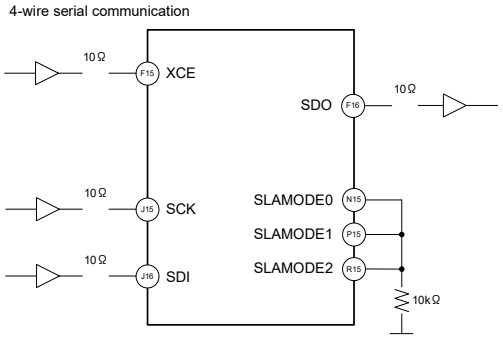
22.3. Analog Other Pins

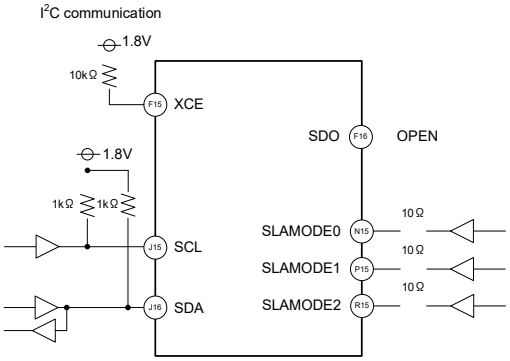


Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

22.4. Digital I/O Pins

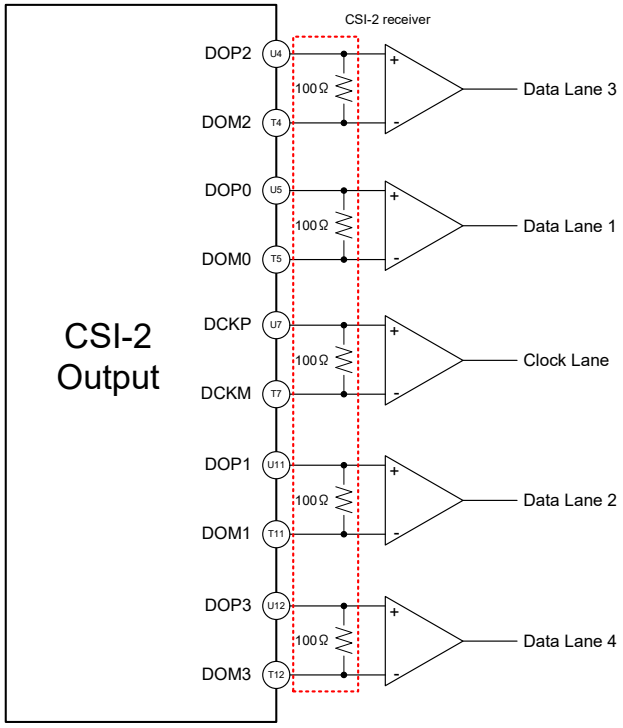






Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

22.5. Output pins



The MIPI IF terminating resistor is not used in LP mode. (Required in HS mode)
Therefore, control the terminating resistor on the receiving side.

Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

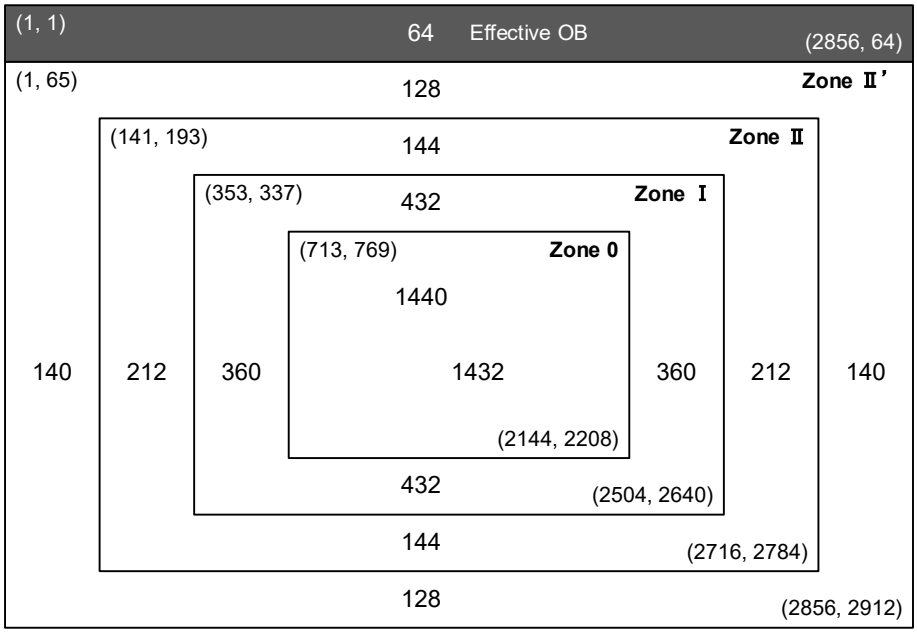
23. Spot Pixel Specifications

($A_{VDD}1$ = 3.3 V, $A_{VDD}2$ = 2.9 V, O_{VDD} = 1.8 V, D_{VDD} = 1.2 V, Tj = 60 ˚C, 30 frame/s, Gain: 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone			Measurement method	Remarks
		0 to II'	Effective OB	Ineffective OB		
Black and white pixels at high light	30 % ≤ D	58	No evaluation criteria applied		1	
White pixels in the dark	5.6 mV ≤ D	1446		No evaluation criteria applied	2	1/30 s storage
Black pixels at signal saturated	D ≤ 598 mV	0	No evaluation criteria applied		3	

Note) 1. Zone is specified based on all-pixel drive mode
2. D…Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

23.1. Spot Pixel Zone Definition



24. Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, particle radiation such as cosmic rays etc. may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	3 pcs
10.0 mV or higher	2 pcs
24.0 mV or higher	1 pcs
50.0 mV or higher	1 pcs
72.0 mV or higher	1 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

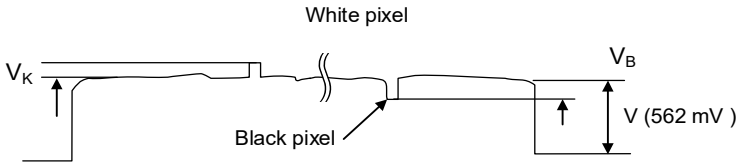
Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

25. Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

(1) Black or white pixels at high light
After adjusting the luminous intensity so that the average value V of the signal outputs is 562 mV, measure the local dip point (black pixel at high light, V_B) and peak point (white pixel at high light, V_K) in the signal output V, and substitute the value into the following formula.

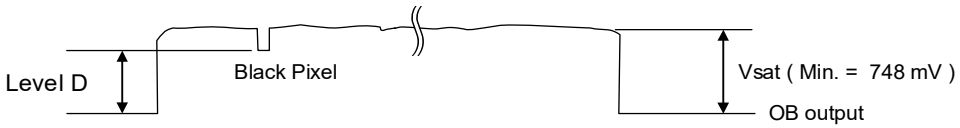
Spot pixel level D = ((V_B or V_K) / Average value of V) × 100 [%]



Signal output waveform

(2) White pixels in the dark
Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

(3) Black pixels at signal saturated
Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

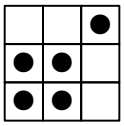
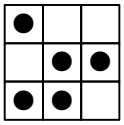
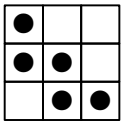
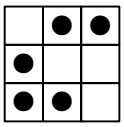


Signal output waveform

26. Spot Pixel Pattern Specification

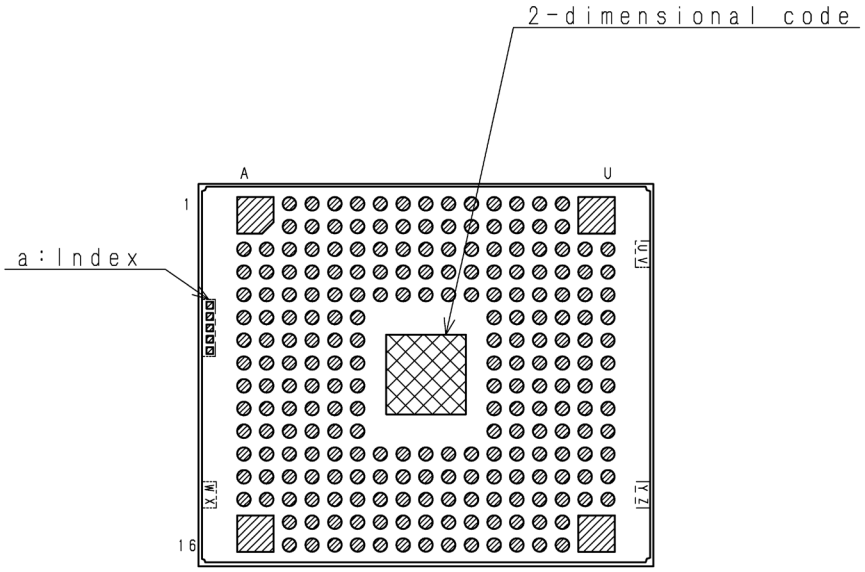
White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.

Pixel patterns with 5 or more spot pixels occurring in the 3 × 3 pixels area

No.	Pattern	White pixel Black pixel Bright pixel
1		Rejected
2		Rejected
3		Rejected
4		Rejected

Note) 1. “● ” shows the position of white pixel, black pixel and bright pixel.
2. When 12 or more spot pixels indicated “Rejected” is selected and removed.
3. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

27. Marking



Note : One character of alphabet or number shall be placed from U to Z part.
(Plating option)

As for part "a", up to 5 indexes are arranged.
(Plating option)

DRAWING No. AM-B566AAMJ(2D)

28. Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

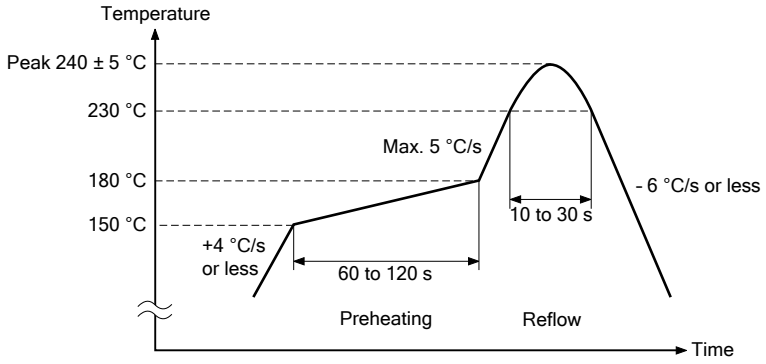
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Recommended temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.

(b) Perform the reflow soldering only one time.

(c) Finish reflow soldering within 72 h after unsealing the degassed packing. Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.

(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(e) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the conditions mentioned above.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After the reflow, the paste residue of protective tape may remain around the seal glass. (The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

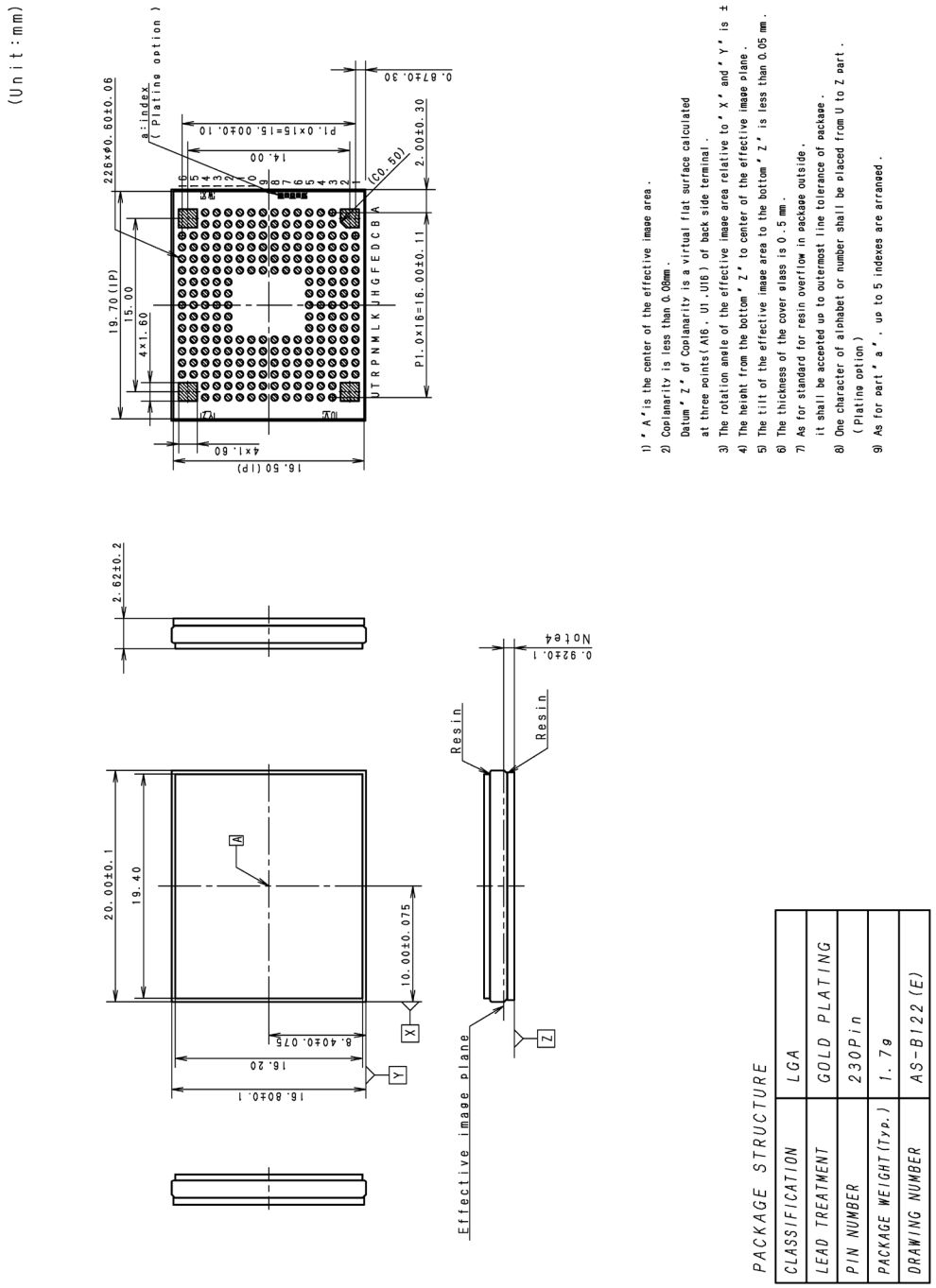
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Material_No.14-0.0.9

29. Package Outline

(Unit: mm)



1) "A" is the center of the effective image area.
2) Coplanarity is less than 0.08mm.
   Datum "Z" of Coplanarity is a virtual flat surface calculated
   at three points(A16. U1. U16) of back side terminal.
3) The rotation angle of the effective image area relative to "X" and "Y" is ±0.5°.
4) The height from the bottom "Z" to center of the effective image plane.
5) The tilt of the effective image area to the bottom "Z" is less than 0.05mm.
6) The thickness of the cover glass is 0.5mm.
7) As for standard for resin overflow in package outside,
   it shall be accepted up to outermost line tolerance of package.
8) One character of alphabet or number shall be placed from U to Z part.
   (Plating option)
9) As for part "a", up to 5 indexes are arranged.

PACKAGE STRUCTURE

CLASSIFICATION	LGA
LEAD TREATMENT	GOLD PLATING
PIN NUMBER	230Pin
PACKAGE WEIGHT(Typ.)	1.7g
DRAWING NUMBER	AS-B122(E)

30. List of Trademark Logos and Definition Statements

Pregius S

* Pregius S is a registered trademark or trademark of Sony Group Corporation or its affiliates. Pregius S is a global shutter sensor technology for active pixel-type CMOS image sensors. By stacking the signal processing on the back illuminated type CMOS Image Sensor it realizes small chip size and high sensitivity, whilst using the high picture quality global shutter pixel technology of Pregius.

SONY

Revision History

Date of change	Ver.	Page	Contain of Change
2020/5/11	0.1	—	First Edition
2020/11/13	0.2	1	Delete: “Recommended exit pupil distance”
		19	Update the figure of System Clear (XCLR)
		22	Update the figure of Serial Communication 4-wire
		26 28	Update the unit of sensitivity
		27	Update Standard imaging condition I, II, III
		28	Update description of Sensitivity
		57	Delete HADD_ON_SEL register Correction: reflection timing of Chip-ID=04h, Address=00h, bit [0]
		76 to 78	Correction: note 1 in the table
		79	Update the Image Drawing of Sutter stabilization wait time inserted Delete the description of the table reference
		84 91 99 102	Correction: the setting of address 24h and 26h to 27h.
		92 97	Correction: the description of FINFO_HWIDTH register
		111	Correction: setting value of SHS register
		114 116	Correction: the I^2C address of XMSTA register
		115	Update the Image Drawing of Interrupt Operation
		116	Correction: the Calculation Formula of Exposure Time
		118	Update the Image Drawing of Transition from Normal Mode to Sequential Trigger Mode Update the Image Drawing of Transition from Sequential Trigger Mode to Normal Mode
		121	Update the Image Drawing of Pulse Output Function in Global Shutter (Sequential Trigger Mode)
		129	Correction: Readout mode (Fast Trigger mode) in the table
		131	Update the Image Drawing of Power-on Sequence Correction: “all powe supply” to “all power supplies”
		133	Update the Image Drawing of Power-off Sequence Correction: the table for Power-off Sequence
		144	Correction: the list of White Pixel, Black Pixel and Bright Pixel Pattern
2020/12/25	E20Z08	-	Update Official version
		1	Delete “Tentative”
		3	Update the Absolute Maximum Ratings
		8	Update Chip Center and Optical Center
		17	Update the Power Consumption
		25	Update the Spectral Sensitivity Characteristics
		26	Update the Image Sensor Characteristics
		28	Update the Measurement Method for Sensitivity
		73	Update Description of Chip-ID=0Eh, Address=C5h
		79	Update the Image Drawing of Sutter stabilization wait time inserted

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Date of change	Ver.	Page	Contain of Change
2020/12/25	E20Z08	80	Update Frame Structure of CSI-2 output
		81	Update the Image Drawing of Embedded Data Format
		82	Update table
		85	Update Pixel Array Image Drawing in All-pixel scan Mode (CSI-2 output Shutter stabilization wait time is not included)
		100	Update Pixel Array Image Drawing in Vertical / Horizontal 1/2 subsampling mode (CSI-2 output Shutter stabilization wait time is not included)
		102	Correction: “Glbl Timing Registers” to “Global Timing Registers”
		103	Update Pixel Array Image Drawing in 2x2 FD binning mode (CSI-2 output Shutter stabilization wait time is not included)
		111, 114, 116	Update Calculation Formula of the Exposure time
		112	Update list of Exposure setting
		114	Update Parameter List of Global Shutter (Sequential Trigger Mode)
		116	Update Parameter List of Global Shutter (Fast Trigger Mode)
		141	Update the Spot Pixel Specification and Spot Pixel Zone
		142	Update the Annual number of occurrences
		143	Update the Measurement Method for Spot Pixels
		145	Update the Marking
		146	Update the Package Outline
2021/2/25	E20Z08A12	3	Update table of the Absolute Maximum Ratings Add "Do not exceed 4.65V" to remarks of the input voltage, the output voltage
		11	Update the Image Drawing of Pin Configuration
		28	Correction calculating formula of PLS (“10/33.3” to “1/3000”)
		81	Update the Image Drawing of Embedded Data Format
		82	Update table
		111, 112, 114	Correction value of t_{OFFSET} (“2.47 [µs]” to “2.7 [µs]”)
		112	Update the list of Exposure Setting
		114	Update Parameter List of Global Shutter (Sequential Trigger Mode)
		116	Correction value of t_{OFFSET} (“2.53 [µs]” to “2.7 [µs]”) Update Parameter List of Global Shutter (Fast Trigger Mode)
		122	Update the Image Drawing of “The Example of Format of RAW8 / RAW10 / RAW12”
		125	Correction the MIPI standard name (“Specification” to “Standard”)
		130	Update chapter "Other Functions"
		131	Correction minimum value of INCK rising to Communication start (T_{XCE}) (“20 [µs]” to “20 [ms]”)
		133	Update the figure of Power-off Sequence Update the table
		137	Update the Image Drawing of Digital Power Pins
2021/10/29	E20Z08B1X	80, 82, 83	Addition: Embedded data (2nd to 4th lines)

SONY

Date of change	Ver.	Page	Contain of Change
2021/10/29	E20Z08B1X	82	Correction: "4300h [2:0]"→"3400h [2:0]"
		141	Addition: note about terminating resistors in peripheral circuits of MIPI IF
2022/7/12	E20Z08C27	150	Correction: Description statements of trademark logo
2022/12/15	E20Z08D2Z	105, 132, 135, 136	Update: The sensor startup time 1138 ms or more → 6.8 ms or more