



GC2093 CSP

1/2.9''2Mega CMOS Image Sensor

Datasheet

Beta 0.3

2020-02-21

Ordering Information

◆ GC2093

(Colored, 47PIN-CSP)

GENERATION REVISION HISTORY

REV.	EFFECTIVEDATE	DESCRIPTION OFCHANGES	PREPARED BY
Beta 0.1	2019-12-27	Beta Document Release	DSC-AE Dept.
Beta 0.2	2019-12-31	fix register	DSC-AE Dept.
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1. Sensor Overview

1.1 General Description

GC2093 is a high quality 1080P CMOS image sensor, for security camera products, digital camera products and mobile phone camera applications. GC2093 incorporates a 1920H x 1080V pixel array, on-chip 10-bit ADC, and image signal processor.

The full scale integration of high-performance and low-power functions makes the GC2093 best fit the design, reduce implementation process, and extend the battery life of Motion Camera, Car DVR, and a wide variety of mobile applications.

It provides RAW10 and RAW8 data formats with MIPI and DVP interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

Additionally, it has HDR function by staggered output mode, letting user use 2 different exposure time frames combine one picture to improve dynamic range and avoid smearing.

1.2 Features

- ◆ Standard optical format of 1/2.9 inch
- ◆ 2.8μm*2.8μm
- ◆ Output formats: Raw Bayer 10bit/8bit
- ◆ Power supply requirement: AVDD28: 2.7~2.9V(Typ.2.8V)
DVDD18: 1.15~1.3V (Typ.1.2V)
IOVDD: 1.7~2.8V (Typ.1.8V)
- ◆ PLL support
- ◆ Support frame sync
- ◆ DVP /MIPI (2lane) interface support
- ◆ Horizontal/Vertical mirror

- ◆ Image processing module
- ◆ HDR function
- ◆ OTP support(1K bits):
- ◆ Package: CSP

1.3 Application

- ◆ Security cameras
- ◆ Automotive
- ◆ Cellular Phone Cameras
- ◆ Digital still cameras and camcorders
- ◆ Video telephony and conferencing equipment

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/2.9inch
Pixel Size	2.8 μ m $\times$ 2.8 μ m
Active pixel array	1920 $\times$ 1080
Shutter type	Electronic rolling shutter
ADC resolution	10 bit ADC
Max Frame rate	60fps@full size
Power Supply	AVDD28: 2.8V DVDD: 1.2V IOVDD: 1.8V
Power Consumption	TBD
MAX SNR	38dB
Dark Current	TBD
Sensitivity	3.9 V/lux·s
Dynamic range	81 dB linear mode 105 dB HDR mode
Operating temperature:	-30~85℃
Stable Image temperature	0~60℃
Storage temperature	-40~125℃
Optimal lens chief ray angle(CRA)	12°(linear)
Package type	CSP
Input clock frequency	6~27MHz

2. DC Parameters

2.1 Standby Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	TBD	TBD	uA
Digital	I_{DVDD}	—	TBD	TBD	uA
I/O	I_{IOVDD}	—	TBD	TBD	uA

RST: L, PWND: L

Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, $T_j=25^{\circ}\text{C}$

2.2 Power off Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	0	0	uA
Digital	I_{DVDD}	—	0	0	uA
I/O	I_{IOVDD}	—	0	0	uA

Power off, $T_j=25^{\circ}\text{C}$

2.3 Operation current

Full size (DVP)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	TBD	TBD	mA
Digital	I_{DVDD}	—	TBD	TBD	mA
I/O	I_{IOVDD}	—	TBD	TBD	mA

Input clock: 27MHz, Frame rate: 30FPS, RAW 10,

Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, $T_j=25^{\circ}\text{C}$

Full size (MIPI 2 Lane)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	TBD	TBD	mA
Digital	I_{DVDD}	—	TBD	TBD	mA
I/O	I_{IOVDD}	—	TBD	TBD	mA

Input clock: 27MHz, Frame rate: 30FPS, RAW 10,

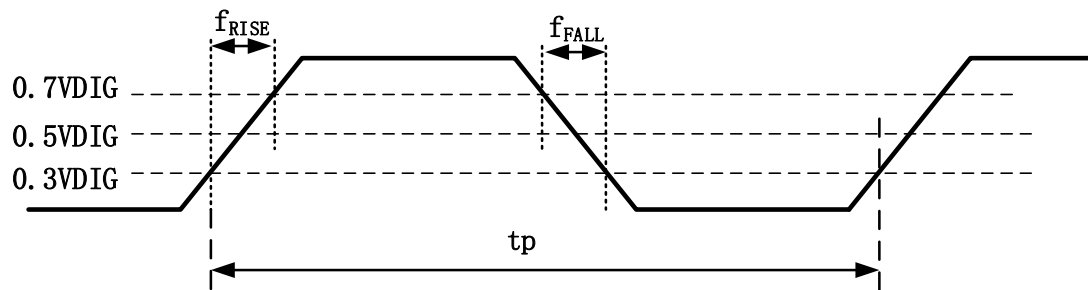
Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, $T_j=25^{\circ}\text{C}$

2.4 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Power supply	V_{AVDD}	2.7	2.8	2.9	V
	V_{DVDD}	1.15	1.2	1.3	V
	V_{IOVDD}	1.7	1.8	2.8	V
Digital Input(Conditions: AVDD = 2.8V, DVDD =1.2V, IOVDD = 1.8V)					
Input voltage HIGH	V_{IH}	0.7*VIF			V
Input voltage LOW	V_{IL}			0.3*VIF	V
Digital Output(Conditions: AVDD =2.8V, IOVDD = 1.8V, standard Loading 25PF)					
Output voltage HIGH	V_{OH}	0.8*VIF			V
Output voltage LOW	V_{OL}			0.2*VIF	V

3. AC Characteristics

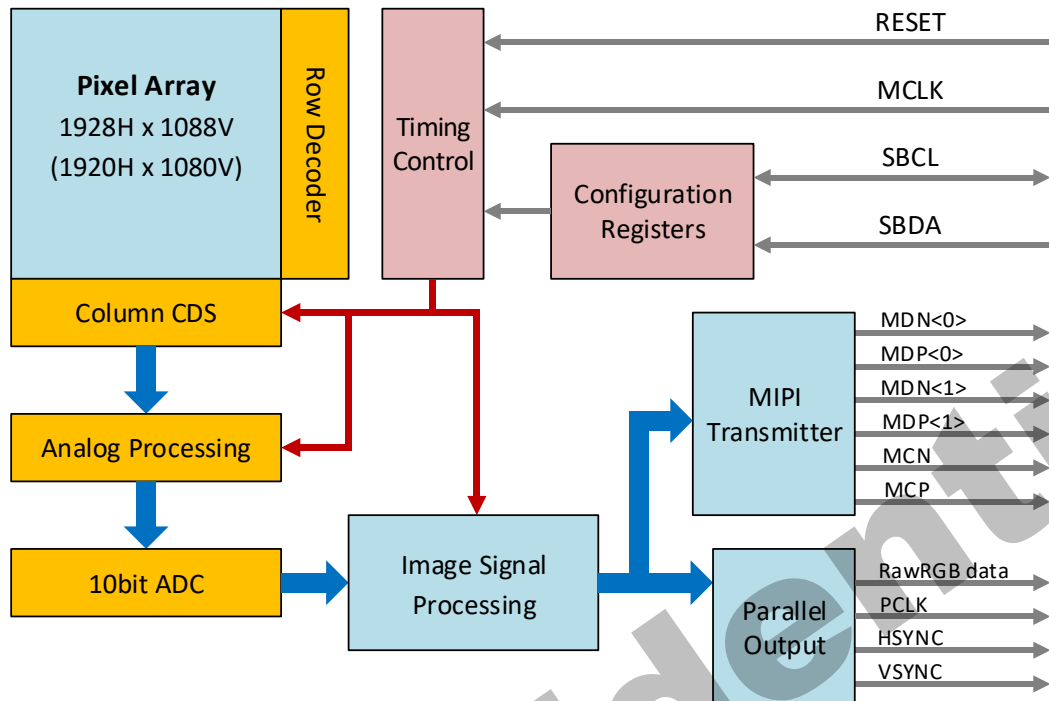
Master clock wave diagram



Input clock square waveform specifications :

Item	Symbol	Min	Typ	Max	unit
Frequency	f_{SCK}	6	24	27	MHz
jitter (period,	T_{jitter}			600	ps
Rise Time	f_{RISE}	1		15	ns
Fall Time	f_{FALL}	1		15	ns
Duty Cycle	f_{DUTY}	40		60	%
Input Leakage	f_{ILEAK}	-10		10	μA

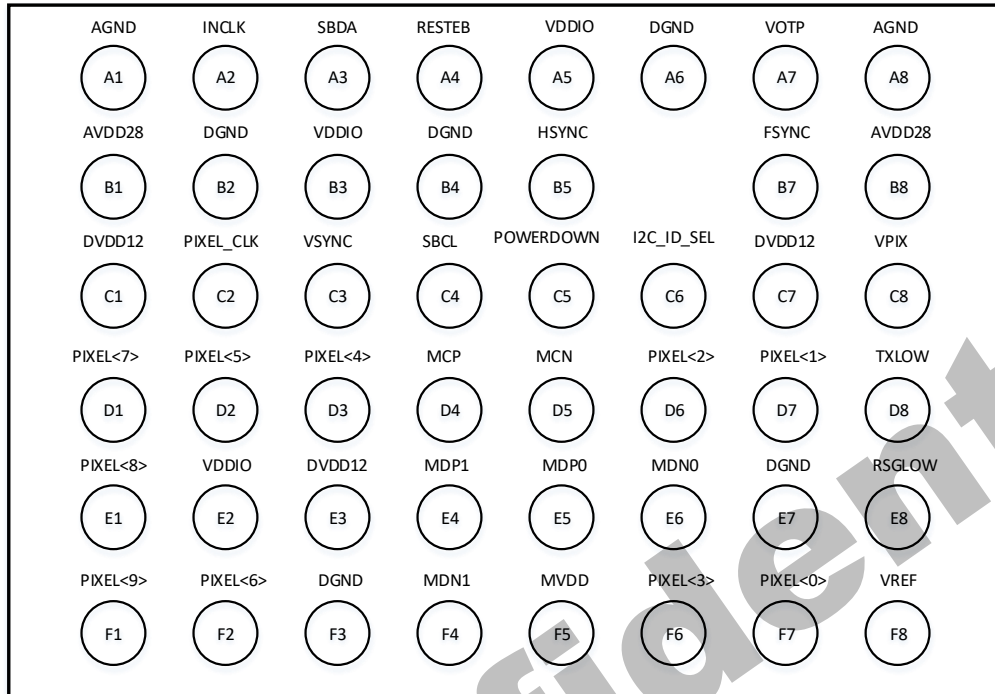
4. Block Diagram



GC2093 has an active image array of 1920x1080 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block. Users can easily control these functions via two-wire serial interface bus.

5. CSP Package Specifications

5.1 Pin Diagram (CSP)



Top View

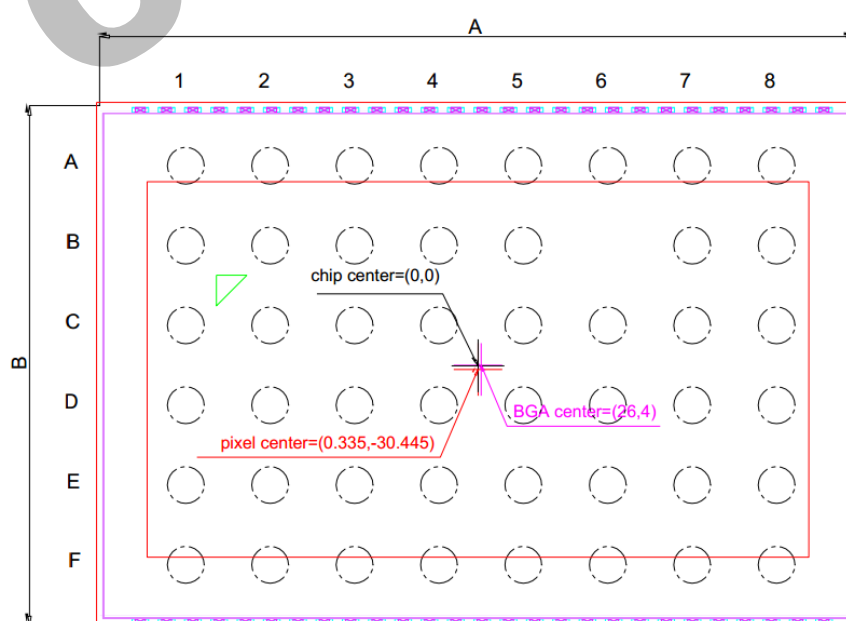
5.2 Pin Descriptions

Pin	Name	Pin Type	Description
A1	AGND	Ground	Ground for analog
A2	INCLK	Input	Sensor input clock
A3	SBDA	I/O	Two-wire serial bus, data
A4	RESETB	Input	Chip reset control: (floating forbidden) 0: chip reset 1: normal work
A5	VDDIO	POWER	I/O POWER.
A6	DGND	Ground	Ground for digital
A7	VOTP	POWER	For OTP power supply
A8	AGND	Ground	Ground for analog
B1	AVDD28	AVDD28	ANALOG POWER

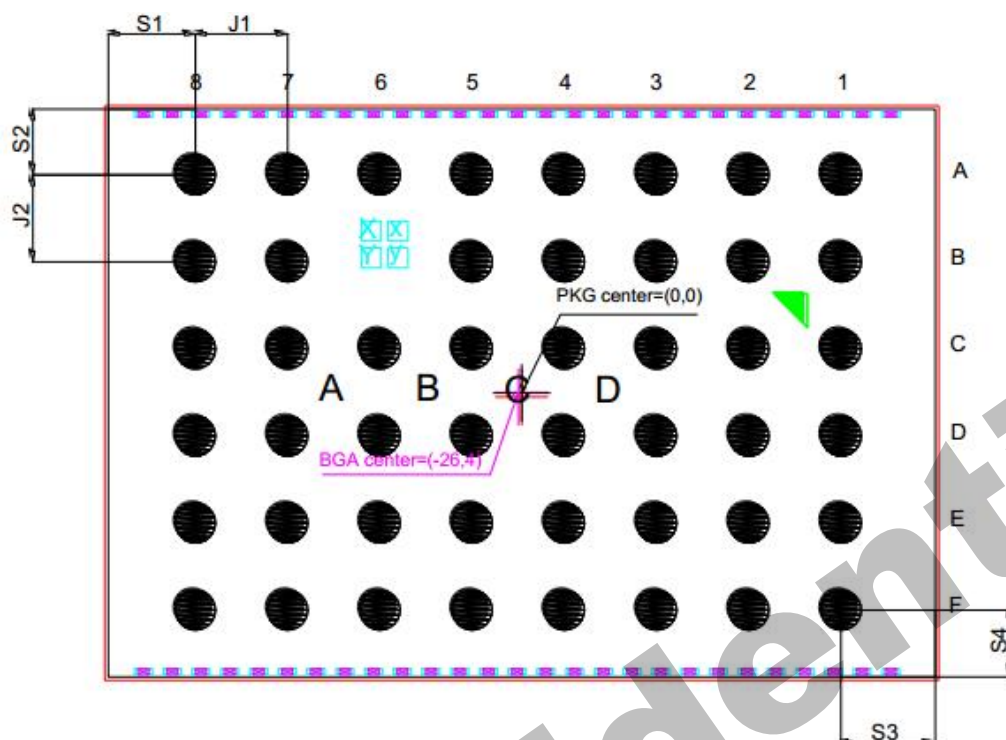
B2	DGND	Ground	Ground for digital
B3	VDDIO	POWER	I/O POWER
B4	DGND	Ground	Ground for digital
B5	HSYNC	Output	DVP HSYNC
B6	\	\	\
B7	FSYNC	I/O	Frame sync control
B8	AVDD28	POWER	ANALOG POWER
C1	DVDD12	POWER	DIGITAL POWER
C2	PIXEL_CLK	Output	DVP CLK
C3	VSYN	Output	DVP VSYNC
C4	SBCL	Input	Two-wire serial bus, clock
C5	POWERDOWN	Input	Sensor power down control: (floating forbidden) 0: standby 1: normal work
C6	I2C_ID_SEL	Input	ID_SEL (floating forbidden) 0: 0x6e/0x6f (default) 1: 0xfc/0xfd
C7	DVDD12	POWER	DIGITAL POWER
C8	VPIX	POWER	Internal power supply
D1	PIXEL<7>	Output	DVP07
D2	PIXEL<5>	Output	DVP05
D3	PIXEL<4>	Output	DVP04
D4	MCP	Output	MIPI clock (+)
D5	MCN	Output	MIPI clock (-)
D6	PIXEL<2>	Output	DVP02
D7	PIXEL<1>	Output	DVP01
D8	TXLOW	POWER	Internal power supply
E1	PIXEL<8>	Output	DVP08

E2	VDDIO	POWER	I/O POWER
E3	DVDD12	POWER	DIGITAL POWER
E4	MDP1	Output	MIPI data <1> (+)
E5	MDP0	Output	MIPI data <0> (+)
E6	MDN0	Output	MIPI data <0> (-)
E7	DGND	Ground	Ground for digital
E8	RSGLOW	POWER	Internal power supply
F1	PIXEL<9>	Output	DVP09
F2	PIXEL<6>	Output	DVP06
F3	DGND	Ground	Ground for digital
F4	MDN1	Output	MIPI data <1> (-)
F5	MVDD	Power	DIGITAL POWER
F6	PIXEL<3>	Output	DVP03
F7	PIXEL<0>	Output	DVP00
F8	VREF	POWER	Internal power supply

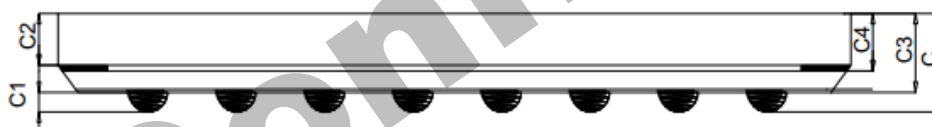
5.3 Package Specification (unit: μm)



GC2093 Package diagram (Top View Image Side)



GC2093 Package diagram (Bottom View BGA Side)



GC2093 Package diagram (Side View)

Description	symbol	Nominal	Min	Max
		Millimeters		
Package Body Dimension X	A	6.1870	6.1620	6.2120
Package Body Dimension Y	B	4.2400	4.2150	4.2650
Package Height	C	0.7600	0.7050	0.8150
Ball Height	C1	0.1500	0.1200	0.1800
Glass Thickness	C2	0.4000	0.3900	0.4100
CV Thickness	C3	0.6100	0.5750	0.6450

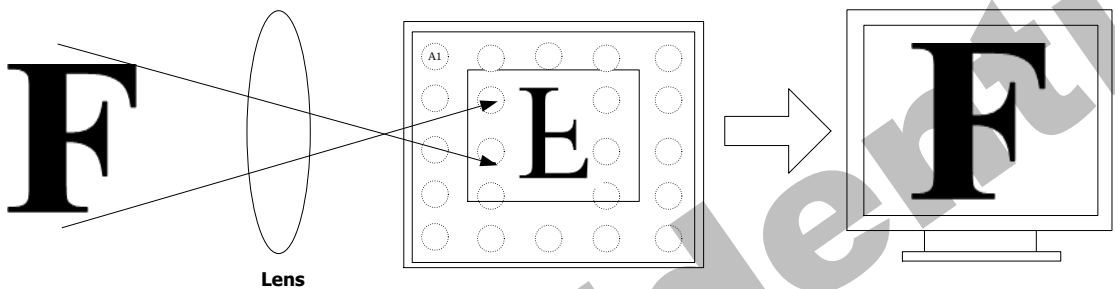
Silicon Thickness	C4	0.4450	0.4250	0.4650
Package Body Thickness	D	0.3000	0.2700	0.3300
Thickness from top glass surface to wafer	N	47		
Ball Diameter	N1	8		
Total Ball Count	N2	6		
Ball Count X axis	J1	0.6900		
Ball Count Y axis	J2	0.6500		
Pins pitch X axis	X	0.026000	0.001000	0.051000
Pins pitch Y axis	Y	0.004000	-0.02100	0.029000
BGA ball center to package center offset in X-direction	X1	0.026000	0.001000	0.051000
BGA ball center to package center offset in Y-direction	Y1	0.004000	-0.021000	0.029000
BGA ball center to chip center offset in X-direction	S1	0.652500	0.622500	0.682500
BGA ball center to chip center offset in Y-direction	S2	0.491000	0.461000	0.521000
Edge to Pin Center Distance along X	S3	0.704500	0.674500	0.734500
Edge to Pin Center Distance along Y	S4	0.499000	0.469000	0.529000

Note: The package center, optical center, and BGA center of the chip are not coincident. If setting the package center as the origin (0, 0), the BGA center coordinate is (26, 4), the optical center coordinate is (0.335, -30.445), with μm unit.

6. Optical Specifications

6.1 Readout Position

The GC2093 default status is readout from the lower left corner with pin A1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so proper image output results when Pin A1 is located in the upper left corner.



Readout direction can be set by the registers.

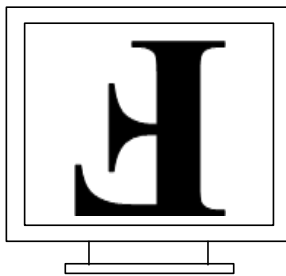
Function	Register Address	Register Value	First Pixel
Normal	0x0017[1:0]	00	Gr
Horizontal mirror	0x0017[1:0]	01	R
Vertical Flip	0x0017[1:0]	10	B
Horizontal Mirror and Vertical Flip	0x0017[1:0]	11	Gb



Horizontal Mirror

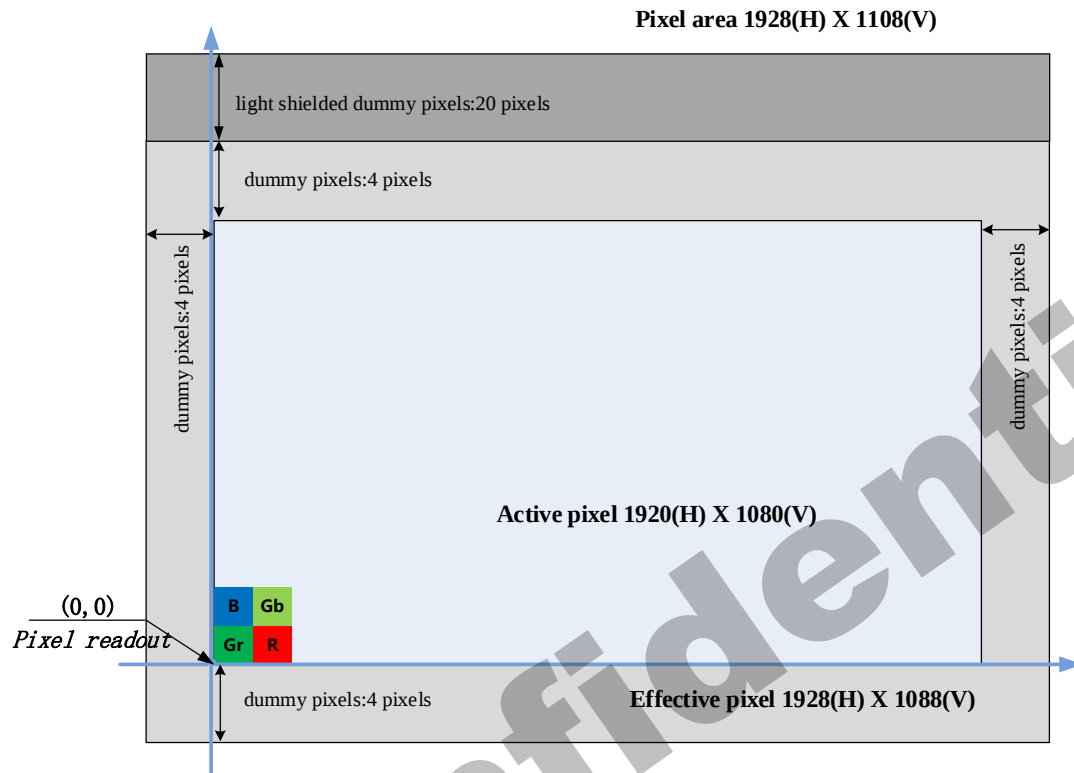


Vertical Flip



Horizontal Mirror and Vertical Flip

6.2 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color GR/BG array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 1919. If flip in column, column is read out from 1919 to 0.

If no flip in row, row is read out from 0 to 1079. If flip in row, row is read out from 1079 to 0.

6.3 Lens Chief Ray Angle (CRA)

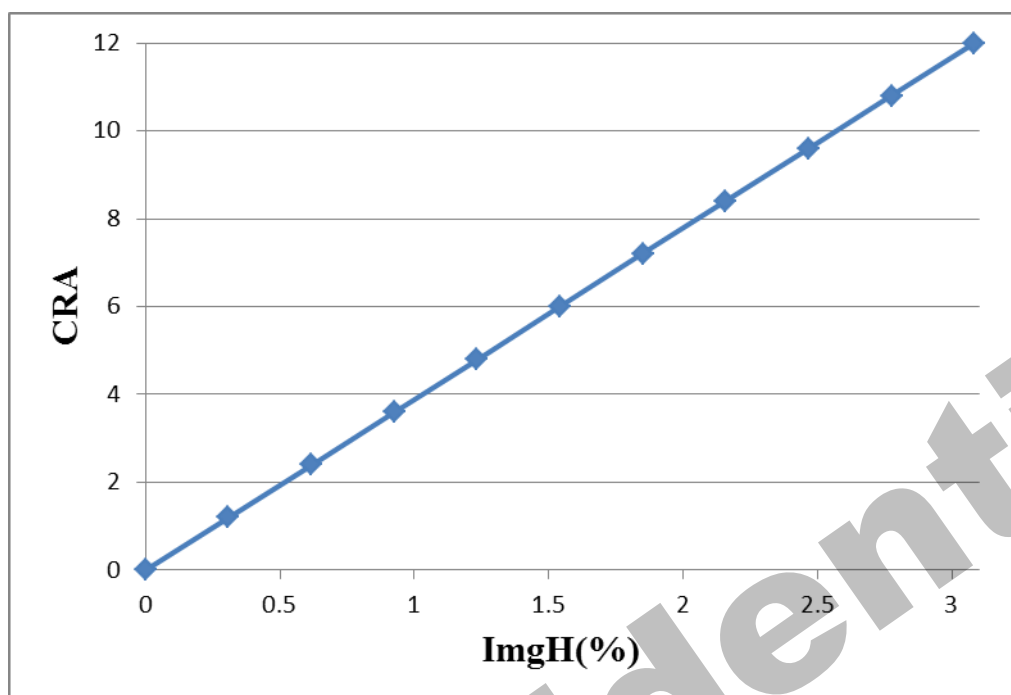


Image Height (%)	Image Height (mm)	CRA (degree)
0	0	0
10	0.3085	1.2
20	0.617	2.4
30	0.9255	3.6
40	1.234	4.8
50	1.5425	6
60	1.851	7.2
70	2.1595	8.4
80	2.468	9.6
90	2.7765	10.8
100	3.085	12

6.4 QE Spectral Characteristics

TBD

7. Two-wire Serial Bus Communication

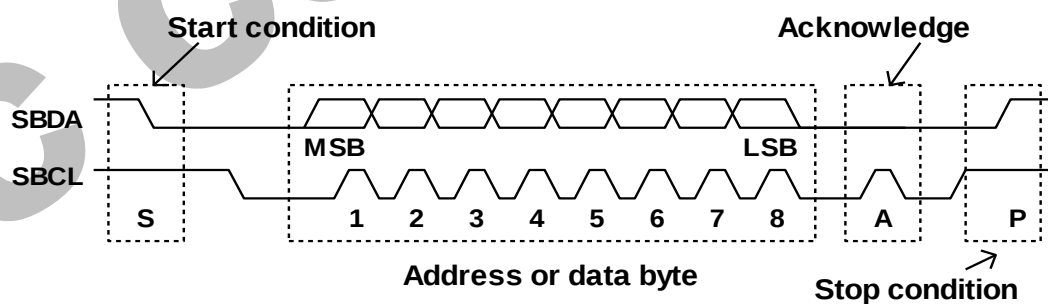
GC2093 Device Address:

ID_SEL	Slave address write mode	Slave address read mode
0(default)	0x6e	0x6f
1	0xfc	0xfd

7.1 Protocol

The host must perform the role of a communications master and GC2093 acts as either a slave receiver or transmitter. The master must do

- ◆ Generate the **Start(S)/Stop(P)** condition
- ◆ Provide the serial clock on **SBCL**.



Single Register Writing:

S	6eH	A	Register Address	A	Data	A	P
---	-----	---	------------------	---	------	---	---

Incremental Register Writing:

S	6eH	A	Register Address	A	Data(1)	A		Data(N)	A	P
---	-----	---	------------------	---	---------	---	-------	---------	---	---

Single Register Reading:

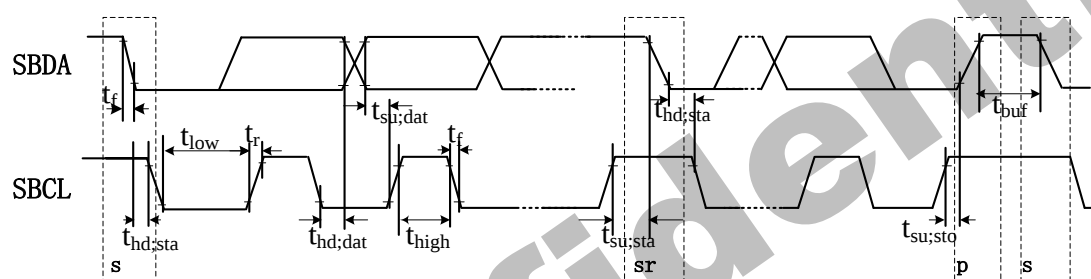
S	6eH	A	Register Address	A	S	6fH	A	Data	NA	P
---	-----	---	------------------	---	---	-----	---	------	----	---

Notes:

From master to slave



From slave to master

S: Start condition**P:** Stop condition**A:** Acknowledge bit**NA:** No acknowledge**Register Address:** Sensor register address**Data:** Sensor register value**7.2 Serial Bus Timing**

Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between stop and start condition	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	0.6	--	--	μs
Data hold time	$t_{hd;dat}$	0	--	0.9	μs
Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	Pf

8.1 DVP timing

Timing diagram for Vsync and Hsync signals. The diagram shows two horizontal timelines. The top timeline is labeled Vsync and the bottom timeline is labeled Hsync. Vsync has a single pulse with a width labeled Ft and a delay from the start of the frame to the start of the pulse labeled St. Hsync has a series of pulses with a width labeled Vt and a delay from the start of the frame to the start of the first pulse labeled Et. A vertical blanking interval VB is shown between the end of Vsync and the start of Hsync.

VB->Vblank, setting by register 0x0007 and 0x0008

The diagram illustrates the timing relationships for the HS-Link protocol. It features two main signals: CLK (red) and Dp/Dn (blue). The CLK signal is shown as a series of red circles, and the Dp/Dn signal is shown as a blue line. The diagram includes several timing parameters: $T_{CLK-POST}$, $T_{CLK-TRAIL}$, $T_{HS-EXIT}$, $T_{HS-LEAVE}$, T_{LPX} , $T_{HS-RECOVER}$, $T_{CLK-ZERO}$, $T_{CLK-SETTLE}$, $T_{HS-SETTLE}$, $T_{HS-SKIP}$, $T_{CLK-MISS}$, T_{EOT} , T_{CLK-PR} , T_{HS-PR} , and $T_{HS-SETTLE}$. The diagram is divided into several sections by vertical dashed lines, indicating different states of the link.

- ◆ Clock must be reliable during high speed transmission and mode-switching.
- ◆ Clock can go to LP only if data lanes are in LP (and nothing relies on it).

- ◆ In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

$T_{CLK_HS_PREPARE}$: setting by Register 0x0322

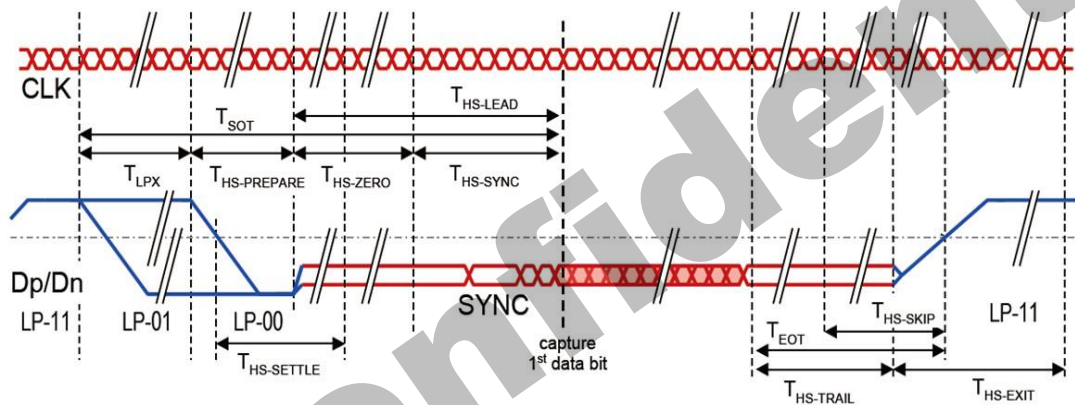
T_{CLK_ZERO} : setting by Register 0x0323

T_{CLK_PRE} : setting by Register 0x0324

T_{CLK_POST} : setting by Register 0x0325

T_{CLK_TRAIL} : setting by Register 0x0326

8.3 Data Burst



Notice:

- ◆ Clock keeps running and samples data lanes (except for lanes in LPS).
- ◆ Unambiguous leader and trailer sequences required to distill real bits.
- ◆ Trailer is removed inside PHY (a few bytes).
- ◆ Time-out to ignore line values during line state transition.

T_{LPX} : setting by Register 0x0321

$T_{HS_PREPARE}$: setting by Register 0x0329

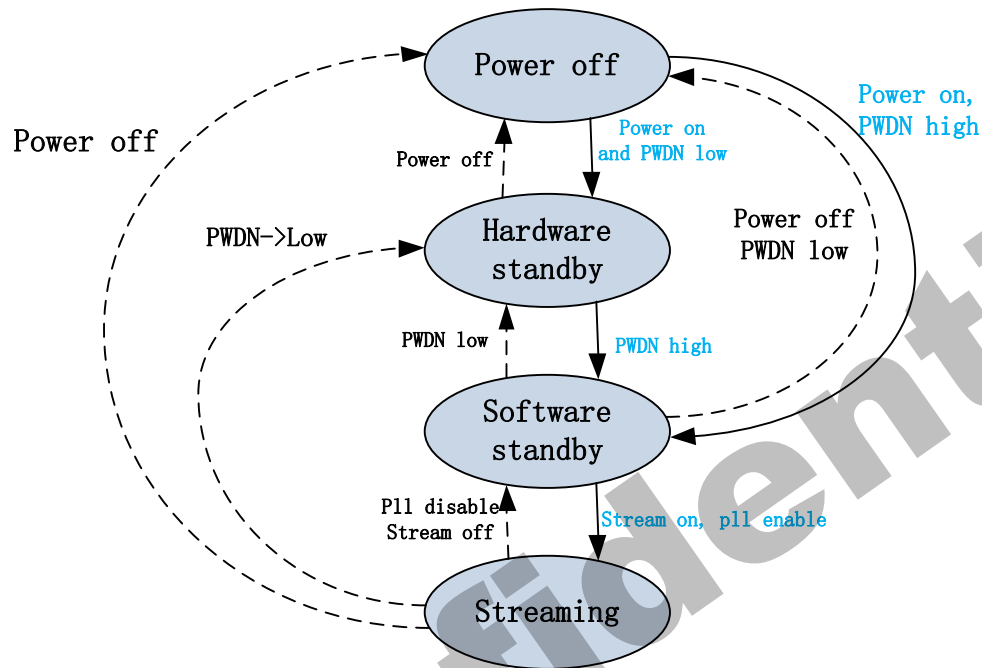
T_{HS_ZERO} : setting by Register 0x032a

T_{HS_TRAIL} : setting by Register 0x032b

T_{HS_EXIT} : setting by Register 0x0327

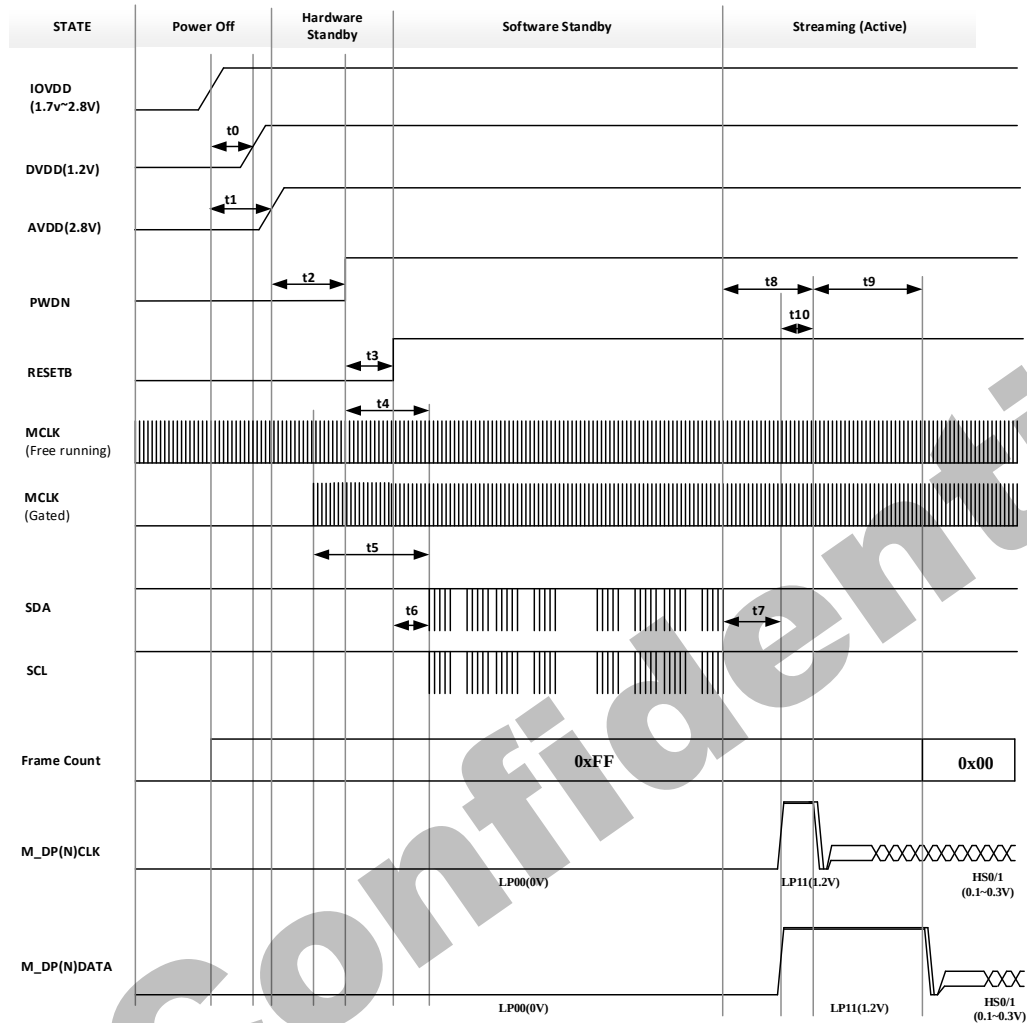
9. Function description

9.1 Operation mode



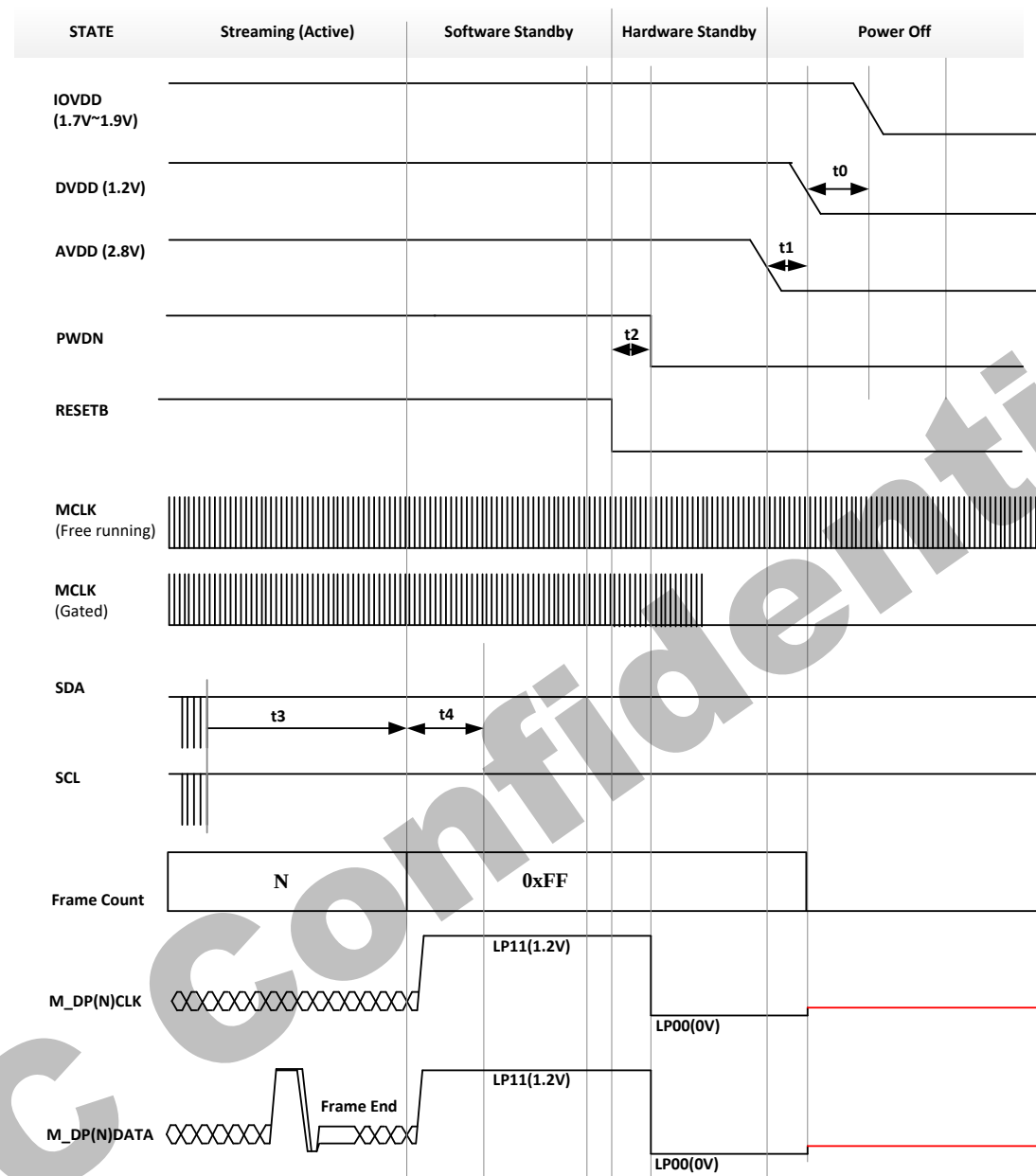
Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on PWDN and RESETB, and stop MCLK	PWDN low
Software standby	Two- wire serial communication with sensor, pll is ready for fast return to streaming mode	Stream mode off PLL disable RESETB high PWDN high
Streaming	Sensor is fully powered and is streaming image data on the MIPI CSI-2 bus	All

9.2 Power on Sequence



Parameter	Description	Min.	Max	Unit
t0	From IOVDD to DVDD12	50	-	μs
t1	From IOVDD to AVDD28	50	-	μs
t2	From AVDD28 to PWDN pull high	0	-	μs
t3	From PWDN pull high to RESETB pull high	0	-	μs
t4	PWDN rising to first I2C transaction	50	-	μs
t5	Minimum No. of MCLK cycles prior to the first I2C transaction	1200	-	MCLK
t6	From RESETB rising to first I2C transaction	50	-	μs
t7	PLL start up/lock time	-	1	ms
t8	Entering streaming mode – First frame start sequence (fixed part)		10	ms
t9	Entering streaming mode – First frame start sequence (variable part)	-		lines
t10	DPHY initialization period (TINIT)	0.1	-	ms

9.3 Power off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From DVDD12 pull down to IOVDD pull down	0	-	μs
t1	From AVDD28 pull down to DVDD12 pull down	0	-	μs
t2	From RESETB pull low to PWDN pull low	0	-	μs
t3	Enter Software Standby CCI command – Device in Software Standby mode	0	-	μs
t4	Minimum number of MCLK cycles after the last CCI transaction or MIPI frame end code.	2000		MCLK

- If the sensor's power cannot be cut off, please keep power supply, then set PWDN pin low. It will make sensor standby

- Register should be reloaded before works.
- If the standby sequence needs to be modified, please contact FAE of *Galaxycore Inc.*

9.4 Black level calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

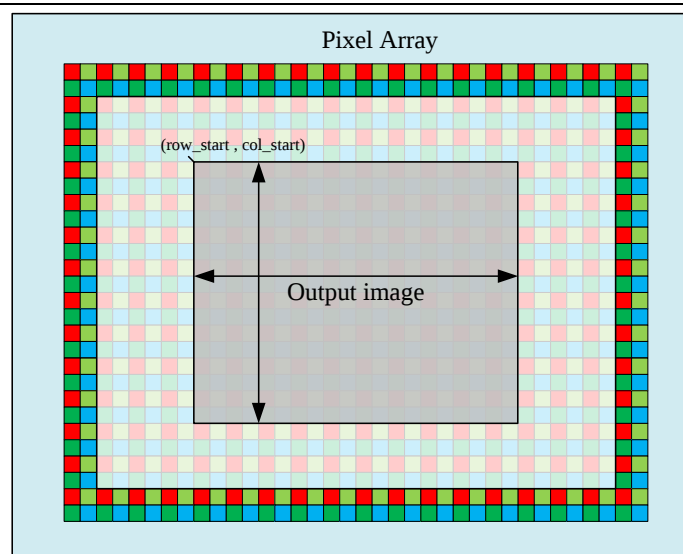
9.5 Integration time

The integration time is controlled by the integration time registers

Addr.	Register name	Description
0x0003	Shutter time	[5:0] shutter time[13:8]
0x0004		[7:0] shutter time[7:0]
0x0041	Frame length	[5:0] frame length[13:8]
0x0042		[7:0] frame length[7:0]

9.6 Windowing

GC2093 has a rectangular pixel array 1920 x 1080, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.



Addr.	Register name	Description
0x000d	win_height	[2:0]win_height[10:8]
0x000e		[7:0]win_height[7:0]
0x000f	win_width	[3:0]win_width[11:8]
0x0010		[7:0]win_width[7:0]
0x0009	Row start	[2:0]row_start[10:8]
0x000a		[7:0]row_start [7:0]
0x000b	Col start	[2:0]col_start[10:8]
0x000c		[7:0]col_start[7:0]

9.7 HDR mode

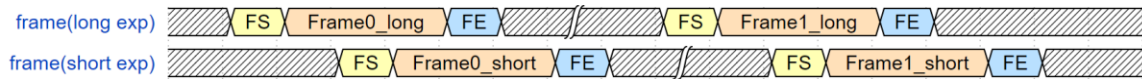
GC2093 has HDR function. If the function is enabled, by setting 2 different exposure times (always called long and short exposure), user can get 2 frame data in staggered output mode, and can combine two frames into one picture to improve dynamic range and avoid smearing.

The DVP output timing as following:



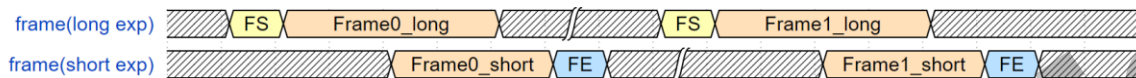
When user choose MIPI protocol as output format, different exposure time line can be distinguished by virtual channel according to MIPI protocol. By default, long exposure line' ID is 00, and short exposure line's ID is 01.

The MIPI output timing as following (virtual channel mode):



Additionally, User can distinguish different exposure time line without virtual channel. In this mode, Short exposure time line has fixed offset lines with Long exposure time line.

The MIPI output timing as following (no virtual channel mode):

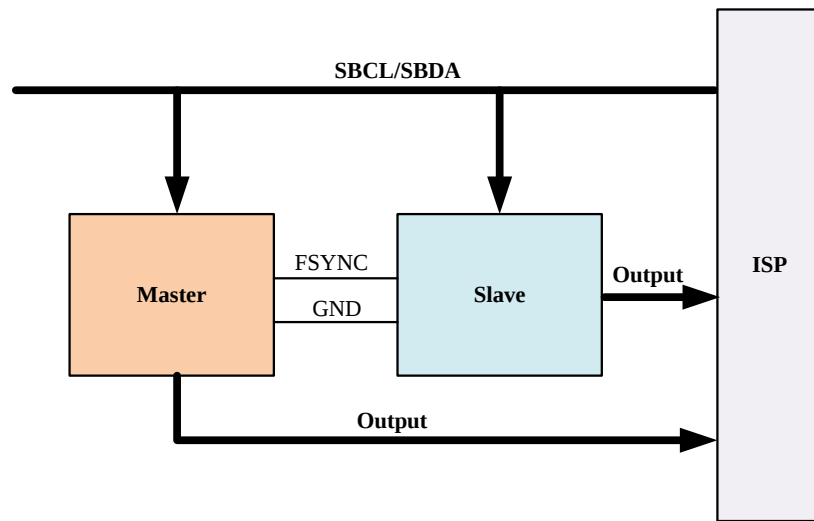


The HDR related registers is in the following table

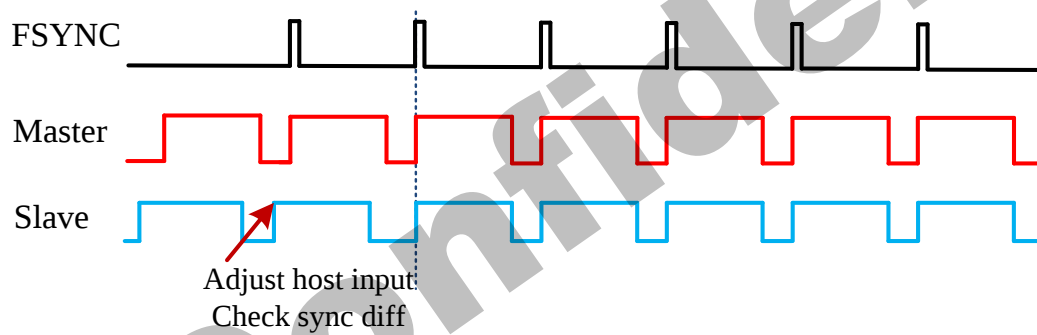
Addr.	Register name	Description
0x0027	HDR enable	[4] HDR Mode 1: HDR enable 0: HDR disable
0x0001	Shutter time	[5:0] Short exposure shutter time[13:8]
0x0002		[7:0] Short exposure shutter time[7:0]
0x0003		[5:0] Long exposure shutter time[13:8]
0x0004		[7:0] Long exposure shutter time[7:0]
0x0215	Virtual Channel	[7]virtual channel En 1: virtual channel enable 0: virtual channel disable [1:0] virtual channel ID

9.8 Frame sync mode

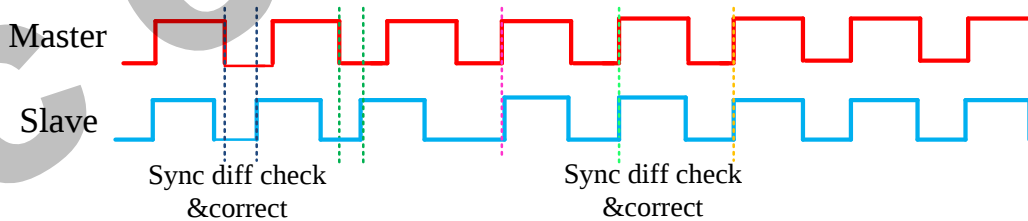
GC2093 can support hardware frame sync for dual camera application. It can be set both master and slave sensor. When use this mode, the two sensor's FSYNC pin must connect to each other.



Adjust mismatch sync



Dynamic mismatch sync control



Addr.	Register name	Description
0x007f	fsync_mode	[4]fsync_clear_counter [3:0]fsync_mode
0x0082	fsync_mode_new2	
0x0083	fsync_mode_new3	
0x0084	Fsync row time	
0x0085	fsync_mode_new4	
0x0086	fsync_row_diff_th	[5:0] fsync_row_diff_th

0x0087	Debug_mode4	[5:4] fsync_vb_gap
0x0088	fsync_row_diff_big[13:8]	[5:0] fsync_row_diff_big[13:8]
0x0089	fsync_row_diff_big [7:0]	[7:0] fsync_row_diff_big [7:0]
0x008a	fsync_row_diff_big2[13:8]]	[5:0] fsync_row_diff_big2[13:8]
0x008b	fsync_row_diff_big2 [7:0]	[7:0] fsync_row_diff_big2[7:0]

9.9 OTP memory

GC2093 sensor has 1K bits embedded OTP(One Time Programmable) memory, 256 bits, which is for storing camera module calibration data.

9.10 Frame structure

Frame structure is controlled by HB, frame length, window start, window height, window width and VB.

Frame length control

Frame length are controlled by window height, minimum VB and shutter time.

- Frame length depend shutter time.
 - Minimum frame length = window height + 20 +VB (VB_min = 16)
 - If shutter time < minimum frame length:
Actual frame length = minimum frame length
 - If shutter time > minimum frame length:
Actual frame length = shutter time + 16 (recommended).
- Fix frame rate
 - User can fix VB to fix frame rate.

Line length control

Line length = 1200 (not recommended to be modified)

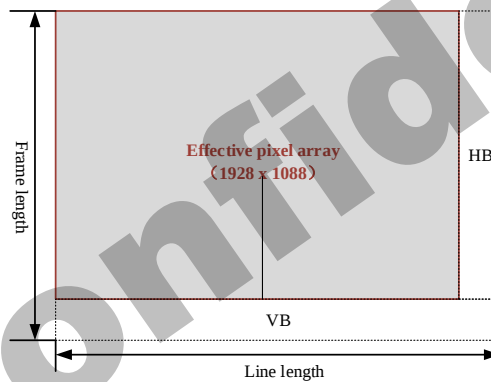
Addr.	Register name	Description
0x0005	Line length	[3:0] Line length[11:8] X2
0x0006		[7:0] Line length[7:0] X2

Output window array control

Addr.	Register name	Description
0x0191	Out_window_y1	[2:0] Out_window_y1[10:8]
0x0192		[7:0] Out_window_y1[7:0]
0x0193	Out_window_x1	[3:0] Out_window_x1[11:8]
0x0194		[7:0] Out_window_x1[7:0]
0x0195	Out window height	[2:0] Out window height[10:8]
0x0196		[7:0] Out window height[7:0]
0x0197	Out window width	[3:0] Out window width[11:8]
0x0198		[7:0] Out window width[7:0]

Blank time control

1. line blank time is controlled by HB
2. frame blank time
 - frame blank time = frame length lines – window height – 20



10. Register List

System Register

Address	Name	Width	Default Value	Description
0x03f0	CHIP_ID_high	8	0x20	[7:0]CHIP ID high
0x03f1	CHIP_ID_low	8	0x93	[7:0]CHIP ID low
0x0005	Line length[11:8]	4	0x04	
0x0006	Line length[7:0]	8	0x48	
0x0041	Frame length[13:8]	6	0x04	
0x0042	Frame length[7:0]	8	0xe0	
0x0009	CISCTL_capt_row_start[10:8]	3	0x00	
0x000a	CISCTL_capt_row_start [7:0]	8	0x00	
0x000b	CISCTL_capt_col_start [10:8]	3	0x00	
0x000c	CISCTL_capt_col_start [7:1]	8	0x00	
0x000d	CISCTL_capt_win_height[10:8]	3	0x04	
0x000e	CISCTL_capt_win_height [7:0]	8	0x48	
0x000f	CISCTL_capt_win_width [10:8]	3	0x07	
0x0010	CISCTL_capt_win_width [7:0]	8	0x90	
0x0190	Win_mode	1	0x01	
0x0191	out_win_y1[10:8]	3	0x00	
0x0192	out_win_y1[7:0]	8	0x00	
0x0193	Out_win_x1[11:8]	4	0x00	
0x0194	Out_win_x1[7:0]	8	0x00	
0x0195	Out_win_height[10:8]	3	0x04	
0x0196	Out_win_height[7:0]	8	0x38	
0x0197	Out_win_width[11:8]	4	0x07	
0x0198	Out_win_width[7:0]	8	0x38	
0x0199	Out_win_offset	4	0x05	for auto_updown[3:2] out_offset_y1=1 for auto_mirror[1:0] out_offset_x1=1
0x0160	WB_offset	8	0x00	
0x0017	Mirror & flip	2	0x00	[1]: flip [0]: mirror
0x018c	Test_Image	1	0x00	[0]: test image en

Analog & CISCTL

Address	Name	Width	Default Value	Description
0x0001	Exposure_Short[13:8]	6	0x00	
0x0002	Exposure_Short [13:8]	8	0x00	
0x0003	Exposure [13:8]	6	0x00	
0x0004	Exposure [7:0]	8	0x10	
0x00b1	auto_pregain_sync[9:6]	4	0x01	4.6 Precision
0x00b2	auto_pregain[5:0]	8	0x00	
0x00b3	Analog_PGA_gain[7:0]	8	0x00	
0x00b4	Analog_PGA_gain[9:8]	2	0x00	
0x00b8	Col_gain[11:6]	8	0x00	6.6 Precision
0x00b9	Col_gain[5:0]	8	0x00	

CSI/PHY1.0

Address	Name	Width	Default Value	Description
0x0201	DPHY_analog_mode1	8	0x20	
0x0202	DPHY_analog_mode2	8	0x16	
0x0203	DPHY_analog_mode3	8	0xca	
0x0204	FIFO_prog_full_level[7:0]	8	0x08	
0x0205	FIFO_prog_full_level[11:8]	4	0x00	
0x0206	FIFO_mode	8	0x00	
0x0211	LDI_set	8	0x2b	
0x0212	LWC_set[7:0]	8	0x60	
0x0213	LWC_set[15:8]	8	0x09	
0x0214	SYNC_set	8	0xb8	
0x0215	DPHY_mode	8	0x10	
0x0216	LP_set	8	0x29	
0x021b	fifo2_prog_full_level	5	0x08	
0x021c	fifo2_push_prog_full_level	5	0x08	
0x021d	sram_test_mode	4	0x02	
0x0220	T_init_set	8	0x80	
0x0221	T_LPX_set	8	0x10	
0x0222	T_CLK_HS_PREPARE_set	8	0x05	
0x0223	T_CLK_zero_set	8	0x20	
0x0224	T_CLK_PRE_set	8	0x02	
0x0225	T_CLK_POST_set	8	0x20	

0x0226	T_CLK_TRAIL_set	8	0x08	
0x0227	T_HS_exit_set	8	0x10	
0x0228	T_wakeup_set	8	0xa0	
0x0229	T_HS_PREPARE_set	8	0x06	
0x022a	T_HS_Zero_set	8	0x0a	
0x022b	T_HS_TRAIL_set	8	0x08	
0x0230	MIPI_test	2	0x00	
0x0235	OUT_pad_test_data	8	0x00	
0x0236	clkIp_drv	2	0x00	[1:0]clkIp_drv
0x0237	lp_drv	4	0x00	[3:2] data1lp_drv [1:0] data0lp_drv
0x0238	prbs_mode	8	0x20	
0x0239	prbs_LDI	8	0x3d	
0x024a	prbs_seed[7:0]	8	0x9a	
0x024b	prbs_seed[15:8]	8	0x78	
0x024c	MIPI_TSEL	2	0x01	[1:0] MIPI_TSEL
0x02aa	o_vsync_pola o_hsync_pola pad_test_valid pad_test_value	8	0x00	[7] o_vsync_pola [6] o_hsync_pola [5:3] pad_test_valid [2:0]pad_test_value

Fsync

Address	Name	Width	Default Value	Description
0x007f	fsync_mode	8	0x13	[3:0]fsync_mode
0x0082	fsync_mode_new2	8	0x00	
0x0083	fsync_mode_new3	6	0x04	
0x0084	Fsync row time	8	0x00	
0x0085	fsync_mode_new4	8	0x01	
0x0086	fsync_row_diff_th	8	0x02	[5:0] fsync_row_diff_th
0x0087	Debug_mode4	8	0x58	[5:4] fsync_vb_gap
0x0088	fsync_row_diff_big[13:8]	6	0x00	
0x0089	fsync_row_diff_big [7:0]	8	0x04	
0x008a	fsync_row_diff_big2[13:8]	6	0x00	
0x008b	fsync_row_diff_big2 [7:0]	8	0x10	

HDR

Address	Name	Width	Default Value	Description
0x0027	HDR enable	1	0x00	[0] HDR Mode 1: HDR enable 0: HDR disable
0x0215	Virtual Channel	8	0x05	[7]virtual channel En 1: virtual channel enable 0: virtual channel disable [1:0] virtual channel ID