GC2083 CSP

1/3’’ 2Mega CMOS Image Sensor

Datasheet

V1.1

2022-05-18

Ordering Information

◆ **GC2083-C51YA**

(Colored, 50PIN-CSP)

GENERATION REVISION HISTORY

Version.	Effective Date	Description of Changes	Prepared by
V1.0	2022-05-07	Document Release	DSC-AE Dept.
V1.1	2022-05-18	P11: Update MCN pin, MCP pin Description	DSC-AE Dept.

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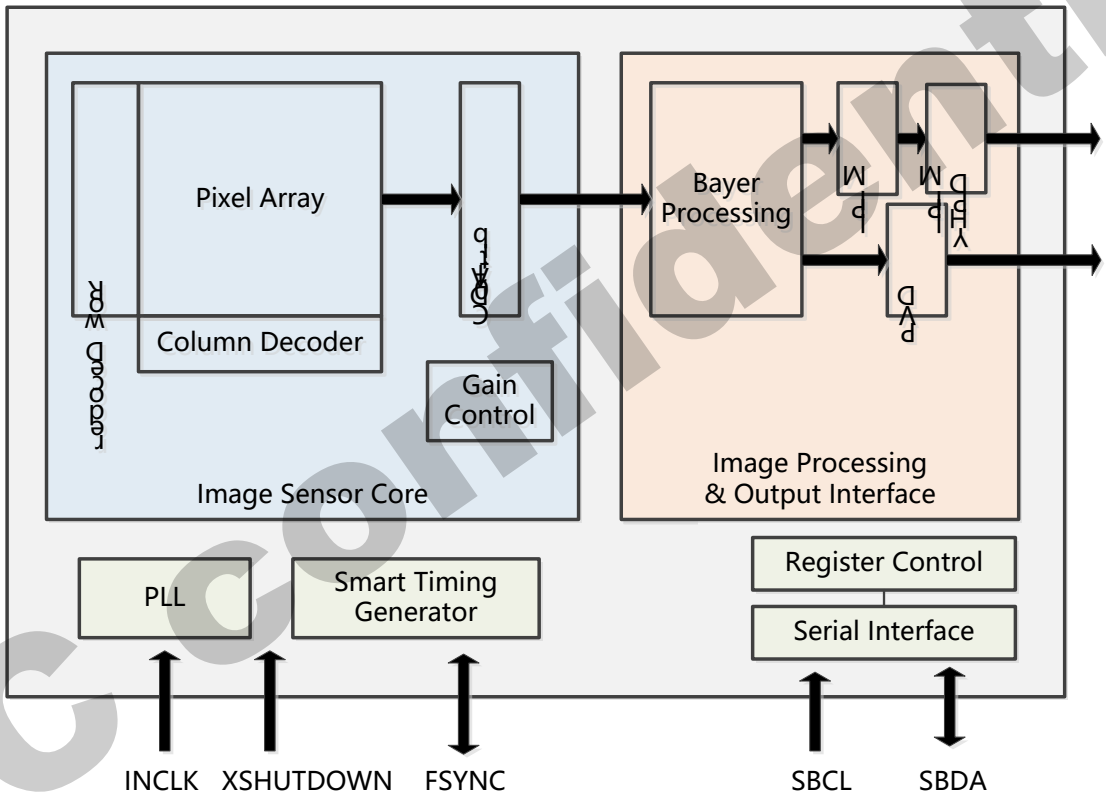
1. Sensor Overview

1.1 General Description

GC2083 is a high quality 2Mega CMOS image sensor, for security camera digital camera and mobile phone camera applications. GC2083 incorporates a 1920H x 1080V active pixel array, on-chip 10-bit ADC, and image signal processor. It is programmable through a simple two-wire serial interface and has very low power consumption. It provides RAW10 and RAW8 data formats with MIPI and DVP interface.

Figure 1: Block Diagram



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1.2 Features

- Optical size: 1/3 inch
- Pixel size : 2.7μm x 2.7μm FSI
- Active image size: 1920 x 1080
- Color Filter: RGB Bayer
- Output formats: Raw Bayer 10bit/8bit
- Power supply requirement: AVDD28: 2.7~2.9V (Typ. 2.8V)
  DVDD: Generated by the internal regulator (Typ.1.2V)
  IOVDD: 1.7~1.9V (Typ. 1.8V)
- Power Consumption: 128mW @Full Size @30fps
- Frame rate: 30fps@Full Size
- PLL support
- Frame sync support (master/slave)
- Windowing support
- Mirror and Flip support
- Analog Gain: 64X(Max)
- Sensitivity: 3.24 V/lux.s
- Dynamic range: 74 dB
- MAX SNR: 37 dB
- Dark Current: 62 e-/s @60℃
- Micro lens chief ray angle (CRA): 12°(linear)
- Operation Temperature: -30~85℃
- Stable Image temperature: -20~60℃
- Storage temperature: -40~125℃
- Package: CSP

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2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Description	Symbol	Rating	Unit	Note
Analogue absolute max	V_{AVDD_MAX}	-0.3~3.9	V	Refer to GND
IO absolute max	V_{IOVDD_MAX}	-0.3~3.6	V	
Digital input voltages	V_{IF_MAX}	-0.3~V_{IOVDD}+0.3	V	

Note: Digital input voltage: XCLK, SBCL, SBDA, XSHUTDOWN, FSYNC

2.2 Operation Conditions

Table 2: Operation Conditions

Description	Symbol	Min.	Typical	Max.	Unit
Analog power supply	V_{AVDD}	2.7	2.8	2.9	V
IO power supply	V_{IOVDD}	1.7	1.8	1.9	V
Digital input voltages	V_{IF}	0		IOVDD	V
Test temperature	T_{TEST}	21	25	27	℃

Note: 1. Digital input voltage: XCLK, SBCL, SBDA, XSHUTDOWN, FSYNC.
2. Test temperature: image quality test condition.

2.3 DC Characteristics

Table 3: DC Characteristics

Characteristics	Symbol	Min.	Typical	max	Unit
Input voltage HIGH	V_{IH}	0.7 x V_{IF}	-	-	V
Input voltage Low	V_{IL}	-	-	0.3 x V_{IF}	V
Output voltage HIGH	V_{OH}	0.7 x V_{IOVDD}	-	-	V
Output voltage LOW	V_{OL}	-	-	0.3 x V_{IOVDD}	V

Note: Input voltage apply to XCLK, SBCL, SBDA, XSHUTDOWN, FSYNC.

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2.4 AC Characteristics

Figure 2: AC Characteristics

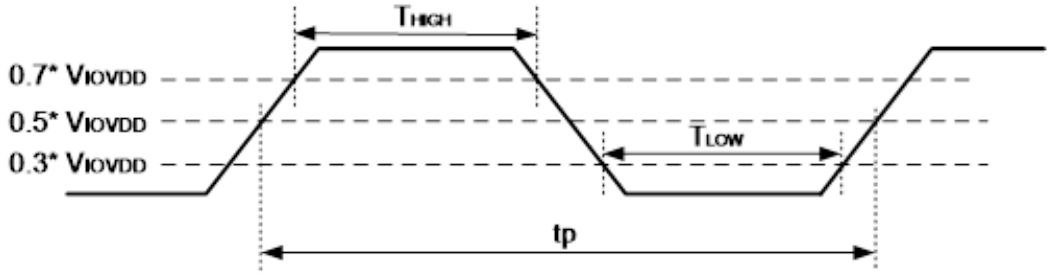

Table 4: AC Characteristics

Item	Symbol	Min.	Typ.	max	unit
Frequency	f_{SCK}	6	27	36	MHz
jitter (period, peak-to-peak)	T_{jitter}			600	ps
High level width	T_{HIGH}	0.4tp		0.6tp	ns
Low level width	T_{LOW}	0.4tp		0.6tp	ns
Duty Cycle	f_{DUTY}	40		60	%

2.5 Power Consumption

Table 5: Power Consumption

Item	Symbol	Min	Typ	Max	Unit
Full size @30fps MIPI 2lane	I_{AVDD}	-	20.93	-	mA
	I_{IOVDD}	-	38.40	-	mA
Full size @30fps DVP	I_{AVDD}	-	20.98	-	mA
	I_{IOVDD}	-	34.40	-	mA
Standby current	I_{AVDD}	-	0.1	-	μA
	I_{IOVDD}	-	82.23	-	μA
Power off current	I_{total}	-	-	0	μA

Note: 1. All operate current are measured at 27MHz XCLK.
2. Standby current is measured at XSHUTDOWN = L, XCLK=27MHz.
3. We recommend that power should be turned off, when lower power consumption is required.

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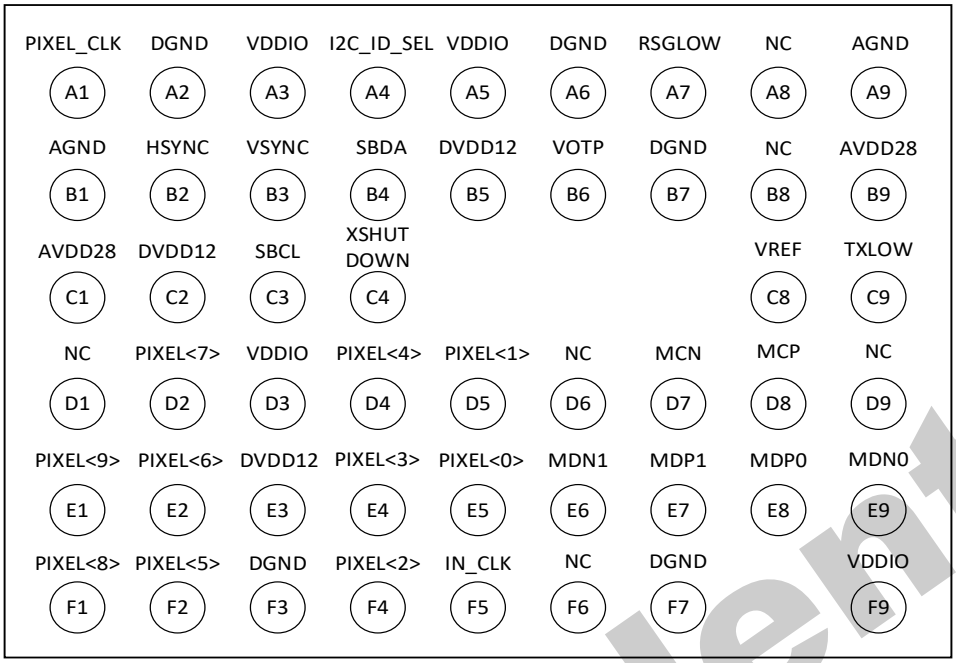
3. CSP Package Specifications

Figure 3: CSP Pin Top View



3.1 Pin Descriptions

Table 6: Pin Descriptions

Pin	Name	Type	A/D	Description
A1	PIXEL_CLK	OUTPUT	D	DVP clock
A2	DGND	GROUND	D	Ground for Digital.
A3	VDDIO	POWER	D	I/O Power supply:1.8V
A4	I2C_ID_SEL	INPUT	D	ID_SEL (floating forbidden). 0:0x6e, 1:0x7e
A5	VDDIO	POWER	D	I/O Power supply:1.8V
A6	DGND	GROUND	D	Ground for Digital.
A7	RSGLOW	POWER	A	Internal power supply.
A8	NC	NC		NC
A9	AGND	GROUND	A	Ground for analog.
B1	AGND	GROUND	A	Ground for analog.
B2	HSYNC	OUTPUT	D	DVP HSYNC.
B3	VSYNC	I/O	D	DVP VSYNC.
B4	SBDA	I/O	D	Two-wire serial bus, data.
B5	DVDD12	POWER	D	Digital power supply: 1.2V Generated by the internal regulator
B6	VOTP	POWER	D	OTP power supply: 2.8V (floating available)
B7	DGND	GROUND	D	Ground for Digital.
B8	NC	NC		NC

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Pin	Name	Type	A/D	Description
B9	AVDD28	POWER	A	Analog power supply: 2.8V
C1	AVDD28	POWER	A	Analog power supply: 2.8V
C2	DVDD12	POWER	D	Digital power supply: 1.2V Generated by the internal regulator
C3	SBCL	I/O	D	Two-wire serial bus, clock.
C4	XSHUTDOWN	INPUT	D	Sensor power down control: (floating forbidden) 0: reset & standby; 1: normal work
C5	\	\		\
C6	\	\		\
C7	\	\		\
C8	VREF	POWER	A	Internal power supply.
C9	TXLOW	POWER	A	Internal power supply.
D1	NC	NC		NC
D2	PIXEL<7>	OUTPUT	D	DVP07
D3	VDDIO	POWER	D	I/O power supply: 1.8V
D4	PIXEL<4>	OUTPUT	D	DVP04
D5	PIXEL<1>	OUTPUT	D	DVP01
D6	NC	NC		NC
D7	MCN	OUTPUT	D	MIPI clock (-).
D8	MCP	OUTPUT	D	MIPI clock (+).
D9	NC	NC		NC
E1	PIXEL<9>	OUTPUT	D	DVP09
E2	PIXEL<6>	OUTPUT	D	DVP06
E3	DVDD12	POWER	D	Digital power supply: 1.2V Generated by the internal regulator
E4	PIXEL<3>	OUTPUT	D	DVP03
E5	PIXEL<0>	OUTPUT	D	DVP00
E6	MDN1	OUTPUT	D	MIPI data <1> (-).
E7	MDP1	OUTPUT	D	MIPI data <1> (+).
E8	MDP0	OUTPUT	D	MIPI data <0> (+).
E9	MDN0	OUTPUT	D	MIPI data <0> (-).
F1	PIXEL<8>	OUTPUT	D	DVP08
F2	PIXEL<5>	OUTPUT	D	DVP05
F3	DGND	GROUND	D	Ground for Digital.
F4	PIXEL<2>	OUTPUT	D	DVP02
F5	IN_CLK	INPUT	D	Sensor input clock.
F6	NC	NC		NC
F7	DGND	GROUND	D	Ground for Digital.
F8	\	\		\
F9	VDDIO	POWER	D	I/O power supply: 1.8V

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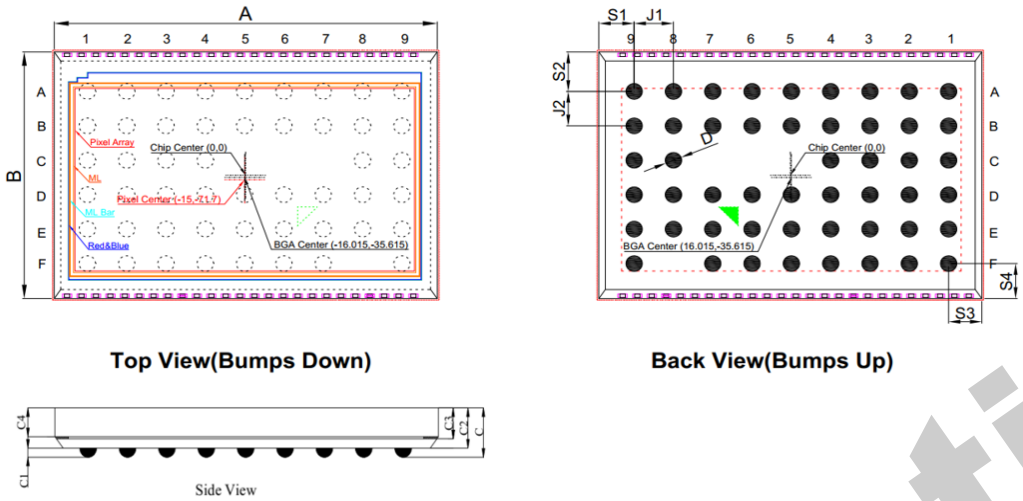
3.2 Package Specification

Figure 4: Mechanical Drawing View(μm)



Top View(Bumps Down) **Back View(Bumps Up)**

Table 7: Package Specifications

Description	symbol	Nominal	Min	Max
		Millimeters		
Package Body Dimension X	A	5.8440	5.8190	5.8690
Package Body Dimension Y	B	3.9380	3.9130	3.9630
Package Height	C	0.6500	0.5950	0.7050
Ball Height	C1	0.1300	0.1000	0.1600
Package Body Thickness	C2	0.5200	0.4850	0.5550
Thickness from top glass surface to wafer	C3	0.3450	0.3300	0.3600
Glass Thickness	C4	0.3000	0.2900	0.3100
Ball Diameter	D	0.2500	0.2200	0.2800
Total Ball Count	N	50(6NC)		
Ball Count X axis	N1	9		
Ball Count Y axis	N2	6		
Pins pitch X axis	J1	0.6000	0.5900	0.6100
Pins pitch Y axis	J2	0.5500	0.5400	0.5600
BGA ball center to package center offset in X-direction	X	0.016015	-0.0090	0.0410
BGA ball center to package center offset in Y-direction	Y	0.035615	0.0106	0.0606
BGA ball center to chip center offset in X-direction	X1	0.016015	-0.0090	0.0410
BGA ball center to chip center offset in Y-direction	Y1	0.035615	0.0106	0.0606
Edge to Pin Center Distance along X1	S1	0.538015	0.5080	0.5680
Edge to Pin Center Distance along Y1	S2	0.629615	0.5996	0.6596
Edge to Pin Center Distance along X2	S3	0.505985	0.4760	0.5360
Edge to Pin Center Distance along Y2	S4	0.558385	0.5284	0.5884

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Note: The package center, optical center, and BGA center of the chip are not coincident. If setting the package center as the origin (0, 0), the BGA center coordinate is (-16.015, -35.615), the optical center coordinate is (-15, -71.7), with μm unit

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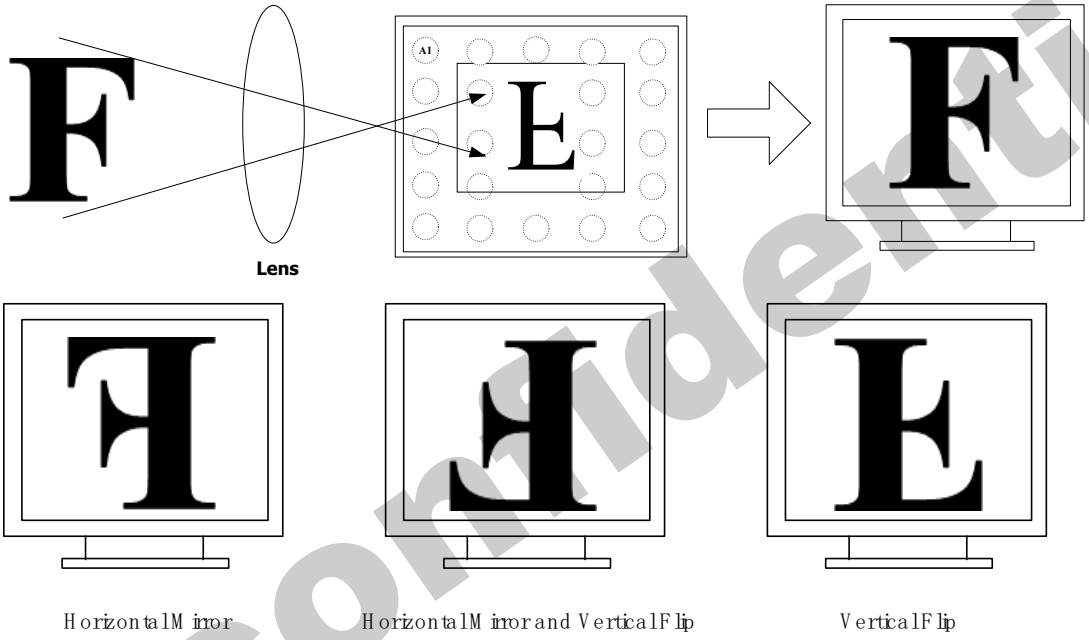
4. Optical Specifications

4.1 Readout Position

GC2083 default status is readout from the lower left corner with pin A1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so proper image output results when Pin A1 is located in the upper left corner.

Figure 5: Readout Position



Readout direction can be set by the registers.

Table 8: Mirror and Flip Information

Function	Register Address	Register Value	First Pixel
Normal	0x0015[1:0], 0x0d15[1:0]	00/00	R
Horizontal mirror	0x0015[1:0], 0x0d15[1:0]	01/01	Gr
Vertical Flip	0x0015[1:0], 0x0d15[1:0]	10/10	Gb
Horizontal Mirror and Vertical Flip	0x0015[1:0], 0x0d15[1:0]	11/11	B

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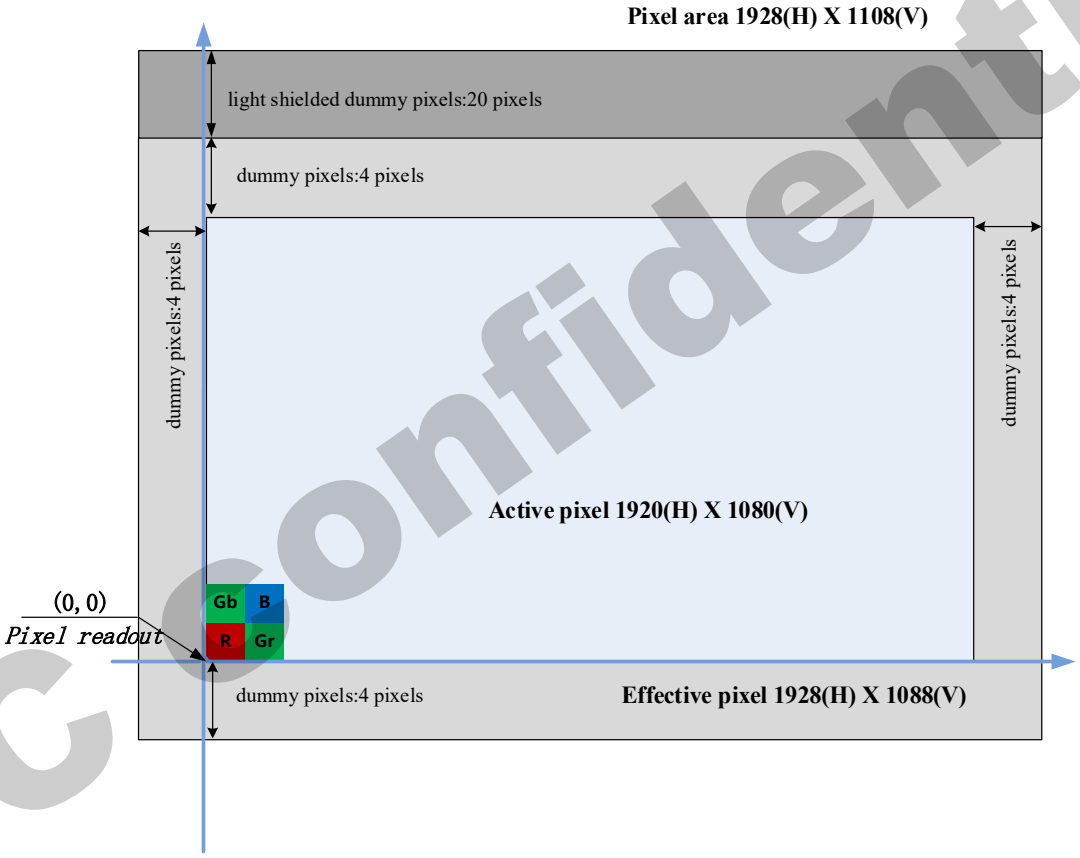
4.2 Pixel Array

Pixel array is covered by Bayer pattern color filters. The primary color GR/BG array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 1919. If flip in column, column is read out from 1919 to 0.

If no flip in row, row is read out from 0 to 1079.If flip in row, row is read out from 1079 to 0.

Figure 6: Pixel Array



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4.3 Lens Chief Ray Angle (CRA)

Figure 7 CRA Information

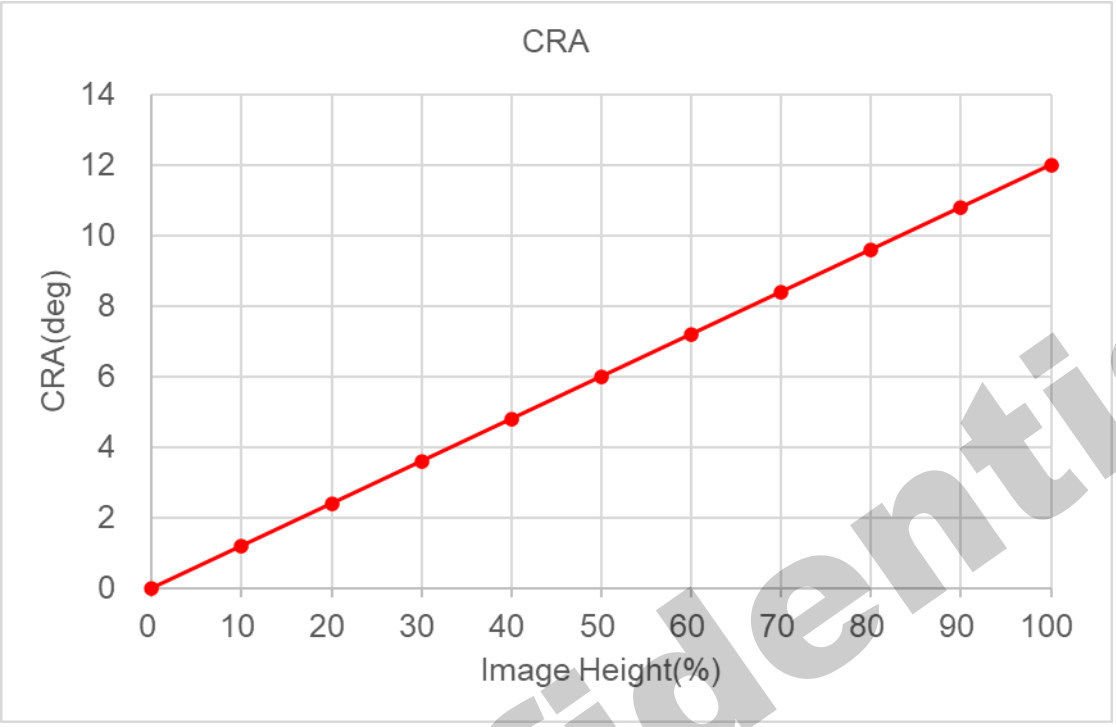

Table 9: CRA Information

Image Heigh (%)	Image Height (mm)	CRA (degree)
00	0.000	0
10	0.297	1.2
20	0.595	2.4
30	0.892	3.6
40	1.190	4.8
50	1.487	6
60	1.784	7.2
70	2.082	8.4
80	2.379	9.6
90	2.677	10.8
100	2.974	12

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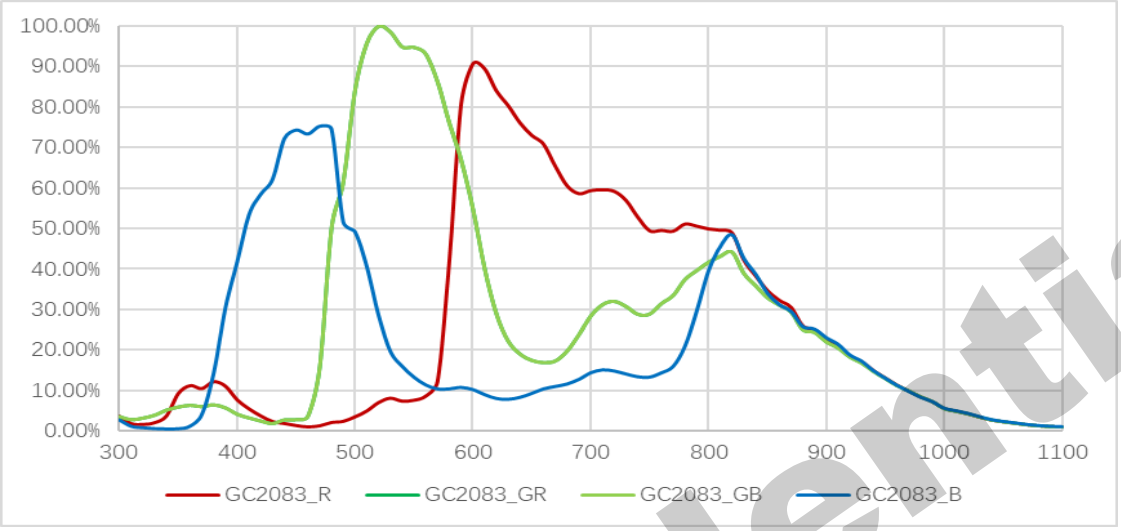
4.4 QE Spectral Characteristics

The optical spectrum of QE is below:

Figure 8 QE curve



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5. Two-wire Serial Bus Communication

GC2083 Device Address:

Table 10: Device ID

ID_SEL	Slave address write mode	Slave address read mode
0(default)	0x6e	0x6f
1	0x7e	0x7f

NOTE: When IDSEL0/IDSEL1 is “High”, it means connect to IOVDD. When IDSEL0/IDSEL1 is “Low”, you should connect it to DGND.

5.1 Protocol

The host must perform the role of a communications master and GC2083 acts as either a slave receiver or transmitter. The master must do:

- Generate the Start(S)/Stop(P) condition
- Provide the serial clock on SBCL

Figure 9: Write operate (2 bytes address –1byte data format)

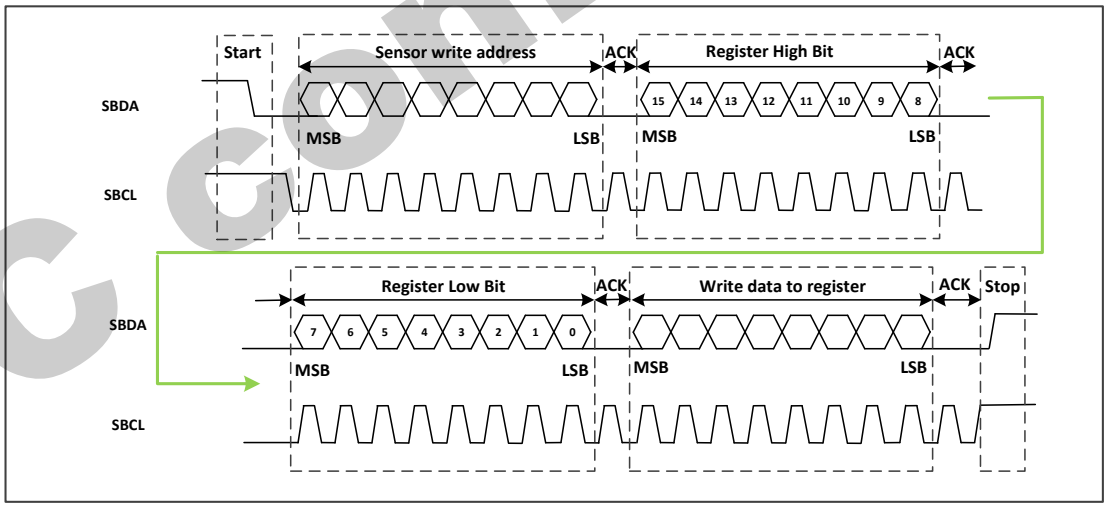

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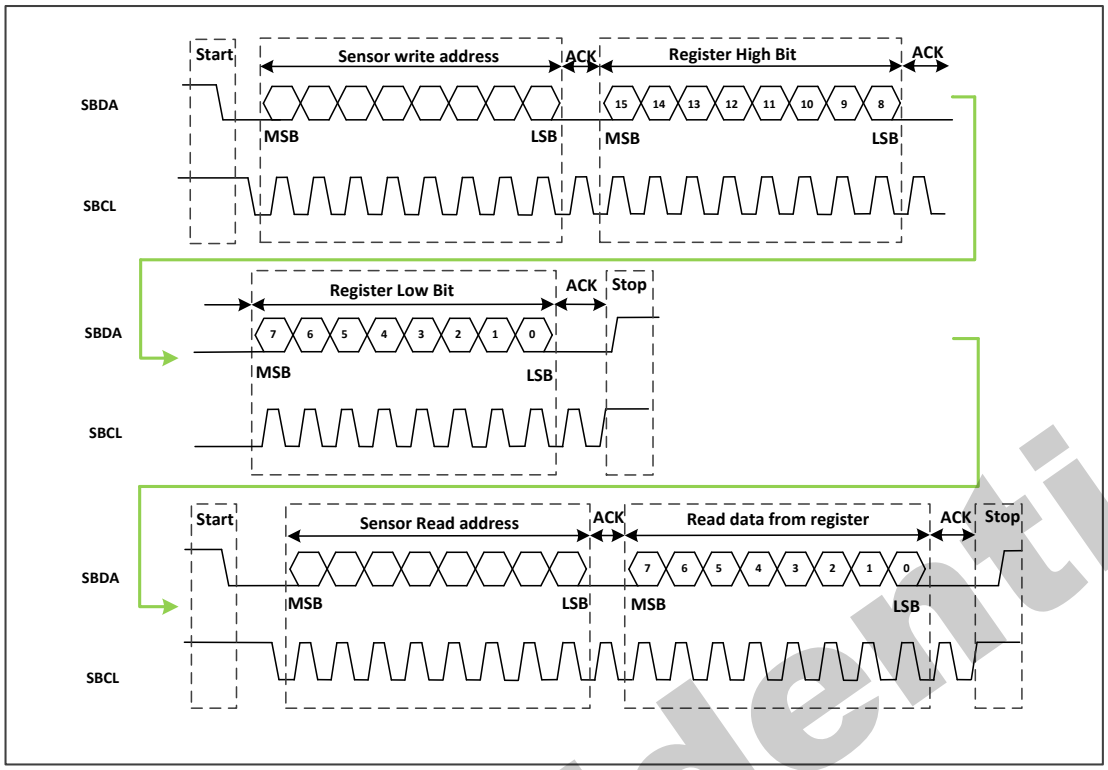
Figure 10: Read Operate (2 bytes address –1byte data format)



5.2 Serial Bus Timing

Figure 11: Serial Bus Timing

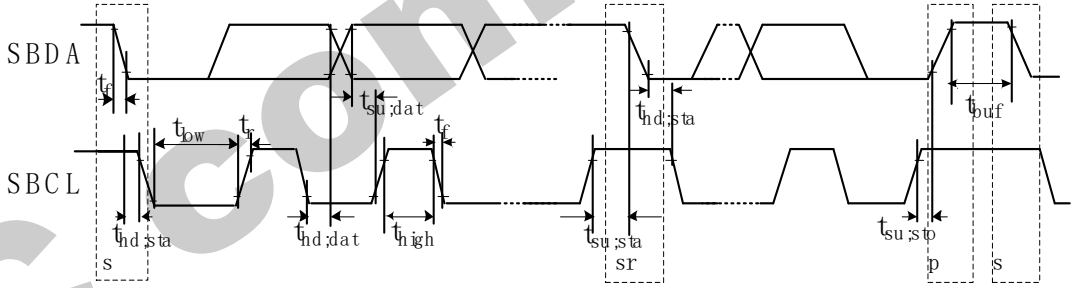


Table 11: Serial Bus Timing

Parameter	Symbol	Min	Typ.	Max	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between a stop and a start	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	600	--	--	ns
Data hold time	$t_{hd;dat}$	0	--	900	ns

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Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	100	pf

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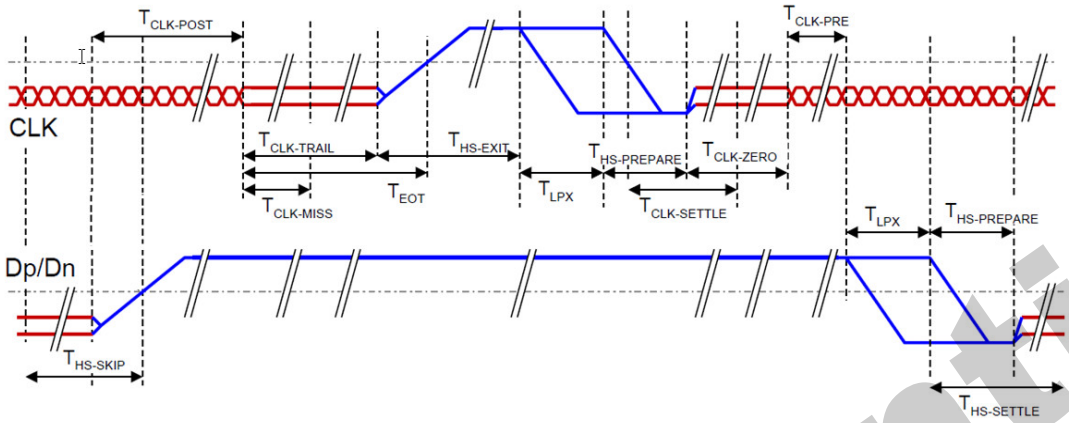
6. MIPI Timing

6.1 Clock Lane Low-power

Figure 12: MIPI Clock Lane Time



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).
  - $T_{CLK\_HS\_PREPARE}$: setting by Register 0x0222
  - T_{CLK_ZERO}: setting by Register 0x0223
  - T_{CLK_PRE}: setting by Register 0x0224
  - T_{CLK_POST}: setting by Register 0x0225
  - T_{CLK_TRAIL}: setting by Register 0x0226

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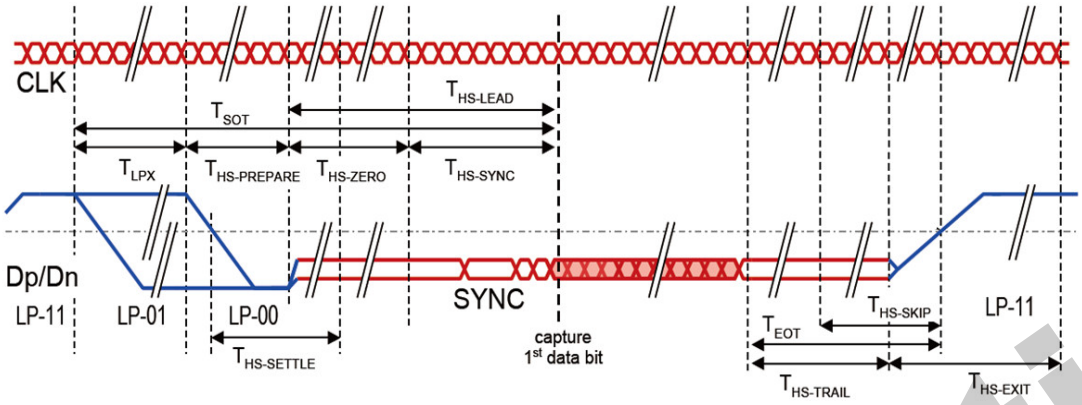
6.2 Data Burst

Figure 13: MIPI Data Lane Time

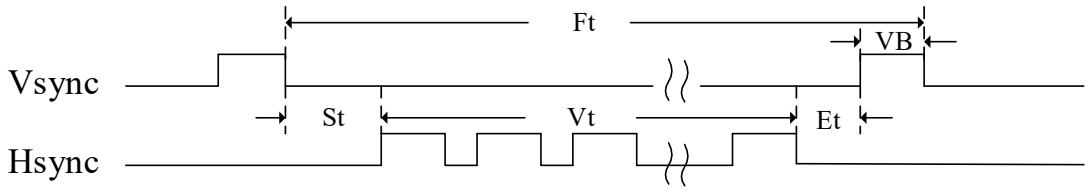


Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.
  - T_{LPX}: setting by Register 0x0221
  - $T_{HS\_PREPARE}$: setting by Register 0x0229
  - T_{HS_ZERO}: setting by Register 0x022a
  - T_{HS_TRAIL}: setting by Register 0x022b
  - T_{HS_EXIT}: setting by Register 0x0227

7. DVP Timing

Figure 14: DVP timing



Notice:

- Vsync is low active and Hsync is high active by default setting
- The output format can be RAW Bayer 10bit or 8bit

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8. Function Description

8.1 Operation Mode

Figure 15: Operation Mode

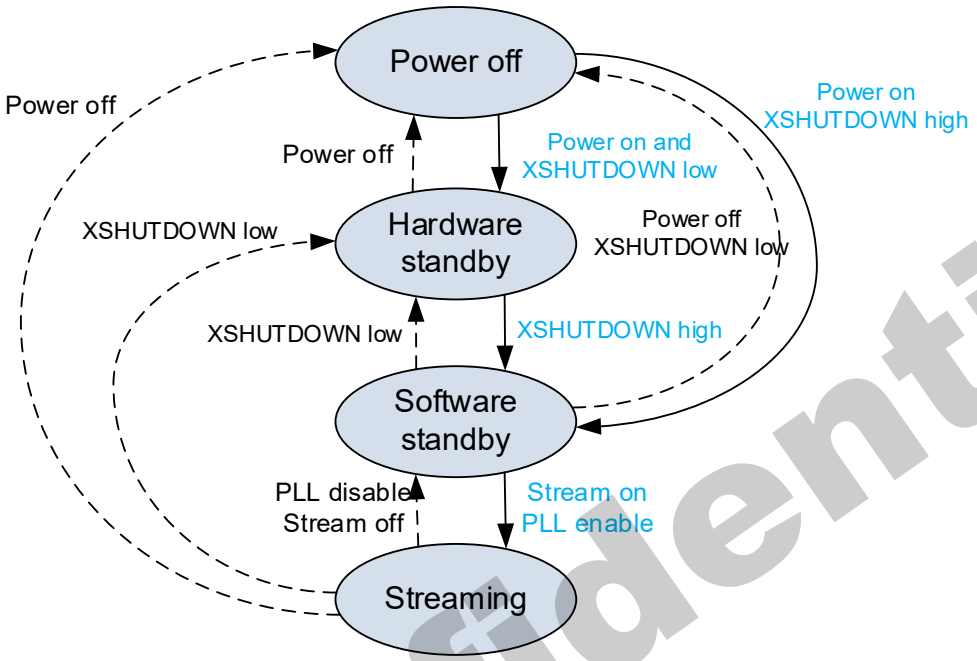

Table 12: Operate State

Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on XSHUTDOWN	XSHUTDOWN low
Software standby	Two- wire serial communication with sensor is possible, pll is ready for fast return to streaming mode	Stream mode off PLL disable XSHUTDOWN high
Streaming	Sensor is fully powered and streaming image data on the MIPI CSI-2 bus	All Pad Enabled

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8.2 Power on Sequence

Figure 16: Power on Timing

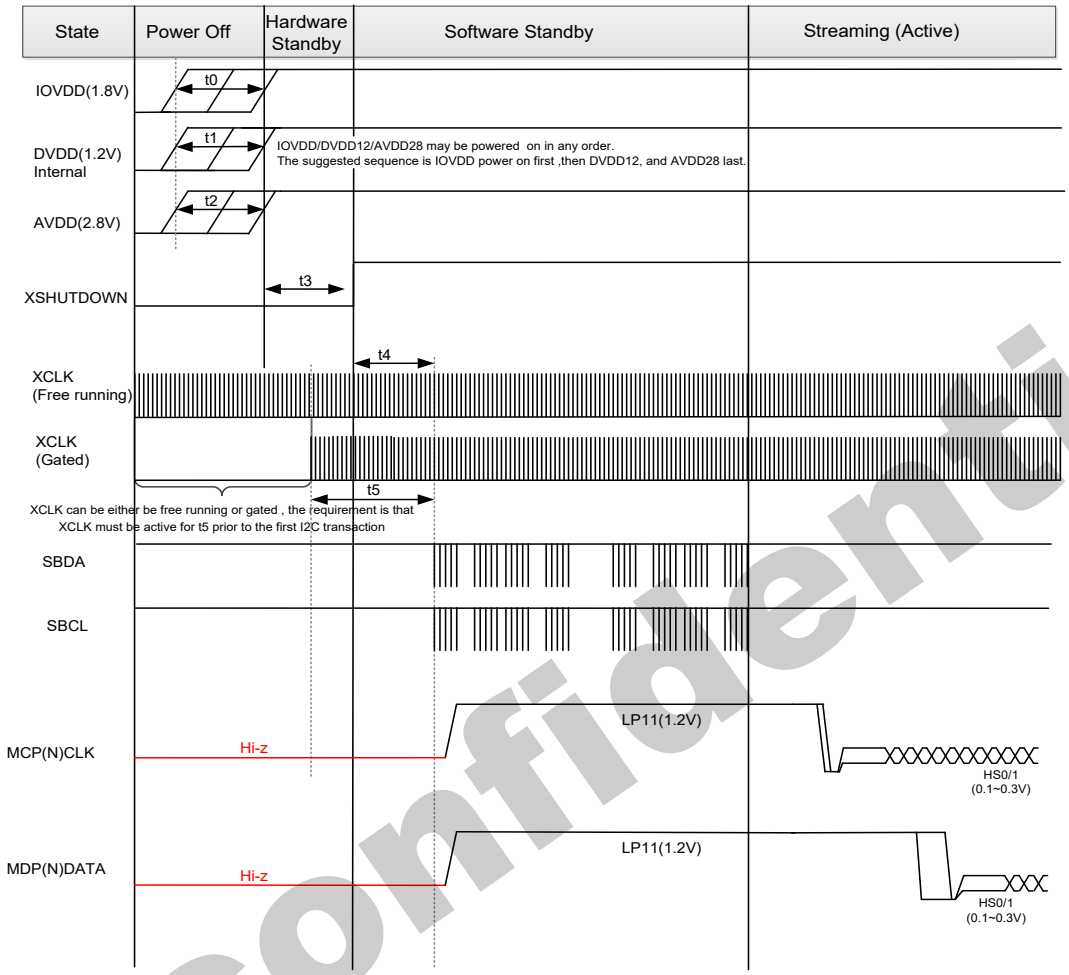

Table 13: Power on Timing

Parameter	Description	Min.	Max.	Unit
t0	IOVDD/DVDD12/AVDD28 may rise in any order. The rising separation can vary from 0μs to indefinite.	0	-	μs
t1				
t2				
t3	From power on to XSHUTDOWN pull high	0	-	μs
t4	XSHUTDOWN rising to first I2C transaction	50	-	μs
t5	Minimum No. of XCLK cycles prior to the first I2C transaction	1200	-	XCLK

Note: 1. IOVDD/DVDD12/AVDD28 may rise in any order.
2. The suggested sequence is IOVDD powered on first, then DVDD12, and AVDD28 last.
3. Register should be reloaded before works.

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8.3 Power off Sequence

Figure 17: Power off Timing

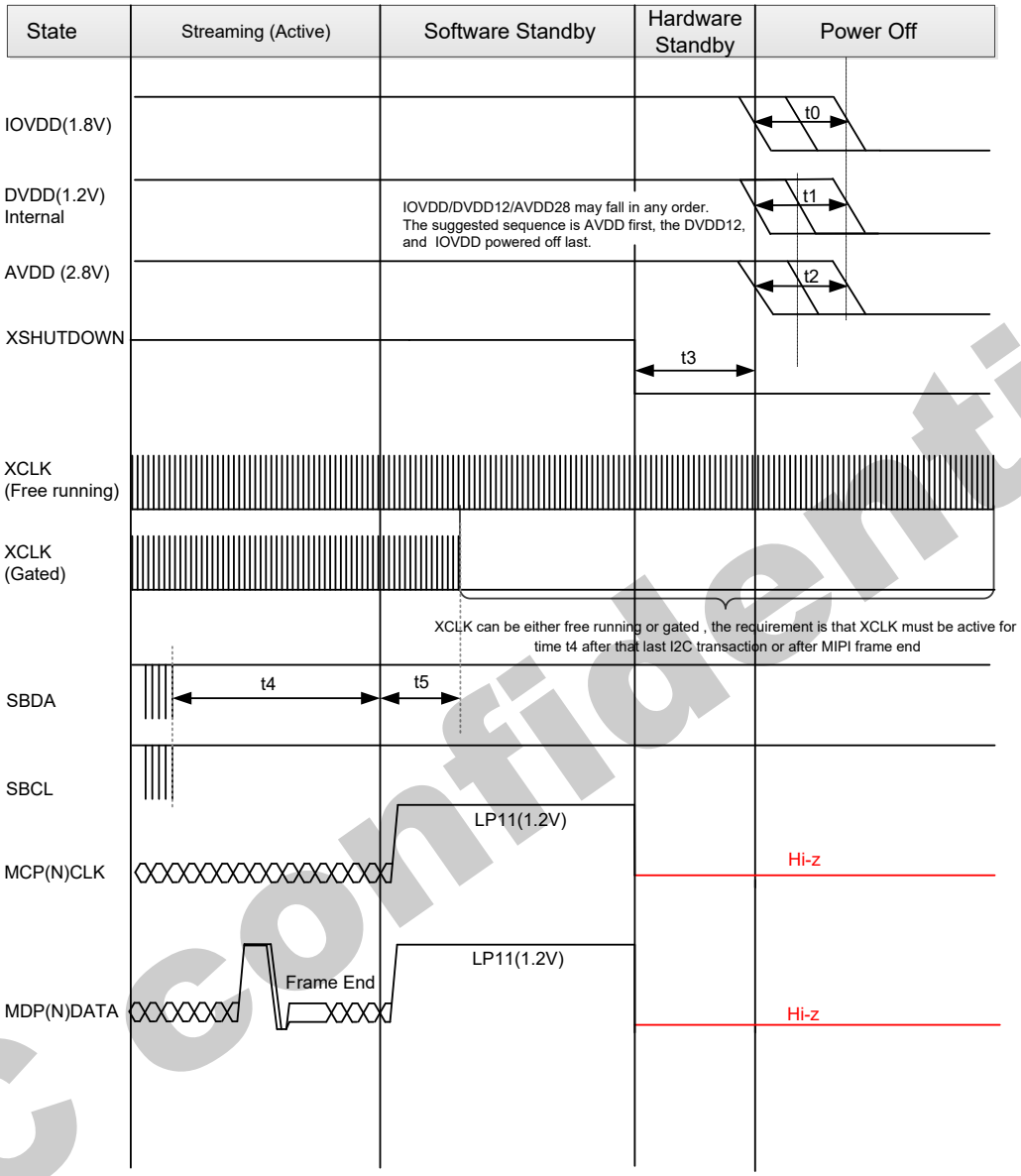

Table 14: Power off Timing

Parameter	Description	Min.	Max.	Unit
t0	IOVDD/DVDD12/AVDD28 may fall in any order. The fall separation can Vary from 0µs to indefinite.	0	-	µs
t1				
t2				
t3	From XSHUTDOWN pull down to power off	0		µs
t4	Enter Software Standby command – Device in Software Standby mode	0	-	µs

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t5	Minimum number of XCLK cycles after the last transaction or MIPI frame end code.	2000		XCLK

Note: 1. IOVDD/DVDD12/AVDD28 may fall in any order. The suggested sequence is AVDD first, the DVDD12, and IOVDD powered off last.
2. If the sensor’s power cannot be cut off, please keep power supply, then set XSHUTDOWN pin low. It will make sensor standby.
3. If the standby sequence needs to be modified, please contact FAE of *Galaxycore Inc*.

8.4 Black Level Calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

8.5 Integration Time

The integration time is controlled by the shutter time registers. When you want to set an exposure value that is bigger than the current frame length value, you should first set a new frame length and make sure that it’s bigger than the exposure value you’d like to set.

Table 15: Shutter Time Register

Addr.	Register name	Description
0x0d03	Shutter time	[5:0] shutter time[13:8]
0x0d04		[7:0] shutter time[7:0]

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8.6 Windowing

GC2083 has a rectangular pixel array 1920 x 1080, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.

Figure 18: Windowing Mode

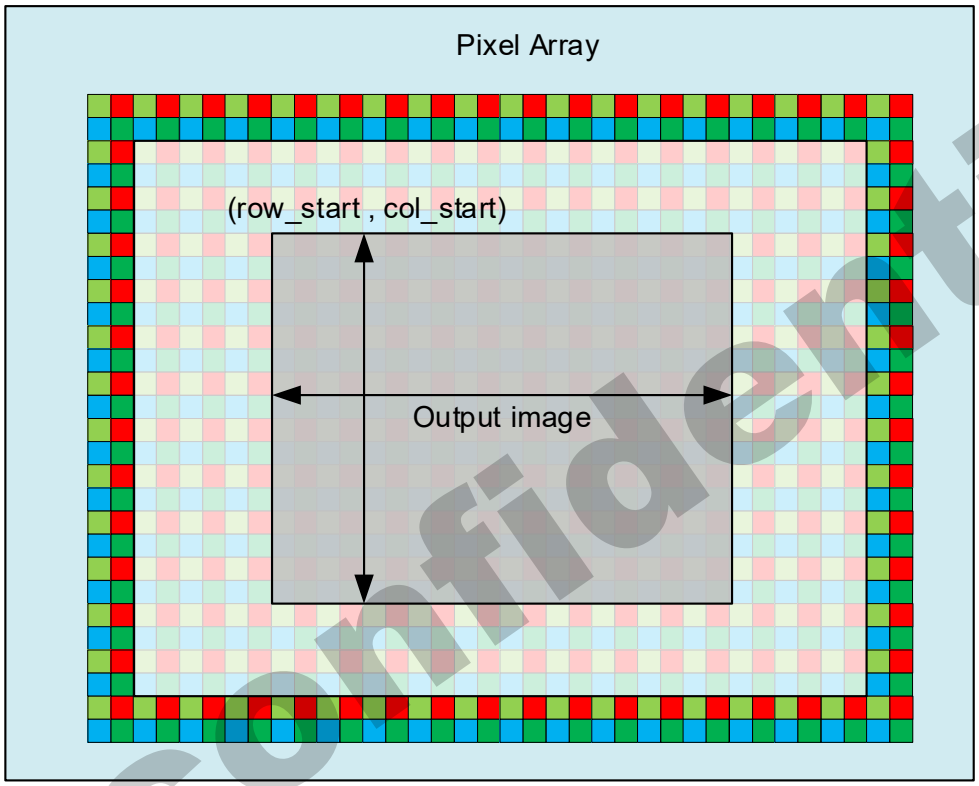

Table 16: Window Set Register

Addr.	Register name	Description
0x0d0d	win_height	[2:0]win_height[10:8]
0x0d0e		[7:0]win_height[7:0]
0x000f	win_width	[3:0]win_width[11:8]
0x0010		[7:0]win_width[7:0]
0x0d09	Row start	[2:0]row_start[10:8]
0x0d0a		[7:0]row_start [7:0]
0x000b	Col start	[2:0]col_start[10:8]
0x000c		[7:0]col_start[7:0]

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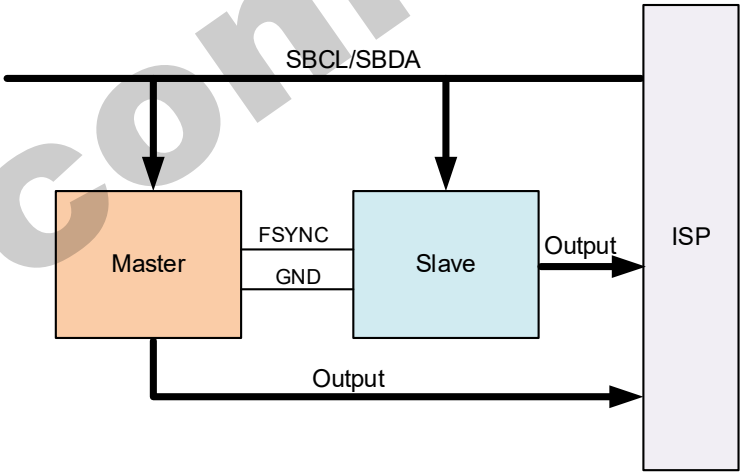
Table 17: Out Window Set Register

Addr.	Register name	Description
0x0191	out_win_y1	[3:0] out_win_y1[10:8]
0x0192		[7:0] out_win_y1[7:0]
0x0193	out_win_x1	[3:0] out_win_x1[11:8]
0x0194		[7:0] out_win_x1[7:0]
0x0195	out_win_height	[3:0] out_win_height[10:8]
0x0196		[7:0] out_win_height[7:0]
0x0197	out_win_width	[3:0] out_win_width[11:8]
0x0198		[7:0] out_win_width[7:0]

8.7 Frame Sync Mode

GC2083 can support hardware frame sync for dual camera application. It can be set both master and slave sensor. When use this mode, the two sensor’s FSYNC pin must connect to each other.

Figure 19: Frame Sync Configuration



Master Mode:

When GC2083 operates as a master device, it controls vertical synchronous timings and outputs synchronous signal called Vsync signal or Fsync signal from the FSYNC pin.

Slave Mode:

GC2083 can be worked as a slave and automatically synchronized within

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a certain VSYNC time period. It is important to control two image sensors’ rolling shutters with the same timing.

8.8 Frame Structure

Frame structure is controlled by line length, frame length, window height, window width.

Frame length control:

Frame length is controlled by window height, minimum VB and shutter time.

◆ Frame length depend shutter time.

- Minimum frame length = window height + 16 +VB (VB_min = 16)
- If shutter time < minimum frame length: Actual frame length = minimum frame length
- If shutter time > minimum frame length: Actual frame length = shutter time + 16 (recommended).

◆ Fix frame rate

- User can fix VB to fix frame rate.

Table 18: Frame Length Register

Addr.	Register name	Description
0x0d41	Frame length	[7:0] frame length[15:8]
0x0d42		[7:0] frame length[7:0]
0x0d79	Minimum VB	[7:0] min_vb[15:8]
0x0d7a		[7:0] min_vb[7:0]

Line length control:

Line length control for internal set, and not recommended to be modified.

Table 19: Line Length Register

Addr.	Register name	Description
0x0d05	Line length	[3:0] Line length[11:8]
0x0d06		[7:0] Line length[7:0]

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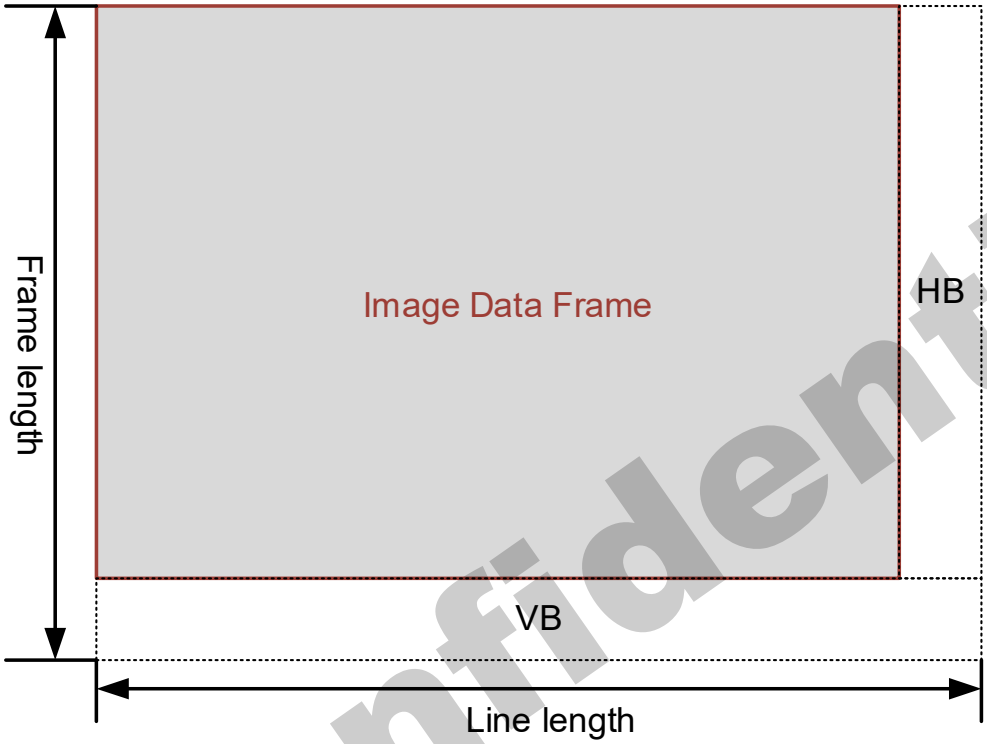
Blank time control:

Line blank time is controlled by line length.

Frame blank time = frame length – out window height

Figure 20: Frame Structure



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9. Register List

System Register:

Address	Name	Default	R/W	Description
0x03f0	Sensor_ID_HIGH	0x20	RO	Sensor_ID
0x03f1	Sensor_ID_LOW	0x83	RO	Sensor_ID

Analog & CISCTL:

Address	Name	Default	R/W	Description
0x0d03	Exposure[13:8]	0x00	RW	[5:0] Exposure[13:8]
0x0d04	Exposure[7:0]	0x10	RW	[7:0] Exposure[7:0]
0x0d05	CISCTL_hb[13:8]	0x08	RW	[5:0] CISCTL_hb[13:8]
0x0d06	CISCTL_hb[7:0]	0x98	RW	[7:0] CISCTL_hb[7:0]
0x0d07	CISCTL_vb[13:8]	0x00	RW	[5:0] CISCTL_vb[13:8]
0x0d08	CISCTL_vb[7:0]	0x10	RW	[7:0] CISCTL_vb[7:0]
0x0d09	CISCTL_row_start[10:8]	0x00	RW	[2:0] CISCTL_row_start[10:8]
0x0d0a	CISCTL_row_start[7:0]	0x02	RW	[7:0] CISCTL_row_start[7:0]
0x000b	CISCTL_col_start [10:8]	0x00	RW	[2:0] CISCTL_col_start [10:8]
0x000c	CISCTL_col_start [7:0]	0x00	RW	[7:0] CISCTL_col_start [7:0]
0x0d0d	CISCTL_win_height[10:8]	0x05	RW	[2:0] CISCTL_win_height[10:8]
0x0d0e	CISCTL_win_height[7:0]	0x18	RW	[7:0] CISCTL_win_height[7:0]
0x000f	CISCTL_win_width[11:8]	0x09	RW	[3:0] CISCTL_win_width[11:8]
0x0010	CISCTL_win_width[7:0]	0x0c	RW	[7:0] CISCTL_win_width[7:0]
0x0d41	Framelength[13:8]	0x05	RW	[5:0] Framelength_high[13:8]
0x0d42	Framelength[7:0]	0x3c	RW	[7:0] Framelength_low[7:0]
0x0d79	min_vb[13:8]	0x00	RW	
0x0d7a	min_vb[7:0]	0x10	RW	
0x0d13	CISCTL_vs_st	0x10	RW	vs_st
0x0d14	CISCTL_vs_et	0x04	RW	vs_et

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CSI/PHY1.0

Address	Name	Default	R/W	Description
0x0201	DPHY_analog_mode1	0x20	RW	[7] disable_set[1] [6:5] clkctr [4] NA [3] disable_set[0] [2] phy-lane1_en [1] phy_lane0_en [0] phy_clk_en
0x0202	DPHY_analog_mode2	0x16	RW	[7:6] data1ctr [5:4] data0ctr [3:0] mipi_diff
0x0203	DPHY_analog_mode3	0xca	RW	[7] clklane_p2s_sel [6:5] data0hs_ph [4] data0delay1s [3] clkdelay1s [2] mipi_en [1:0] clkhs_ph
0x0211	LDI_set	0x2b	RW	[7:0] LDI_set [7:6] vc_id [5:4] data type raw10/8
0x0212	LWC_set[15:8]	0x0b	RW	[7:0] LWC_set_1
0x0213	LWC_set[7:0]	0x40	RW	[7:0] LWC_set_2
0x0214	SYNC_set	0xb8	RW	[7:0] SYNC_set
0x0215	DPHY_mode	0x10	RW	[7] NA [6] mipi para invar when div2 [5] DATA lane gate [4] all_lane_open_mode [3:2] switch_msb_mode [1:0] clklane_mode
0x0216	LP_set	0x29	RW	[7:6] hi-z [5:4] use define
0x0220	T_init_set	0x80	RW	[7:0] T_init_set
0x0221	T_LPX_set	0x10	RW	[7:0] T_LPX_set
0x0222	T_CLK_HS_PREPARE_set	0x05	RW	[7:0] T_CLK_HS_PREPARE_set
0x0223	T_CLK_zero_set	0x20	RW	[7:0] T_CLK_zero_set
0x0224	T_CLK_PRE_set	0x02	RW	[7:0] T_CLK_PRE_set
0x0225	T_CLK_POST_set	0x20	RW	[7:0] T_CLK_POST_set
0x0226	T_CLK_TRAIL_set	0x08	RW	[7:0] T_CLK_TRAIL_set
0x0227	T_HS_exit_set	0x10	RW	[7:0] T_HS_exit_set
0x0228	T_wakeup_set	0xa0	RW	[7:0] T_wakeup_set

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0x0229	T_HS_PREPARE_set	0x06	RW	[7:0] T_HS_PREPARE_set
0x022a	T_HS_Zero_set	0x0a	RW	[7:0] T_HS_Zero_set
0x022b	T_HS_TRAIL_set	0x08	RW	[7:0] T_HS_TRAIL_set
0x0236	clklp_drv	0x00	RW	[1:0] clklp_drv
0x0237	lp_drv	0x00	RW	[3:2] data1lp_drv [1:0] data0lp_drv
0x023e	CSI2_mode	0x48	RW	[7] lane_ena [6] DVPBUF_ena [5] ULPEna [4] MIPI_ena [3] mipi_set_auto_enable [2] RAW8_mode [1] line_sync_mode [0] double_lane_en
0x0290	dvp_out_mode	0x00	RW	[7] o_vsync_pola [6] o_hsync_pola [5] OUT_gate_mode [4] hsync_delay_half_pclk [3] data_delay_half_pclk [2] vsync_polarity [1] hsync_polarity [0] pclk_out_polarity

OUT

Address	Name	Default	R/W	Description
0x018c	Test image	0x10	RW	[2] input test image
0x0191	out_win_y1[10:8]	0x00	RW	[2:0] out_win_y1
0x0192	out_win_y1[7:0]	0x00	RW	Out_win_y1
0x0193	out_win_x1[11:8]	0x00	RW	[3:0]out_win_x1
0x0194	Out_win_x1[7:0]	0x00	RW	out_win_x1
0x0195	Out_win_height[10:8]	0x04	RW	[2:0] out_win_helght[10:8]
0x0196	Out_win_height[7:0]	0x38	RW	out_win_helght[7:0]
0x0197	Out_win_width[11:8]	0x07	RW	[3:0]out_win_width[11:8]
0x0198	Out_win_width[7:0]	0x38	RW	Out_win_width[7:0] must be 8X when raw10
0x0199	Out_win_offset	0x05	RW	[3:0] Out_win_offset for auto_updown[3:2] out_offset_y1=2 for auto_mirror[1:0] out_offset_x1=2

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OB OFFSET

Address	Name	Default	R/W	Description
0x0170	WB_offset_G1	0x40	RW	WB_offset_G1
0x0171	WB_offset_R1	0x40	RW	WB_offset_R1
0x0172	WB_offset_B1	0x40	RW	WB_offset_B1
0x0173	WB_offset_G2	0x40	RW	WB_offset_G2

Gain

Address	Name	Default	R/W	Description
0x00b1	auto_pregain_sync[9:6]	0x01	RW	[7:4] NA [3:0] Auto_pregain[9:6]
0x00b2	auto_pregain[5:0]	0x00	RW	[7:2] Auto_pregain[5:0] [1:0]NA
0x00d0	Analog_PGA_gain[7:0]	0x00	RW	analog_gain
0x0dc1	Analog_PGA_gain[8]	0x00	RW	
0x00b8	Col_gain[11:6]	0x00	RW	[7:6]NA [5:0]col_gain[11:6]
0x00b9	Col_gain[5:0]	0x00	RW	[7:6]NA [5:0]col_gain[5:0]
0x007a	Global gain	0x40	RW	[7:6] global gain

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