



# 1/2.7-Inch 2.1Mp/Full HD Digital Image Sensor

## AR0230CS Data Sheet, Rev. 2

For the latest data sheet, refer to Aptina's Web site: [www.aptina.com](http://www.aptina.com)

### Features

- Superior low-light performance
- Latest 3.0µm pixel with Aptina™ DR-Pix™ technology with Dual conversion Gain
- Full HD support at up to 1080P 60fps for superior video performance
- Linear or high dynamic range capture
- Optional adaptive local tone mapping (ALTM)
- Pixel or Line interleaved T1/T2 output
- Support for external mechanical shutter
- On-chip phase-locked loop (PLL) oscillator
- Integrated position-based color and lens shading correction
- Slave mode for precise frame-rate control
- Stereo/3D camera support
- Statistics engine
- Data interfaces: four-lane serial high-speed pixel interface (HiSPi™) differential signaling (SLVS and HiVCM), or parallel
- Auto black level calibration
- High-speed configurable context switching
- Temperature sensor

### Applications

- Video surveillance
- 1080p60 (Surveillance) video applications
- High dynamic range imaging

### General Description

Aptina's AR0230CS is a 1/2.7-inch CMOS digital image sensor with an active-pixel array of 1928Hx1088V. It captures images in either linear or high dynamic range modes, with a rolling-shutter readout. It includes sophisticated camera functions such as in-pixel binning, windowing and both video and single frame modes. It is designed for both low light and high dynamic range scene performance. It is programmable through a simple two-wire serial interface. The AR0230CS produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including surveillance and HD video.

**Table 1: Key Parameters**

Parameter		Typical Value
Optical format		1/2.7-inch (6.6 mm)
Active pixels		1928(H) x 1088(V) (16:9 mode)
Pixel size		3.0µm x 3.0 µm
Color filter array		RGB Bayer
Shutter type		Electronic rolling shutter and GRR
Input clock range		6 – 48 MHz
Output clock maximum		148.5 Mp/s (4-lane HiSPi) 74.25 Mp/s (Parallel)
Output	Serial	HiSPi 10-, 12-, 14-, 16-, or 20-bit
	Parallel	10-, 12-bit
Frame rate	1080p	60 fps
Responsivity		4.0V/lux-sec
SNR <sub>MAX</sub>		41 dB
Max Dynamic range		Up to 105 dB
Supply voltage	I/O	1.8 or 2.8V
	Digital	1.8 V
	Analog	2.8 V
	HiSPi	0.3V - 0.6V (SLVS), 1.7V - 1.9V (HiVcm)
Power consumption (typical)		<896mW(HDR 1080p60, 8x gain, 25°C)
Operating temperature		-30°C to +85°C ambient
Package options		10x10mm 80-pin iBGA

### Ordering Information

**Table 2: Available Part Numbers**

Part Number	Description
AR0230CSSC00SUEA-E	80-pin iBGA, 0° CRA
AR0230CSSC00SUEAH-E	80-pin iBGA, Headboard 0° CRA
AR0230CSSC00SUEAD3-E	80-pin iBGA, Demo kit 0° CRA

## Table of Contents

Features.....	1
Applications .....	1
General Description .....	1
Ordering Information.....	1
General Description .....	5
Functional Overview.....	6
Pixel Data Format .....	12
Pixel Array Structure .....	12
Default Readout Order .....	13
Features Overview.....	14
3.0mm Dual Conversion Gain Pixel .....	14
HDR.....	14
Resolution .....	14
Frame Rate.....	14
Image Acquisition Mode.....	14
Embedded Data and Statistics.....	15
Multi-Camera Synchronization .....	15
Slave Mode.....	15
Context Switching and Register Updates .....	15
Motion Compensation/DLO .....	16
Tone Mapping.....	16
Adaptive Color Difference (ADACD) Noise Filtering .....	17
Fast Mode Switch (Combi Mode)	17
Analog/Digital Gains .....	17
Skipping/Binning Modes .....	17
Clocking Options .....	17
Temperature Sensor .....	18
Silicon / Firmware / Sequencer Revision Information .....	18
Lens Shading Correction .....	18
Companding .....	18
Compression .....	18
Packaging.....	18
Parallel Interface.....	18
High Speed Serial Pixel (HiSPi) Interface .....	19
Sensor Control Interface.....	19
T1/T2 Line Interleaved Mode .....	19
Electrical Specifications.....	21
Two-Wire Serial Register Interface.....	21
I/O Timing .....	22
DC Electrical Characteristics .....	24
HiSPi Electrical Specifications.....	28
Power-On Reset and Standby Timing.....	29
Power-Up Sequence .....	29
Power-Down Sequence.....	31
Package Diagrams.....	32
Revision History.....	33



## List of Figures

Figure 1:	Block Diagram of AR0230CS.....	6
Figure 2:	Typical Configuration: Serial Four-Lane HiSPi Interface .....	7
Figure 3:	Typical Configuration: Parallel Pixel Data Interface.....	8
Figure 4:	80-Ball IBGA Package.....	9
Figure 5:	Pixel Array Description .....	12
Figure 6:	Pixel Color Pattern Detail (Top Right Corner) .....	13
Figure 7:	Imaging a Scene .....	13
Figure 8:	Quantum Efficiency .....	20
Figure 9:	Two-Wire Serial Bus Timing Parameters.....	21
Figure 10:	I/O Timing Diagram.....	22
Figure 11:	Power Up .....	29
Figure 12:	Power Down.....	31
Figure 13:	80iBGA 10x10 Package Diagram .....	32

**List of Tables**

Table 1:	Key Parameters .....	1
Table 2:	Available Part Numbers.....	1
Table 3:	Pin Descriptions, 80-ball iBGA.....	10
Table 4:	List of Configurable Registers for Context A and Context B .....	16
Table 5:	Two-Wire Serial Bus Characteristics .....	21
Table 6:	I/O Timing Characteristics .....	23
Table 7:	DC Electrical Characteristics .....	24
Table 8:	Absolute Maximum Ratings .....	24
Table 9:	Operating Current Consumption in Parallel Output and Linear Mode .....	25
Table 10:	Operating Current Consumption in Parallel Output and HDR Mode .....	25
Table 11:	Operating Current in HiSPi (HiVCM) Output and Linear Mode .....	26
Table 12:	Operating Current in HiSPi (HiVCM) Output and HDR Mode.....	26
Table 13:	Operating Current in HiSPi (SLVS) Output and Linear Mode.....	27
Table 14:	Operating Current in HiSPi (SLVS) Output and HDR Mode .....	27
Table 15:	Channel Skew .....	28
Table 16:	Power-Up Sequence.....	29
Table 17:	Power-Down Sequence.....	31

## General Description

The Aptina AR0230CS can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 1080p-resolution image at 60 frames per second (fps) through the HiSPi port. In linear mode, it outputs 12-bit or 10-bit A-Law compressed raw data, using either the parallel or serial (HiSPi) output ports. In high dynamic range mode, it outputs 12-bit compressed data using parallel output. In HiSPi mode, 12- or 14-bit compressed, or 16-bit linearized data may be output. The device may be operated in video (master) mode or in single frame trigger mode.

FRAME\_VALID and LINE\_VALID signals are output on dedicated pins, along with a synchronized pixel clock in parallel mode.

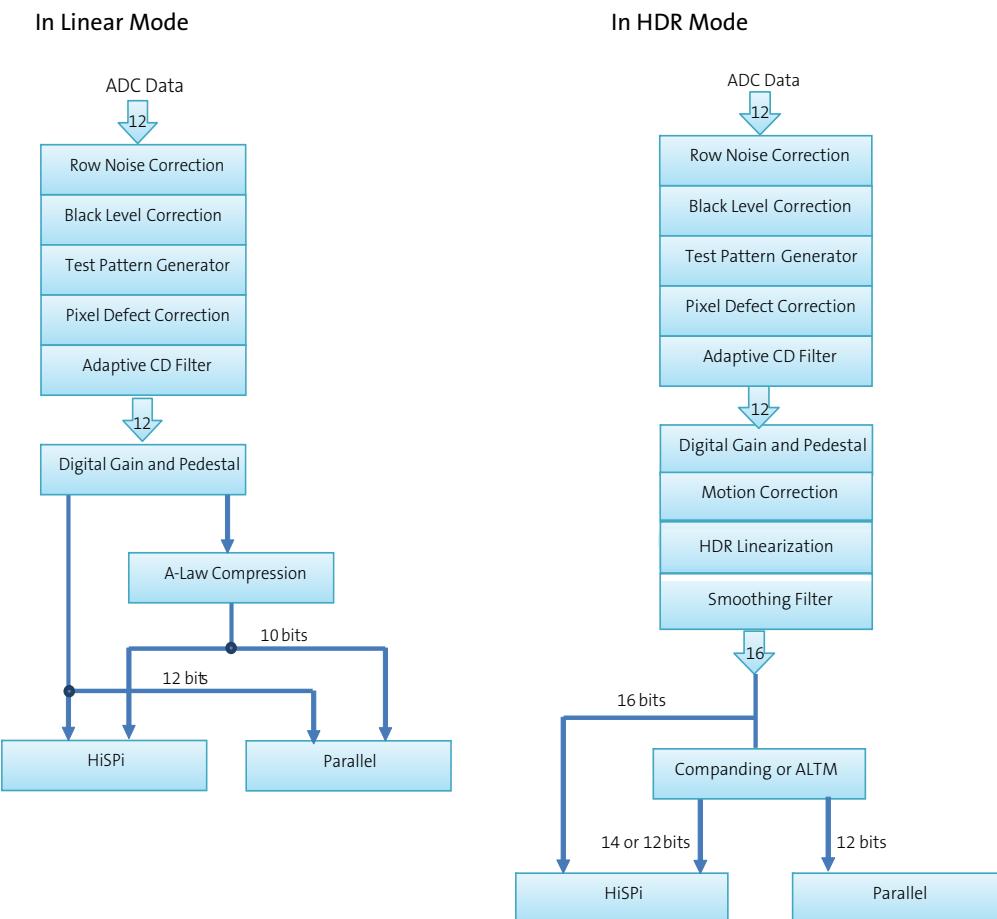
The AR0230CS includes additional features to allow application-specific tuning: windowing and offset, auto black level correction, and on-board temperature sensor. Optional register information and histogram statistic information can be embedded in the first and last 2 lines of the image frame.

The sensor is designed to operate over a wide temperature range, and is available in either a surveillance option (-30°C to +85°C ambient) or an automotive option (-40°C to +105°C ambient).

## Functional Overview

The AR0230CS is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 48 MHz. The maximum output pixel rate is 148.5 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor configured in linear mode, and in HDR mode.

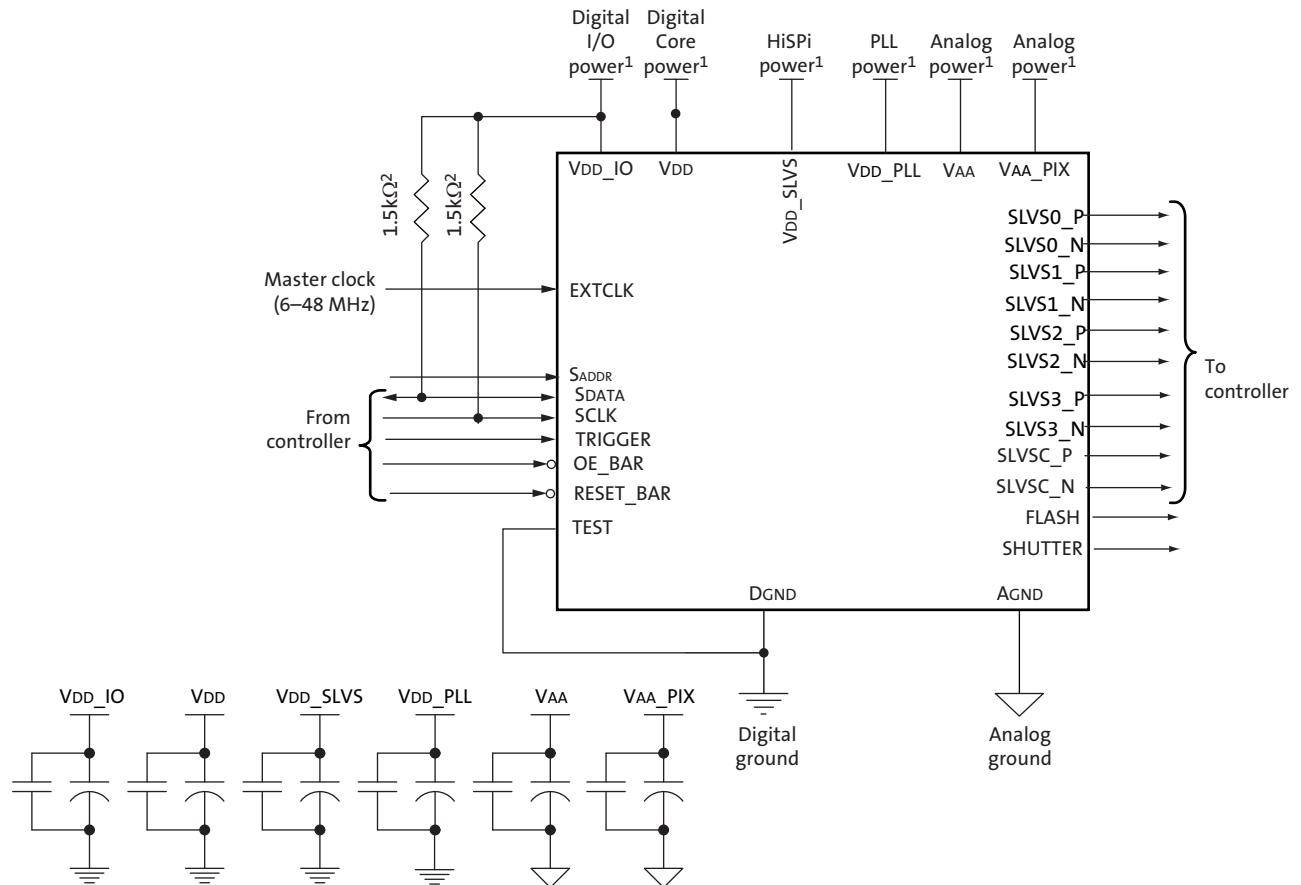
**Figure 1: Block Diagram of AR0230CS**



User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 2.1 Mp Active- Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which

provides further data path corrections and applies digital gain). The sensor also offers a high dynamic range mode of operation where multiple images are combined on-chip to produce a single image at 16-bit per pixel value. A compression mode is further offered to allow the 16 bits per pixel to be transmitted to the host system as a 12-bit value with close to zero loss in image quality.

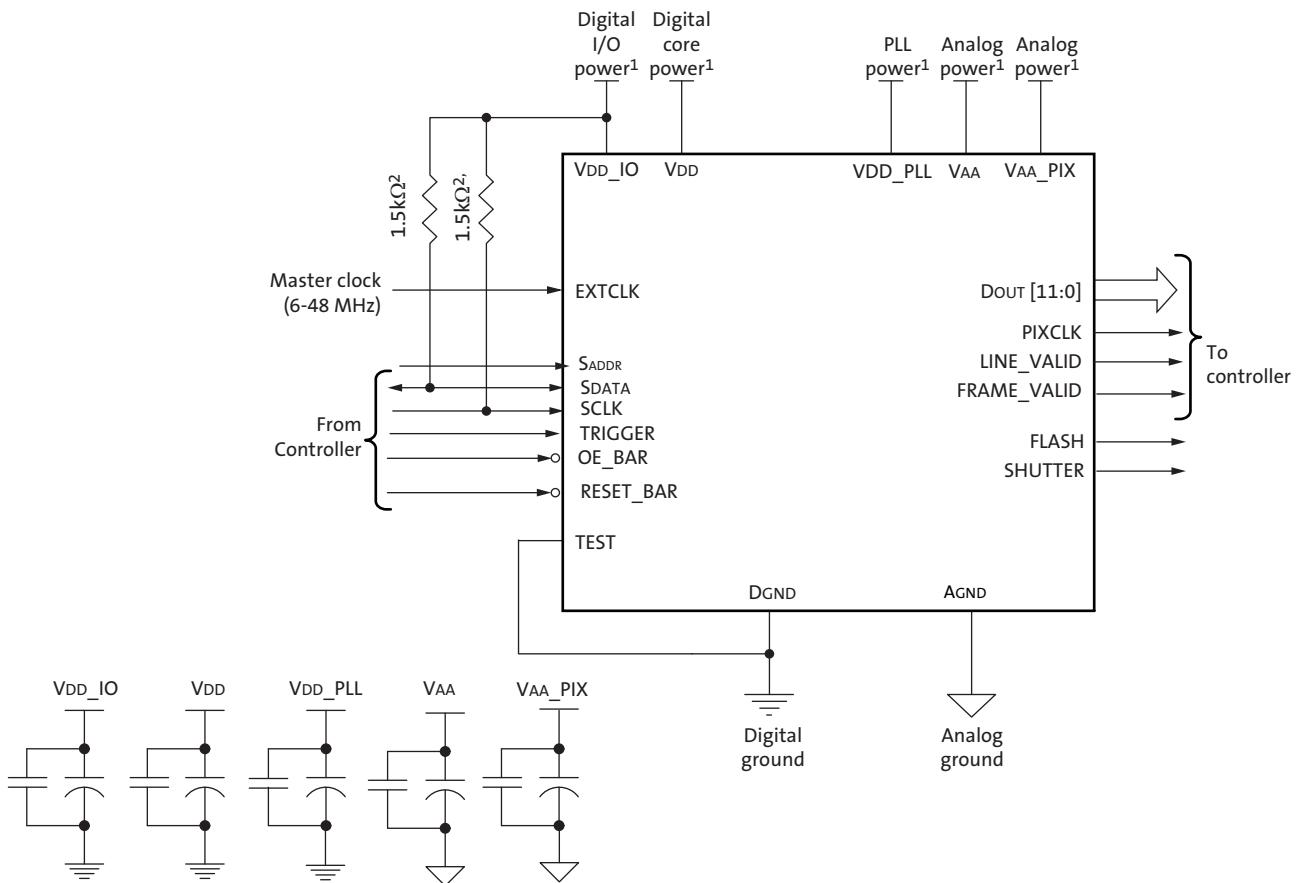
**Figure 2: Typical Configuration: Serial Four-Lane HiSPi Interface**



**Notes:**

1. All power supplies must be adequately decoupled.
2. Aptina recommends a resistor value of  $1.5\text{k}\Omega$ , but a greater value may be used for slower two-wire speed.
3. The parallel interface output pads can be left unconnected if the serial output interface is used.
4. Aptina recommends that  $0.1\mu\text{F}$  and  $10\mu\text{F}$  decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0230CS demo headboard schematics for circuit recommendations.
5. Aptina recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match **VDD\_IO** voltage to minimize any leakage currents.

Figure 3: Typical Configuration: Parallel Pixel Data Interface



## Notes:

1. All power supplies must be adequately decoupled.
2. Aptina recommends a resistor value of  $1.5k\Omega$ , but a greater value may be used for slower two-wire speed.
3. The serial interface output pads and  $V_{DDSLVS}$  can be left unconnected if the parallel output interface is used.
4. Aptina recommends that  $0.1\mu F$  and  $10\mu F$  decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0230CS demo headboard schematics for circuit recommendations.
5. Aptina recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match  $V_{DD\_IO}$  voltage to minimize any leakage currents.
7. The  $EXTCLK$  input is limited to 6-48 MHz.

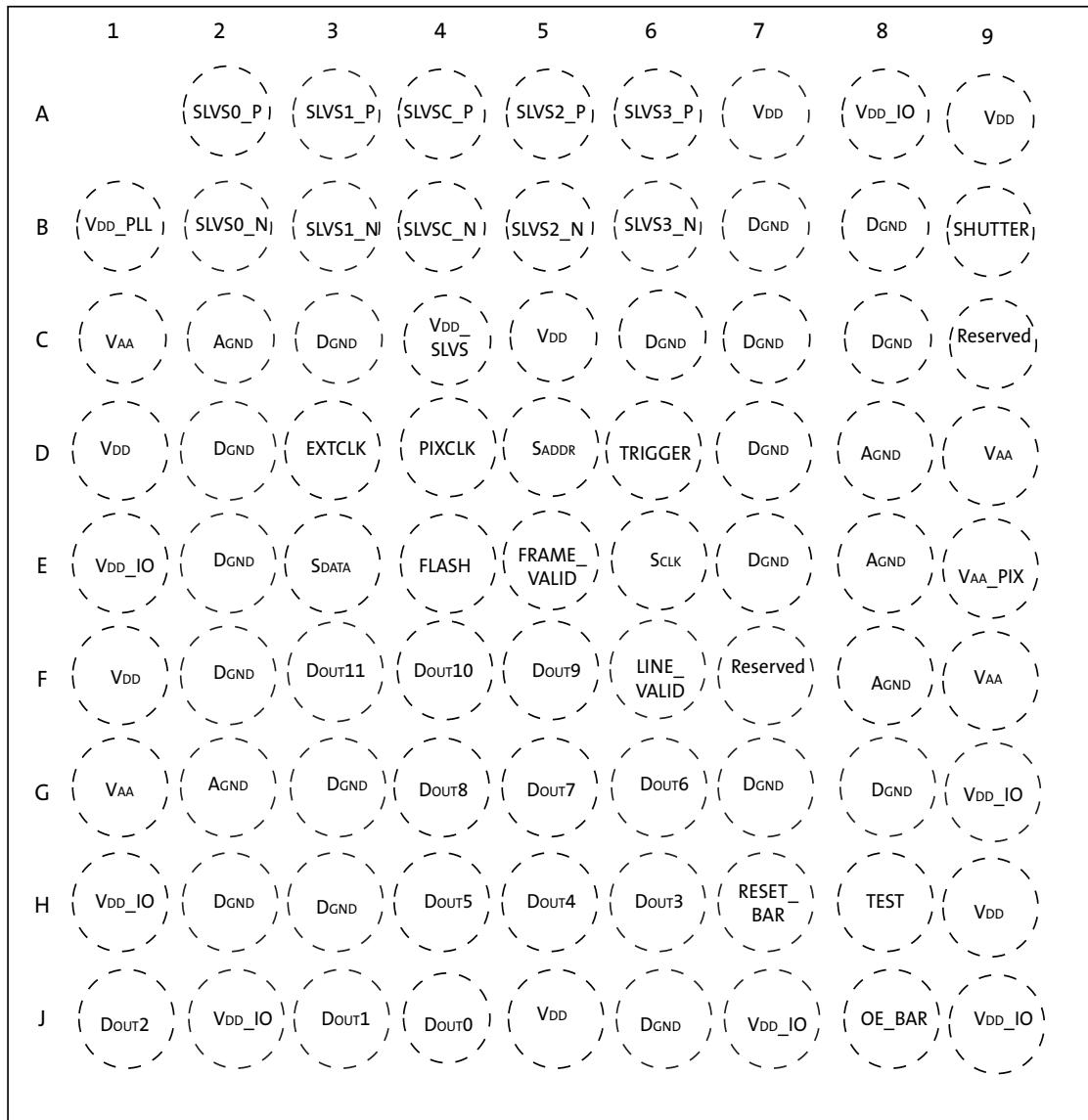
**Figure 4: 80-Ball IBGA Package****Top View  
(Ball Down)**



Table 3: Pin Descriptions, 80-ball iBGA

Name	iBGA Pin	Type	Description
SLVS0_P	A2	Output	HiSPi serial data, lane 0, differential P.
SLVS1_P	A3	Output	HiSPi serial data, lane 1, differential P.
SLVSC_P	A4	Output	HiSPi serial DDR clock differential P.
SLVS2_P	A5	Output	HiSPi serial data, lane 2, differential P.
SLVS3_P	A6	Output	HiSPi serial data, lane 3, differential P.
VDD_PLL	B1	Power	PLL power.
SLVS0_N	B2	Output	HiSPi serial data, lane 0, differential N.
SLVS1_N	B3	Output	HiSPi serial data, lane 1, differential N.
SLVSC_N	B4	Output	HiSPi serial DDR clock differential N.
SLVS2_N	B5	Output	HiSPi serial data, lane 2, differential N.
SLVS3_N	B6	Output	HiSPi serial data, lane 3, differential N.
SHUTTER	B9	Output	Control for external mechanical shutter. Can be left floating if not used.
VAA	C1, G1, D9, F9	Power	Analog power.
AGND	C2, G2, D8, E8, F8	Power	Analog ground.
VDD_SLVS	C4	Power	0.3V-0.6V or 1.7V - 1.9V port to HiSPi Output Driver. Set the High_VCM (R0x306E[9]) bit to 1 when configuring VDD_SLVS to 1.7 – 1.9V.
VDD	C5, J5, A9, H9, A7, D1, F1	Power	Digital power.
Reserved	C9, F7		
DGND	B7, C7, D7, E7, G7, B8, C8, G8, D2, E2, F2, H2, C3, G3, H3, C6, J6	Power	Digital ground.
EXTCLK	D3	Input	External input clock.
PIXCLK	D4	Output	Pixel clock out. Dout is valid on rising edge of this clock.
SADDR	D5	Input	Two-Wire Serial address select. 0: 0x20. 1: 0x30
TRIGGER	D6	Input	Exposure synchronization input.
VAA_PIX	E9	Power	Pixel power.
VDD_IO	E1, H1, J2, J7, A8, G9, J9	Power	I/O supply power.
SDATA	E3	I/O	Two-Wire Serial data I/O.
FLASH	E4	Output	Flash control output.
FRAME_VALID	E5	Output	Asserted when Dout frame data is valid.
SCLK	E6	Input	Two-Wire Serial clock input.
Dout11	F3	Output	Parallel pixel data output (MSB)
Dout10	F4	Output	Parallel pixel data output.
Dout9	F5	Output	Parallel pixel data output.
LINE_VALID	F6	Output	Asserted when Dout line data is valid.
Dout8	G4	Output	Parallel pixel data output.
Dout7	G5	Output	Parallel pixel data output.
Dout6	G6	Output	Parallel pixel data output.
Dout5	H4	Output	Parallel pixel data output.
Dout4	H5	Output	Parallel pixel data output.
Dout3	H6	Output	Parallel pixel data output.
RESET_BAR	H7	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
TEST	H8	Input.	Manufacturing test enable pin (connect to Dgnd).
Dout2	J1	Output	Parallel pixel data output.

**Table 3: Pin Descriptions, 80-ball iBGA**

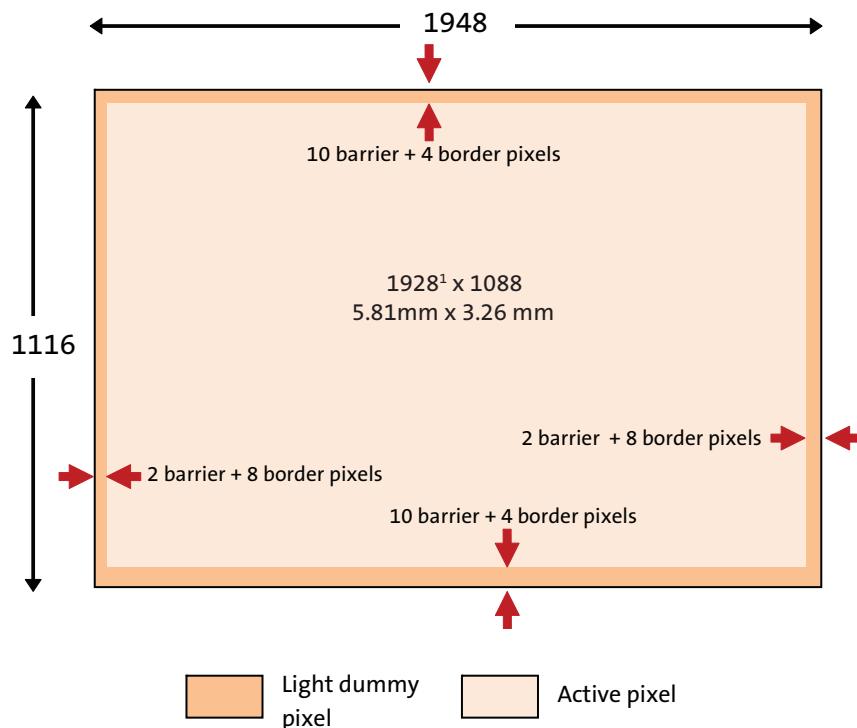
Name	iBGA Pin	Type	Description
DOUT1	J3	Output	Parallel pixel data output.
DOUT0	J4	Output	Parallel pixel data output (LSB)
OE_BAR	J8	Input	Output enable (active LOW).

## Pixel Data Format

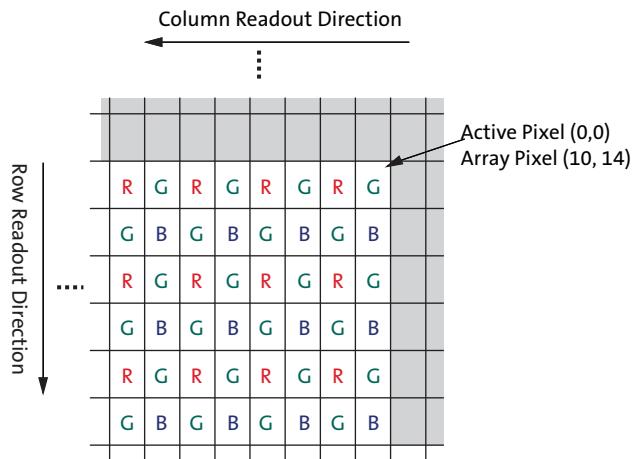
### Pixel Array Structure

While the sensor's format is 1928x1088, additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for mono-chrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

**Figure 5: Pixel Array Description**



**Figure 6: Pixel Color Pattern Detail (Top Right Corner)**

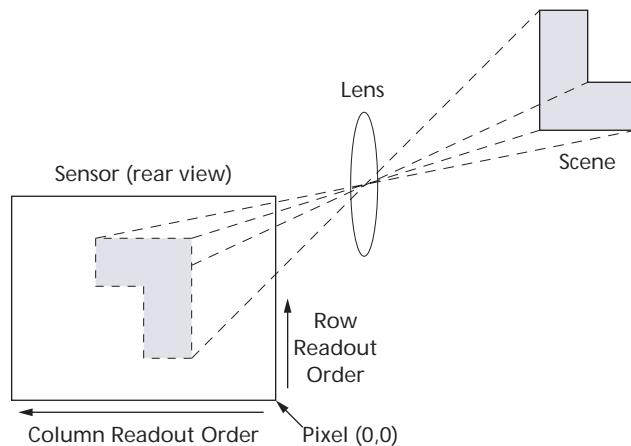


## Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 6). This reflects the actual layout of the array on the die. Also, the first pixel data read out of the sensor in default condition is that of pixel (10, 14).

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 7. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 7.

**Figure 7: Imaging a Scene**



## Features Overview

For a complete description, recommendations, and usage guidelines for product features, refer to the AR0230CS Developer Guide.

### 3.0 $\mu$ m Dual Conversion Gain Pixel

To improve the low light performance and keep the high dynamic range, a large (3.0 $\mu$ m) dual conversion gain pixel is implemented for better image optimization. With a dual conversion gain pixel, the conversion gain of the pixel may be dynamically changed to better adapt the pixel response based on dynamic range of the scene. This gain can be switched manually or automatically by an auto exposure control module.

### HDR

By default, the sensor powers up in HDR Mode. The HDR scheme used is multi-exposure HDR. This allows the sensor to handle up to 96 dB of dynamic range. In HDR mode, the sensor sequentially captures two exposures by maintaining two separate read and reset pointers that are interleaved within the rolling shutter readout. The intermediate pixel values are stored in line buffers while waiting for the two exposure values to be present. As soon as a pixel's two exposure values are available, they are combined to create a linearized 16-bit value for each pixel's response. The exposure ratio may be set to 4x, 8x, 16x, or 32x. Depending on whether HiSPi or Parallel mode is selected, the full 16 bit value may be output, it can be compressed to 12 bits using Adaptive Local Tone Mapping (ALTM), or companded to 12 or 14 bits.

Options to output T1 only, T2 only, or pixel interleaved data are also available. Individual exposures may be read out in a line interleaved mode as described in the T1/T2 Line Interleaved Mode section.

### Resolution

The active array supports a maximum of 1928x1088 pixels to support 1080p resolution. Utilizing a 3.0 $\mu$ m pixel will result in an optical format of 1/2.7-inch (approximately 6.6mm diagonal).

### Frame Rate

At full (1080p) resolution, the AR0230CS is capable of running up to 60 fps.

### Image Acquisition Mode

The AR0230CS supports two image acquisition modes:

- Electronic rolling shutter (ERS) mode

This is the normal mode of operation. When the AR0230CS is streaming, it generates frames at a fixed rate, and each frame is integrated (exposed) using the ERS. When ERS mode is in use, timing and control logic within the sensor sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and subsequently reading that row, the pixels in the row integrate incident light. The integration (exposure) time is controlled by varying the time between row reset and row readout. For each row in a frame, the time between row reset and row readout is the same, leading to a uniform integration time across the frame. When the integration time is changed (by using the two-wire serial interface to change register settings), the timing and control logic controls the transition from old to new integration

time in such a way that the stream of output frames from the AR0230CS switches cleanly from the old integration time to the new while only generating frames with uniform integration. See “Changes to Integration Time” in the AR0230CS Register Reference.

- Global reset mode.

This mode can be used to acquire a single image at the current resolution. In this mode, the end point of the pixel integration time is controlled by an external electromechanical shutter, and the AR0230CS provides control signals to interface to that shutter. The benefit of using an external electromechanical shutter is that it eliminates the visual artifacts associated with ERS operation. Visual artifacts arise in ERS operation, particularly at low frame rates, because an ERS image effectively integrates each row of the pixel array at a different point in time.

## Embedded Data and Statistics

The AR0230CS has the capability to output image data and statistics embedded within the frame timing. There are two types of information embedded within the frame readout.

- Embedded Data:

If enabled, these are displayed on the two rows immediately before the first active pixel row is displayed.

- Embedded Statistics:

If enabled, these are displayed on the two rows immediately after the last active pixel row is displayed.

## Multi-Camera Synchronization

The AR0230CS supports advanced line synchronization controls for multi-camera (stereo) support.

## Slave Mode

The slave mode feature of the AR0230CS supports triggering the start of a frame readout from an input signal that is supplied from an external ASIC. The slave mode signal allows for precise control of frame rate and register change updates.

## Context Switching and Register Updates

The user has the option of using the highly configurable context memory, or a simplified implementation in which only a subset of registers is available for switching. The AR0230 supports a highly configurable context switching RAM of size 256 x 16. Within this Context Memory, changes to any register may be stored. The register set for each context must be the same, but the number of contexts and registers per context are limited only by the size of the context memory.

Alternatively, the user may switch between two predefined register sets A and B by writing to a context switch change bit. When the context switch is configured to context A the sensor will reference the context A registers. If the context switch is changed from A to B during the readout of frame n, the sensor will then reference the context B

coarse\_integration\_time registers in frame n+1 and all other context B registers at the beginning of reading frame n+2. The sensor will show the same behavior when changing from context B to context A. The following registers are context switchable:

**Table 4: List of Configurable Registers for Context A and Context B**

Context A	Context B
Register Description	Register Description
coarse_integration_time	coarse_integration_time_cb
line_length_pck	line_length_pck_cb
frame_length_lines	frame_length_lines_cb
row_bin	row_bin_cb
col_bin	col_bin_cb
fine_gain	fine_gain_cb
coarse_gain	coarse_gain_cb
x_addr_start	x_addr_start_cb
y_addr_start	y_addr_start_cb
x_addr_end	x_addr_end_cb
y_addr_end	y_addr_end_cb
y_odd_inc	y_odd_inc_cb
x_odd_inc	x_odd_inc_cb
green1_gain	green1_gain_cb
blue_gain	blue_gain_cb
red_gain	red_gain_cb
green2_gain	green2_gain_cb
global_gain	global_gain_cb
operation_mode_ctrl	operation_mode_ctrl_cb
bypass_pix_comb	bypass_pix_comb_cb

## Motion Compensation/DLO

In typical multi-exposure HDR systems, motion artifacts can be created when objects move during the T1 or T2 integration time. When this happens, edge artifacts can potentially be visible and might look like a ghosting effect. To correct this, the AR0230CS has special 2D motion compensation circuitry that detects motion artifacts and corrects the image. The motion compensation feature can be optionally enabled by register write. Additional parameters are available to control the extent of motion detection and correction as per the requirements of the specific application.

## Tone Mapping

Real-world scenes often have a very high dynamic range (HDR) that far exceeds the electrical dynamic range of the imager. Dynamic range is defined as the luminance ratio between the brightest and the darkest objects in a scene. Even though the AR0230CS can capture full dynamic range images, the images are still limited by the low dynamic range of display devices. Today's typical LCD monitor has a contrast ratio around 1,000:1 while it is not atypical for an HDR image having a contrast ratio of around 250,000:1. Therefore, in order to reproduce HDR images on a low dynamic range display device, the captured high dynamic range must be compressed to the available range of the display device. This is commonly called tone mapping. The AR0230CS has implemented an adaptive local tone mapping (ALTM) feature to reproduce visually appealing images that increase the local contrast and the visibility of the images.

## Adaptive Color Difference (ADACD) Noise Filtering

A good noise reduction filter will remove noise from an image while retaining as much image detail as possible. To retain image detail, the noise reduction filter must adapt to the image signal. To remove noise, the noise reduction filter must adapt to the noise level of the image signal. The key is to remove the appropriate amount of noise. Over-filtering will cause image blurring while under-filtering will leave noise in the image. The AdaCD algorithm relies on a noise model derived from characterization data to aid in separating noise from signal.

The AR0230CS AdaCD algorithm performs pixel-by-pixel color noise correction for each of the red, blue, and green color planes. Each pixel is corrected based on surrounding pixel values on the same color plane and a noise model. The noise model is based on characterization data, and takes into account applied analog gain.

## Fast Mode Switch (Combi Mode)

To facilitate faster switching between linear and HDR modes, the AR0230CS includes a Combi Mode feature. When enabled, Combi Mode loads a single (HDR) sequencer. When switching from HDR to linear modes, the sequencer remains the same, but only the T1 image is output. While not optimized for linear mode operation, it allows faster mode switching as a new sequencer load is not needed. Switching between modes may result in the output of one bad frame.

## Analog/Digital Gains

A programmable analog gain of 1.5x to 12x applied simultaneously to all color channels will be featured along with a digital gain of 1x to 16x that may be configured on a per color channel basis.

## Skipping/Binning Modes

The AR0230CS supports subsampling. Subsampling allows the sensor to read out a smaller set of active pixels by either skipping, binning, or summing pixels within the readout window. Horizontal binning is achieved in the digital readout. The sensor will sample the combined 2x adjacent pixels within the same color plane. Vertical row binning is applied in the pixel readout. Row binning can be configured as 2x rows within the same color plane. Pixel skipping can be configured up to 2x in both the x-direction and y-direction. Skipping pixels in the x-direction will not reduce the row time. Skipping pixels in the y direction will reduce the number of rows from the sensor effectively reducing the frame time. Skipping will introduce image artifacts from aliasing.

The AR0230CS supports row wise vertical binning. Row wise vertical summing is not supported.

## Clocking Options

The sensor contains a phase-locked loop (PLL) that is used for timing generation and control. The required VCO clock frequency is attained through the use of a pre-PLL clock divider followed by a multiplier. The PLL multiplier should be an even integer. If an odd integer (M) is programmed, the PLL will default to the lower (M-1) value to maintain an even multiplier value. The multiplier is followed by a set of dividers used to generate the

output clocks required for the sensor array, the pixel analog and digital readout paths, and the output parallel and serial interfaces. Use of the PLL is required when using the HiSPi interface.

## Temperature Sensor

The AR0230CS sensor has a built-in PTAT-based temperature sensor, accessible through registers, that is capable of measuring die junction temperature. The value read out from the temperature sensor register is an ADC output value that needs to be converted downstream to a final temperature value in degrees Celsius. Since the PTAT device characteristic response is quite linear in the temperature range of operation required, a simple linear function can be used to convert the ADC output value to the final temperature in degrees Celsius.

Two reference points will be made available via register read for back-calculating the junction temperature value. An error of +/- 5% or better over the full specified operating range of the sensor is to be expected.

## Silicon / Firmware / Sequencer Revision Information

A revision register will be provided to read out (via I2C) silicon and sequencer/OTPM revision information. This will be helpful to distinguish among different lots of material if there are future OTPM or sequencer revisions.

## Lens Shading Correction

The latest lens shading correction algorithm will be included for potential low Z height applications.

## Companding

The 16-bit linearized HDR image may be compressed to 12- or 14- bits using on-chip companding. This is useful if on-chip ALTM will not be used and the ISP cannot handle 16 bit data.

## Compression

When the AR0230CS is configured for linear mode operation, the sensor can optionally compress 12-bit data to 10-bit using A-law compression. The A-law compression is disabled by default

## Packaging

The AR0230CS will be offered in a 10x10 80-iBGA package (parallel and HiSPi). The package will have anti-reflective coating on both sides of the cover glass.

## Parallel Interface

The parallel pixel data interface uses these output-only signals:

- FRAME\_VALID
- LINE\_VALID
- PIXCLK
- DOUT[11:0]

The parallel pixel data interface is disabled by default at power up and after reset. It can be enabled by programming R0x301A. When the parallel pixel data interface is in use, the serial data output signals can be left unconnected.

## High Speed Serial Pixel (HiSPi) Interface

The HiSPi interface supports three protocols, Streaming-S, Streaming-SP, and Packetized SP. The streaming protocols conform to a standard video application where each line of active or intra-frame blanking provided by the sensor is transmitted at the same length. The Packetized SP protocol will transmit only the active data ignoring line-to-line and frame-to-frame blanking data.

The HiSPi interface building block is a unidirectional differential serial interface with four data and one double data rate (DDR) clock lanes. One clock for every four serial data lanes is provided for phase alignment across multiple lanes. The AR0230CS supports serial data widths of 10, 12, 14, 16, or 20 bits on one, two, or four lanes. The specification includes a DLL to compensate for differences in group delay for each data lane. The DLL is connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. Once the DLL has gained phase lock, each lane can be delayed in 1/8 unit interval (UI) steps. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design. Delay compensation may be set for clock and/or data lines in the hispi\_timing register R0x31C0. If the DLL timing adjustment is not required, the data and clock lane delay settings should be set to a default code of 0x000 to reduce jitter, skew, and power dissipation.

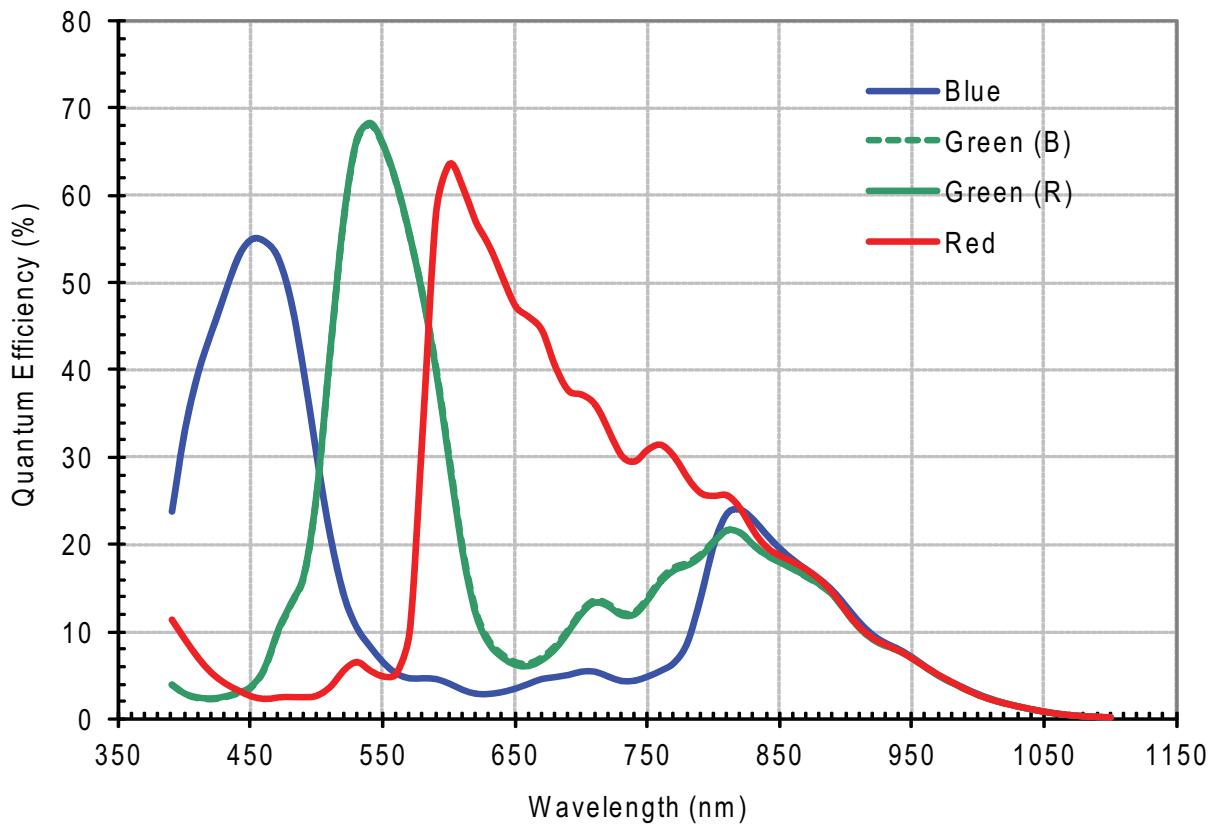
## Sensor Control Interface

The two-wire serial interface bus enables read/write access to control and status registers within the AR0230CS. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers.

Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD\_IO off-chip by a 1.5kΩ resistor. Either the slave or master device can drive SDATA LOW—the interface protocol determines which device is allowed to drive SDATA at any given time. The two-wire serial interface can run at 100 kHz or 400 kHz.

## T1/T2 Line Interleaved Mode

The AR0230CS has the capability to output the T1 and T2 exposures separately, in a line interleaved format. The purpose of this is to enable off chip HDR linear combination and processing. See the AR0230 Developer Guide for more information.

**Figure 8: Quantum Efficiency**

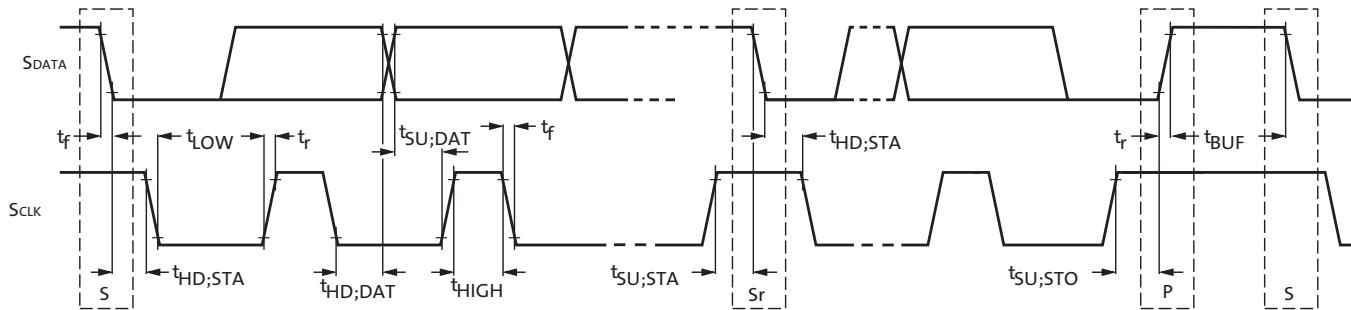
## Electrical Specifications

Unless otherwise stated, the following specifications apply under the following conditions:  $V_{DD} = 1.8V - 0.10/+0.15$ ;  $V_{DD\_IO} = V_{DD\_PLL} = V_{AA} = V_{AA\_PIX} = 2.8V \pm 0.3V$ ;  $V_{DD\_SLVS} = 0.4V - 0.1/+0.2$ ;  $T_A = -30^\circ C$  to  $+85^\circ C$ ; output load = 10pF; frequency = 74.25 MHz; HiSPi off.

### Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 9 and Table 5.

**Figure 9: Two-Wire Serial Bus Timing Parameters**



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

**Table 5: Two-Wire Serial Bus Characteristics**

$f_{EXTCLK} = 27$  MHz;  $V_{DD} = 1.8V$ ;  $V_{DD\_IO} = 2.8V$ ;  $V_{AA} = 2.8V$ ;  $V_{AA\_PIX} = 2.8V$ ;  $V_{DD\_PLL} = 2.8V$ ;  $T_A = 25^\circ C$

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	$f_{SCL}$	0	100	0	400	KHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	$\mu s$
LOW period of the SCLK clock	$t_{LOW}$	4.7	-	1.3	-	$\mu s$
HIGH period of the SCLK clock	$t_{HIGH}$	4.0	-	0.6	-	$\mu s$
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	$\mu s$
Data hold time	$t_{HD;DAT}$	$0^4$	$3.45^5$	$0^6$	$0.9^5$	$\mu s$
Data set-up time	$t_{SU;DAT}$	250	-	$100^6$	-	ns
Rise time of both SDATA and SCLK signals	$t_r$	-	1000	$20 + 0.1Cb^7$	300	ns
Fall time of both SDATA and SCLK signals	$t_f$	-	300	$20 + 0.1Cb^7$	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	$\mu s$
Bus free time between a STOP and START condition	$t_{BUF}$	4.7	-	1.3	-	$\mu s$
Capacitive load for each bus line	$C_b$	-	400	-	400	pF
Serial interface input pin capacitance	$C_{IN\_SI}$	-	3.3	-	3.3	pF
SDATA max load capacitance	$CLOAD\_SD$	-	30	-	30	pF
SDATA pull-up resistor	$R_{SD}$	1.5	4.7	1.5	4.7	$k\Omega$

Notes:

1. This table is based on I<sup>2</sup>C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I<sup>2</sup>C-compatible.
3. All values referred to  $V_{IHmin} = 0.9 VDD$  and  $V_{ILmax} = 0.1 VDD$  levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
5. The maximum  $t^{HD;DAT}$  has only to be met if the device does not stretch the LOW period ( $t^{LOW}$ ) of the SCLK signal.
6. A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, but the requirement  $t^{SU;DAT} \geq 250$  ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line  $t_r \max + t^{SU;DAT} = 1000 + 250 = 1250$  ns (according to the Standard-mode I<sup>2</sup>C-bus specification) before the SCLK line is released.
7.  $C_b$  = total capacitance of one bus line in pF.

## I/O Timing

By default, the AR0230CS launches pixel data, FV, and LV with the falling edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV, and LV using the rising edge of PIXCLK.

See Figure 10 below and Table 6 on page 23 for I/O timing (AC) characteristics.

**Figure 10: I/O Timing Diagram**

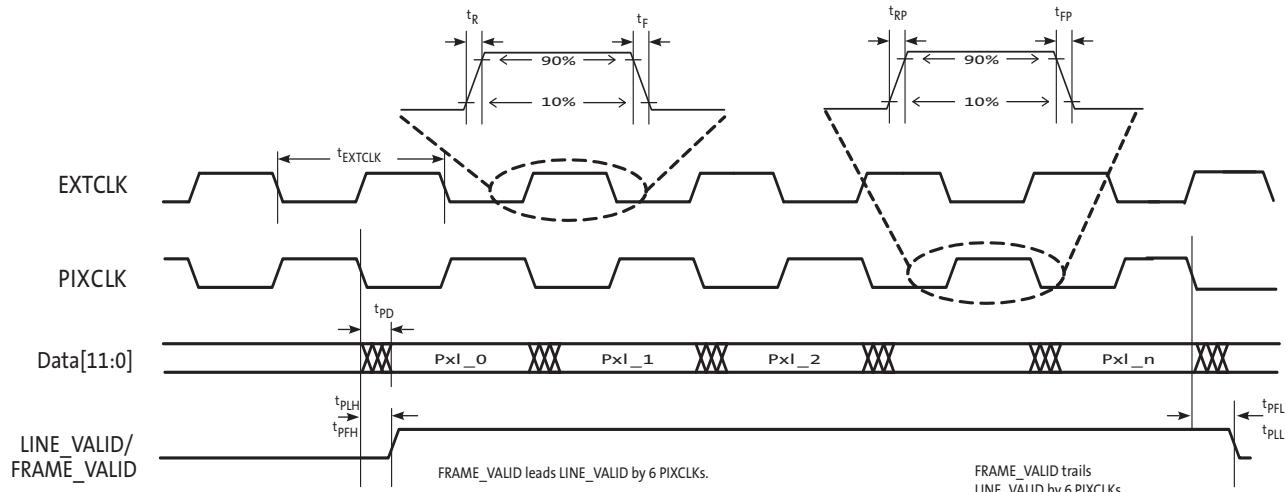




Table 6: I/O Timing Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
$f_{EXTCLK1s}$	Input clock frequency		6	—	48	MHz
$t_{EXTCLK1}$	Input clock period		20.8	—	166	ns
$t_R$	Input clock rise time		—	3	—	ns
$t_F$	Input clock fall time		—	3	—	ns
$t_{RP}$	Pixclk rise time		—	4	—	ns
$t_{FP}$	Pixclk fall time		—	4	—	ns
	Clock duty cycle		40	50	60	%
$t_{PIXJITTER}$	Jitter on PIXCLK		—	1	—	ns
$t_{CP}$	EXTCLK to PIXCLK propagation delay	Nominal voltages, PLL Disabled	—	30	—	ns
$f_{PIXCLK}$	PIXCLK frequency	Default, Nominal Voltages	6		74.25	MHz
$t_{PD}$	PIXCLK to data valid	Default, Nominal Voltages	—	2.3	—	ns
$t_{PFH}$	PIXCLK to FV HIGH	Default, Nominal Voltages	—	8	—	ns
$t_{PLH}$	PIXCLK to LV HIGH	Default, Nominal Voltages	—	8	—	ns
$t_{PFL}$	PIXCLK to FV LOW	Default, Nominal Voltages	—	8	—	ns
$t_{PLL}$	PIXCLK to LV LOW	Default, Nominal Voltages	—	8	—	ns
CLOAD	Output load capacitance		—	<10	—	pF
CIN	Input pin capacitance		—	2.5	—	pF

Note: I/O timing characteristics are measured under the following conditions:

- Temperature is 25°C ambient
- 10 pF load
- 1.8V I/O supply voltage



## DC Electrical Characteristics

The DC electrical characteristics are shown in the tables below.

**Table 7: DC Electrical Characteristics**

Symbol	Definition	Condition	Min	Typ	Max	Unit
VDD	Core digital voltage		1.7	1.8	1.95	V
VDD_IO	I/O digital voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
VAA	Analog voltage		2.5	2.8	3.1	V
VAA_PIX	Pixel supply voltage		2.5	2.8	3.1	V
VDD_PLL	PLL supply voltage		2.5	2.8	3.1	V
VDD_SLVS	HiSPi supply voltage		0.3	0.4	0.6	V
VIH	Input HIGH voltage		VDD_IO*0.7	—	—	V
VIL	Input LOW voltage		—	—	VDD_IO*0.3	V
IIN	Input leakage current	No pull-up resistor; VIN = VDD_IO or DGND	20	—	—	µA
VOH	Output HIGH voltage		VDD_IO-0.3	—	—	V
VOL	Output LOW voltage		—	—	0.4	V
IOH	Output HIGH current	At specified VOH	-22	—	—	mA
IOL	Output LOW current	At specified VOL	—	—	22	mA

**Caution** **Stresses greater than those listed in Table 14 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.**

**Table 8: Absolute Maximum Ratings**

Symbol	Definition	Condition	Min	Max	Unit
VDD_MAX	Core digital voltage		-0.3	2.4	V
VDD_IO_MAX	I/O digital voltage		-0.3	4	V
VAA_MAX	Analog voltage		-0.3	4	V
VAA_PIX	Pixel supply voltage		-0.3	4	V
VDD_PLL	PLL supply voltage		-0.3	4	V
VDD_SLVS_MAX	HiSPi I/O digital voltage		-0.3	2.4	V
t <sub>ST</sub>	Storage temperature		-40	85	°C

Note: Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 9: Operating Current Consumption in Parallel Output and Linear Mode**

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital operating current	Streaming, 1080p30	IDD1	TBD	138	TBD	mA
I/O digital operating current	Streaming, 1080p30	IDD_IO	TBD	18	TBD	mA
Analog operating current	Streaming, 1080p30	IAA	TBD	44	TBD	mA
Pixel supply current	Streaming, 1080p30	IAA_PIX	TBD	5	TBD	mA
PLL supply current	Streaming, 1080p30	IDD_PLL	TBD	6	TBD	mA

Notes: 1. Operating currents are measured at the following conditions:

$$VAA = VAA_PIX = VDD_PLL = 2.8V$$

$$VDD = VDD_IO = 1.8V$$

PLL Enabled and PIXCLK = 74.25 MHz

$$T_A = 25^\circ C$$

**Table 10: Operating Current Consumption in Parallel Output and HDR Mode**

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital operating current	Streaming, 1080p30	IDD	TBD	172	TBD	mA
I/O digital operating current	Streaming, 1080p30	IDD_IO	TBD	13	TBD	mA
Analog operating current	Streaming, 1080p30	IAA	TBD	46	TBD	mA
Pixel supply current	Streaming, 1080p30	IAA_PIX	TBD	6	TBD	mA
PLL supply current	Streaming, 1080p30	IDD_PLL	TBD	6	TBD	mA

Notes: 1. Operating currents are measured at the following conditions:

$$VAA = VAA_PIX = VDD_PLL = 2.8V$$

$$VDD = VDD_IO = 1.8V$$

PLL Enabled and PIXCLK = 74.25 MHz

$$T_A = 25^\circ C$$

**Table 11: Operating Current in HiSPi (HiVCM) Output and Linear Mode**

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	Streaming, 1080p60	IDD	TBD	280	TBD	mA
Analog Operating Current	Streaming, 1080p60	IAA	TBD	48	TBD	mA
Pixel Supply Current	Streaming, 1080p60	IAA_PIX	TBD	5.0	TBD	mA
PLL Supply Current	Streaming, 1080p60	IDD_PLL	TBD	8.3	TBD	mA
SLVS Supply Current	Streaming, 1080p60	IDD_SLVS	TBD	20	TBD	mA

Notes: 1. Operating currents are measured at the following conditions:

$V_{AA}=V_{AA\_PIX}=V_{DD\_PLL}=2.8V$

$V_{DD}=V_{DD\_IO}=1.8V$

$V_{DD\_SLVS}=1.8V$

PLL Enabled and PIXCLK=74.25 Mhz

$T_A=25^{\circ}C$

4-lane HiSPi mode

**Table 12: Operating Current in HiSPi (HiVCM) Output and HDR Mode**

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	Streaming, 1080p60	IDD	TBD	350	TBD	mA
Analog Operating Current	Streaming, 1080p60	IAA	TBD	68	TBD	mA
Pixel Supply Current	Streaming, 1080p60	IAA_PIX	TBD	6.0	TBD	mA
PLL Supply Current	Streaming, 1080p60	IDD_PLL	TBD	8.3	TBD	mA
SLVS Supply Current	Streaming, 1080p60	IDD_SLVS	TBD	20	TBD	mA

Notes: 1. Operating currents are measured at the following conditions:

$V_{AA}=V_{AA\_PIX}=V_{DD\_PLL}=2.8V$

$V_{DD}=V_{DD\_IO}=1.8V$

$V_{DD\_SLVS}=1.8V$

PLL Enabled and PIXCLK=74.25MHz

$T_A=25^{\circ}C$

4-lane HiSPi mode

**Table 13: Operating Current in HiSPi (SLVS) Output and Linear Mode**

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	Streaming, 1080p60	IDD	TBD	280	TBD	mA
Analog Operating Current	Streaming, 1080p60	IAA	TBD	48	TBD	mA
Pixel Supply Current	Streaming, 1080p60	IAA_PIX	TBD	5.0	TBD	mA
PLL Supply Current	Streaming, 1080p60	IDD_PLL	TBD	8.3	TBD	mA
SLVS Supply Current	Streaming, 1080p60	IDD_SLVS	TBD	9.5	TBD	mA

Notes: 1. Operating currents are measured at the following conditions:

$V_{AA}=V_{AA\_PIX}=V_{DD\_PLL}=2.8V$

$V_{DD}=V_{DD\_IO}=1.8V$

$V_{DD\_SLVS}=0.4V$

PLL Enabled and PIXCLK=74.25 MHz

$T_A=25^{\circ}C$

4-lane HiSPi mode

**Table 14: Operating Current in HiSPi (SLVS) Output and HDR Mode**

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	Streaming, 1080p60	IDD	TBD	350	TBD	mA
Analog Operating Current	Streaming, 1080p60	IAA	TBD	68	TBD	mA
Pixel Supply Current	Streaming, 1080p60	IAA_PIX	TBD	6.0	TBD	mA
PLL Supply Current	Streaming, 1080p60	IDD_PLL	TBD	8.3	TBD	mA
SLVS Supply Current	Streaming, 1080p60	IDD_SLVS	TBD	9.5	TBD	mA

Notes: 1. Operating currents are measured at the following conditions:

$V_{AA}=V_{AA\_PIX}=V_{DD\_PLL}=2.8V$

$V_{DD}=V_{DD\_IO}=1.8V$

$V_{DD\_SLVS}=0.4V$

PLL Enabled and PIXCLK=74.25 MHz

$T_A=25^{\circ}C$

4-lane HiSPi mode



## HiSPi Electrical Specifications

The Aptina AR0230CS sensor supports both SLVS and HiVCM HiSPi modes. Please refer to the High-Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing information. The VDD\_SLVS supply in this datasheet corresponds to VDD\_TX in the HiSPi Physical Layer Specification. Similarly, VDD is equivalent to VDD\_HiSPi as referenced in the specification. The DLL as implemented on AR0230CS is limited in the number of available delay steps and differs from the HiSPi specification as described in this section.

**Table 15: Channel Skew**

Measurement Conditions: VDD\_HiSPi = 1.8V; VDD\_HiSPi\_TX = 0.4V; Data Rate = 480 Mbps; DLL set to 0

Data Lane Skew in Reference to Clock	tCHSKEW1PHY	-150	ps

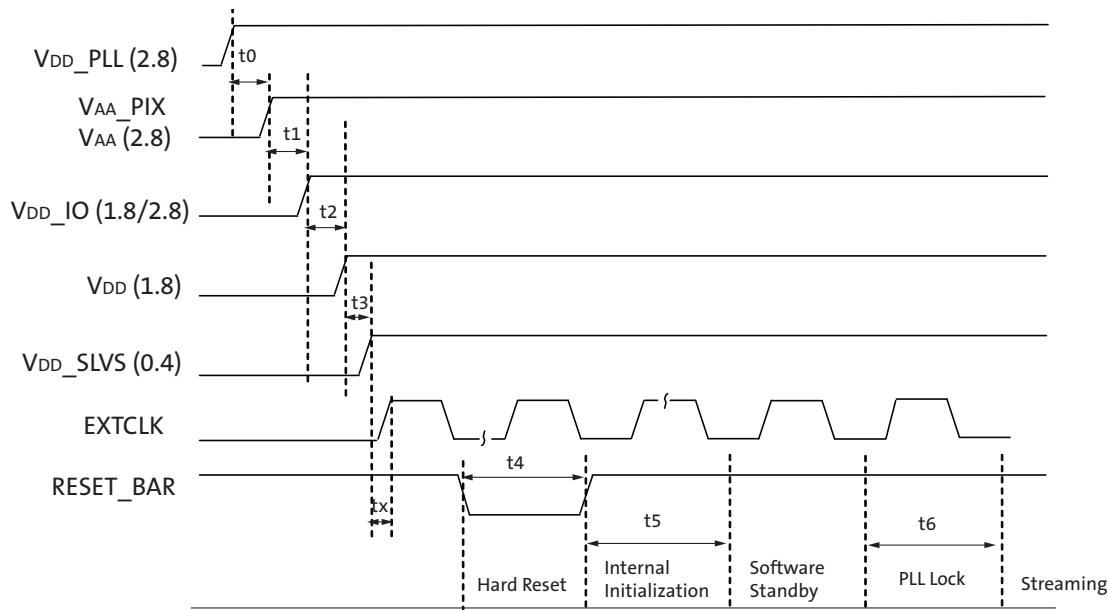
## Power-On Reset and Standby Timing

### Power-Up Sequence

The recommended power-up sequence for the AR0230CS is shown in Figure 11. The available power supplies (VDD\_IO, VDD, VDD\_SLVS, VDD\_PLL, VAA, VAA\_PIX) must have the separation specified below.

1. Turn on VDD\_PLL power supply.
2. After 100 $\mu$ s, turn on VAA and VAA\_PIX power supply.
3. After 100 $\mu$ s, turn on VDD\_IO power supply.
4. After 100 $\mu$ s, turn on VDD power supply.
5. After 100 $\mu$ s, turn on VDD\_SLVS power supply.
6. After the last power supply is stable, enable EXTCLK.
7. Assert RESET\_BAR for at least 1ms. The parallel interface will be tri-stated during this time.
8. Wait 150000 EXTCLKs (for internal initialization into software standby).
9. Configure PLL, output, and image settings to desired values.
10. Wait 1ms for the PLL to lock.
11. Set streaming mode (R0x301a[2] = 1).

**Figure 11: Power Up**



**Table 16: Power-Up Sequence**

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PLL to VAA/VAA_PIX <sup>3</sup>	t0	0	100	—	$\mu$ s
VAA/VAA_PIX to VDD_IO	t1	0	100	—	$\mu$ s
VDD_IO to VDD	t2	0	100	—	$\mu$ s
VDD to VDD_SLVS	t3	0	100	—	$\mu$ s
Xtal settle time	tx	—	30 <sup>1</sup>	—	ms

**Table 16: Power-Up Sequence (continued)**

Definition	Symbol	Minimum	Typical	Maximum	Unit
Hard Reset	t4	1 <sup>2</sup>	–	–	ms
Internal Initialization	t5	150000	–	–	EXTCLKs
PLL Lock Time	t6	1	–	–	ms

Notes:

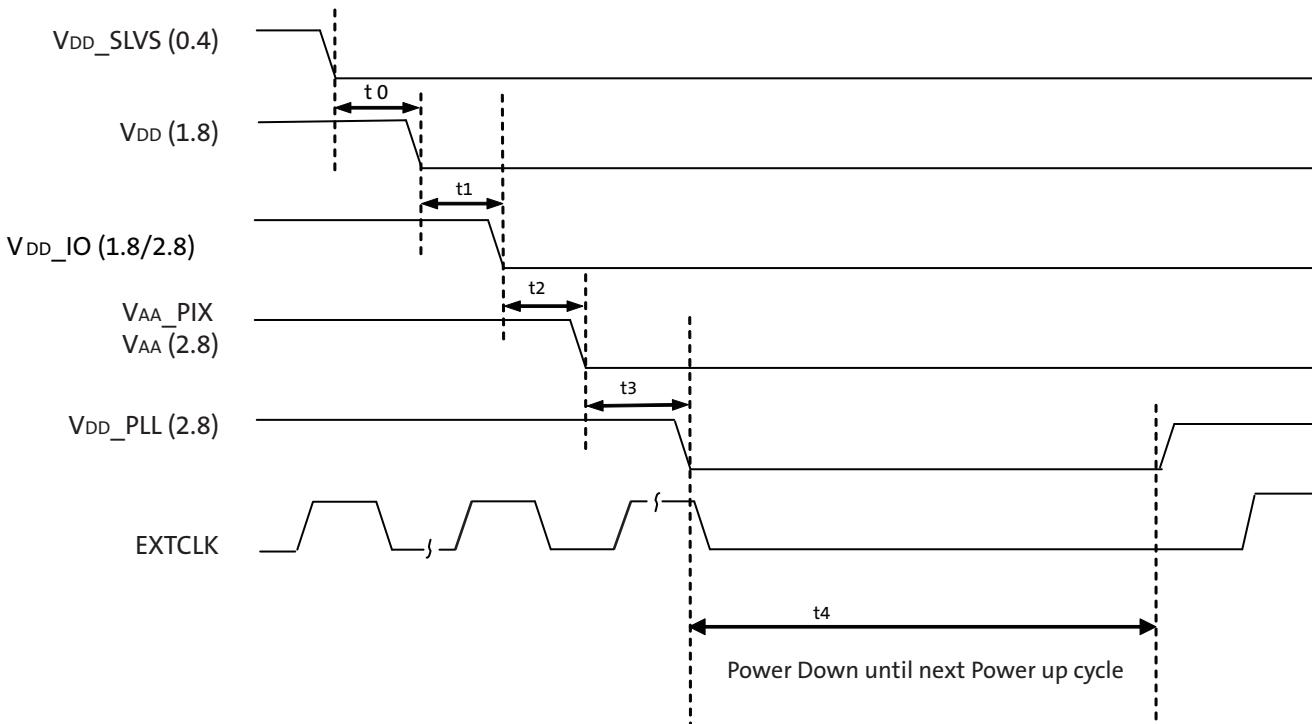
1. Xtal settling time is component-dependent, usually taking about 10 – 100 ms.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
3. It is critical that V<sub>DD</sub>\_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that V<sub>DD</sub>\_PLL is powered after other supplies then sensor may have functionality issues and will experience high current draw on this supply.

## Power-Down Sequence

The recommended power-down sequence for the AR0230CS is shown in Figure 12. The available power supplies (V<sub>DD</sub>\_IO, V<sub>DD</sub>, V<sub>DD</sub>\_SLVS, V<sub>DD</sub>\_PLL, V<sub>AA</sub>, V<sub>AA</sub>\_PIX) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off V<sub>DD</sub>\_SLVS.
4. Turn off V<sub>DD</sub>.
5. Turn off V<sub>DD</sub>\_IO
6. Turn off V<sub>AA</sub>/V<sub>AA</sub>\_PIX.
7. Turn off V<sub>DD</sub>\_PLL.

**Figure 12: Power Down**



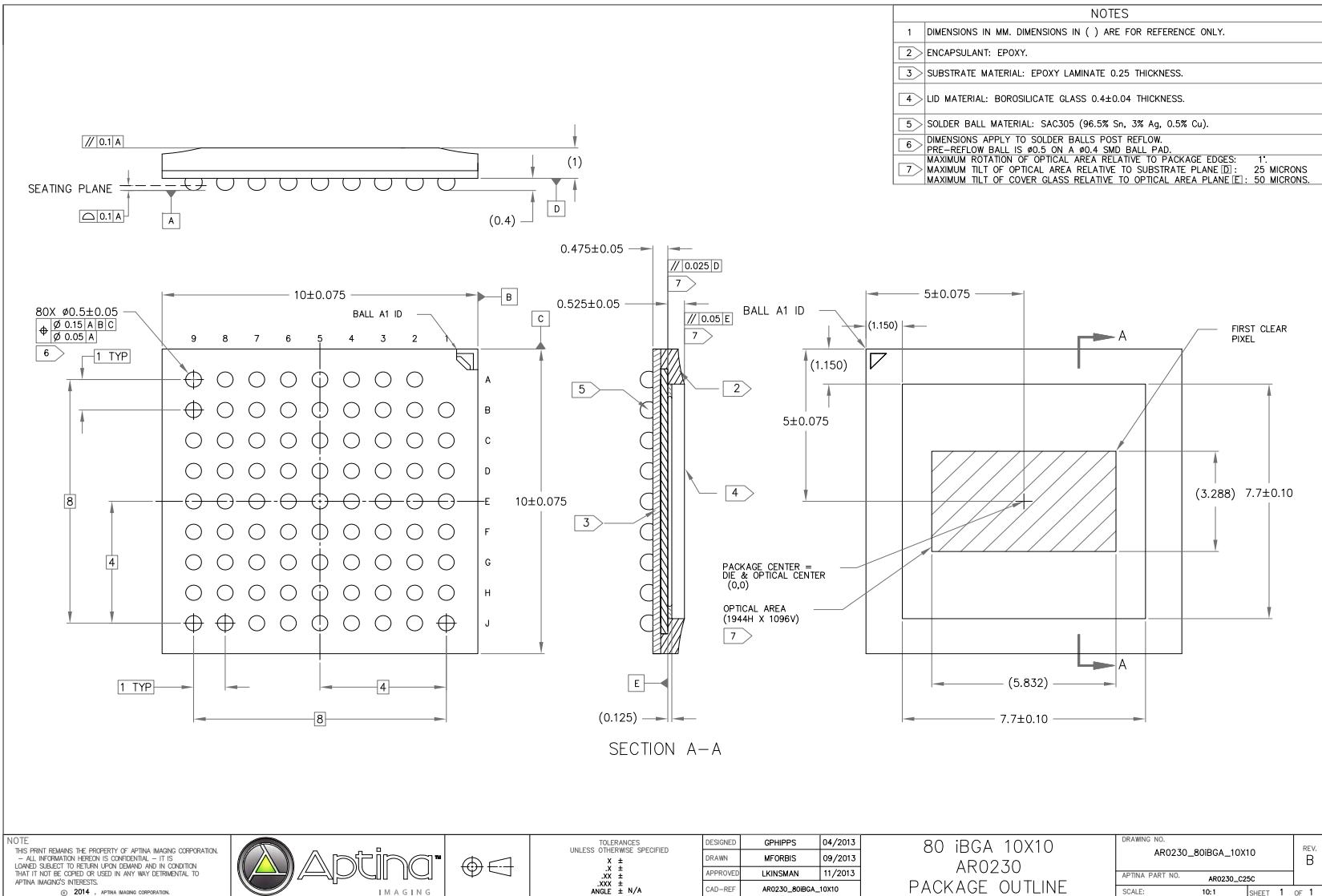
**Table 17: Power-Down Sequence**

Definition	Symbol	Minimum	Typical	Maximum	Unit
V <sub>DD</sub> _SLVS to V <sub>DD</sub>	t <sub>0</sub>	0	—	—	μs
V <sub>DD</sub> to V <sub>DD</sub> _IO	t <sub>1</sub>	0	—	—	μs
V <sub>DD</sub> _IO to V <sub>AA</sub> /V <sub>AA</sub> _PIX	t <sub>2</sub>	0	—	—	μs
V <sub>AA</sub> /V <sub>AA</sub> _PIX to V <sub>DD</sub> _PLL	t <sub>3</sub>	0	—	—	μs
PwrDn until Next PwrUp Time	t <sub>4</sub>	100	—	—	ms

t4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

## Package Diagrams

Figure 13: 80iBGA 10x10 Package Diagram



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DESIGNED: GPHIPPS 04/2013  
DRAWN: MFORBIS 09/2013  
APPROVED: LKINSMAN 11/2013  
CAD-REF: AR0230\_80IBGA\_10X10

80 iBGA 10X10  
AR0230  
PACKAGE OUTLINE

DRAWING NO.: AR0230\_80IBGA\_10X10  
REV. B  
APTEA PART NO.: AR0230\_C25C  
SCALE: 10:1 SHEET 1 OF 1



## Revision History

Rev. 2 .....	9/22/14
	<ul style="list-style-type: none"><li>• Updated Table 1, "Key Parameters," on page 1</li><li>• Updated Table 2, "Available Part Numbers," on page 1</li><li>• Updated "Packaging" on page 18</li><li>• Updated Table 9, "Operating Current Consumption in Parallel Output and Linear Mode," on page 25</li><li>• Updated Table 10, "Operating Current Consumption in Parallel Output and HDR Mode," on page 25</li><li>• Updated Table 11, "Operating Current in HiSPi (HiVCM) Output and Linear Mode," on page 26</li><li>• Updated Table 12, "Operating Current in HiSPi (HiVCM) Output and HDR Mode," on page 26</li><li>• Updated Table 13, "Operating Current in HiSPi (SLVS) Output and Linear Mode," on page 27</li><li>• Updated Table 14, "Operating Current in HiSPi (SLVS) Output and HDR Mode," on page 27</li><li>• Deleted references to iLCC package:<ul style="list-style-type: none"><li>– Figure 4: 48 iLCC Package, Parallel Output</li><li>– Table 3: Pin Descriptions</li><li>– Figure 5: 48 iLCC Package, HiSPi Output</li><li>– Table 4: Pin Descriptions, 48 iLCC</li><li>– Figure 16: 48iLCC 10x10 Parallel Package Diagram</li><li>– Figure 17: 48iLCC 10x10 Serial Package Diagram</li></ul></li></ul>
Rev. 1 .....	3/18/14
	<ul style="list-style-type: none"><li>• Initial release</li></ul>