1/4-Inch 1.0 Mp CMOS Digital Image Sensor with Global Shutter

AR0144 Datasheet, Rev. 4

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Features

- Superior low-light and IR performance
- HD video (720p60)
- 2-lane MIPI or Parallel data interface
- Automatic black Level Calibration (ABLC)
- Programmable control for Region Of Interest (ROI)
- Horizontal and vertical mirroring, windowing and pixel binning
- On chip auto exposure control for any programmable ROI
- 5x5 Statistics engine for any programmable ROI
- Flexible control for row and column skip mode
- On-chip slave or trigger mode for synchronization
- Built in strobe control
- On chip Phase Lock loop (PLL)
- On-chip slave or trigger mode for synchronization

Applications

- Bar code scanner
- Gesture Recognition
- 3D scanning
- Positional tracking
- Iris scanning
- Augmented reality
- Virtual reality
- Biometrics
- Machine vision

General Description

The AR0144 is a 1/4-inch 1.0 Mp CMOS digital image sensor with an active-pixel array of 1280H x 800V. It incorporates a new innovative global shutter pixel design optimized for accurate and fast capture of moving scenes. The sensor produces clear, low noise images in both low-light and bright scenes. It includes sophisticated camera functions such as auto exposure control, windowing, row skip mode, column-skip mode, pixel-binning and both video and single frame modes. It is programmable through a simple two-wire serial interface. The AR0144 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including scanning and industrial inspection.

Table 1: Key Parameters

Parameter		Typical Value
Optical format		1/4-inch (4.5 mm)
Active pixels		1280H x 800V = 1.0 Mp
Pixel size		3.0 µm
Color filter array		RGB Bayer or Monochrome
Chief Ray Angle		0 or 20°
Shutter type		Global shutter
Input clock range		6 – 64 MHz
Output pixel clock (maximum)		74.25 MHz
Output	Serial	MIPI, 2-Lane
	Parallel	12-bit
Frame rate	Full resolution	60 fps
	720p	66 fps
Responsivity	Monochrome	3.6 V/lux-sec
	Color	3.1 V/lux-sec
SNR_{MAX}		38 dB
Dynamic range		63.9 dB
Supply voltage	I/O	1.8 or 2.8 V
	Digital	1.2 V
	Analog	2.8 V
Power consumption		<250mW
Operating temperature		–40°C to +85°C (ambient) –40°C to +105°C (junction)
Package options		5.6 x 5.6 mm 69-ball CSP
		Bare die

‡This document contains information on a new product. Specifications and information herein are subject to change without notice.

Ordering Information

Table 2: Available Part Numbers

Part Number	Product Description	**Orderable Product Attribute Description**
AR0144CSSC00SUKA0-CPBR-E	Color, CSP	RGB-CSP; CRA = 0; with Protective Film, Double Side BBAR Glass
AR0144CSSC00SUKA0-CRBR-E	Color, CSP	RGB-CSP; CRA = 0; without Protective Film, Double Side BBAR Glass
AR0144CSSM00SUKA0-CPBR-E	Mono, CSP	MONO - CSP; CRA = 0; with Protective Film, Double Side BBAR Glass
AR0144CSSM00SUKA0-CRBR-E	Mono, CSP	MONO - CSP; CRA = 0; without Protective Film, Double Side BBAR Glass
AR0144CSSC00SUEAH-GEVB	Color, CSP Head Board	RGB - Headboard; CRA = 0
AR0144CSSM00SUEAH-GEVB	Mono, CSP Head Board	MONO - Headboard; CRA = 0
AR0144CSSC20SUKA0-CPBR-E	Color, CSP	RGB- CSP; CRA = 20; with Protective Film, Double Side BBAR Glass
AR0144CSSC20SUKA0-CRBR-E	Color, CSP	RGB- CSP; CRA = 20; without Protective Film, Double Side BBAR Glass
AR0144CSSM20SUKA0-CPBR-E	Mono, CSP	MONO - CSP; CRA = 20; with Protective Film, Double Side BBAR Glass
AR0144CSSM20SUKA0-CRBR-E	Mono, CSP	MONO - CSP; CRA = 20; without Protective Film, Double Side BBAR Glass
AR0144CSSC20SUEAH-GEVB	Color, CSP Head Board	RGB- Headboard; CRA = 20
AR0144CSSM20SUEAH-GEVB	Mono, CSP Head Board	MONO- Headboard; CRA = 20
AR0144CSSC00SUD20	Color, Bare Die	RGB; CRA = 0
AR0144CSSC20SUD20	Color, Bare Die	RGB; CRA = 20
AR0144CSSM00SUD20	Mono, Bare Die	MONO; CRA = 0
AR0144CSSM20SUD20	Mono, Bare Die	MONO; CRA = 20

See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

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General Description

The ON Semiconductor AR0144 can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a full-resolution image at 60 frames per second (fps). It outputs 12-bit raw data, using either the parallel or serial (MIPI) output ports. The device may be operated in video (master) mode or in frame trigger mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock. A dedicated FLASH pin can be programmed to control external LED or flash exposure illumination.

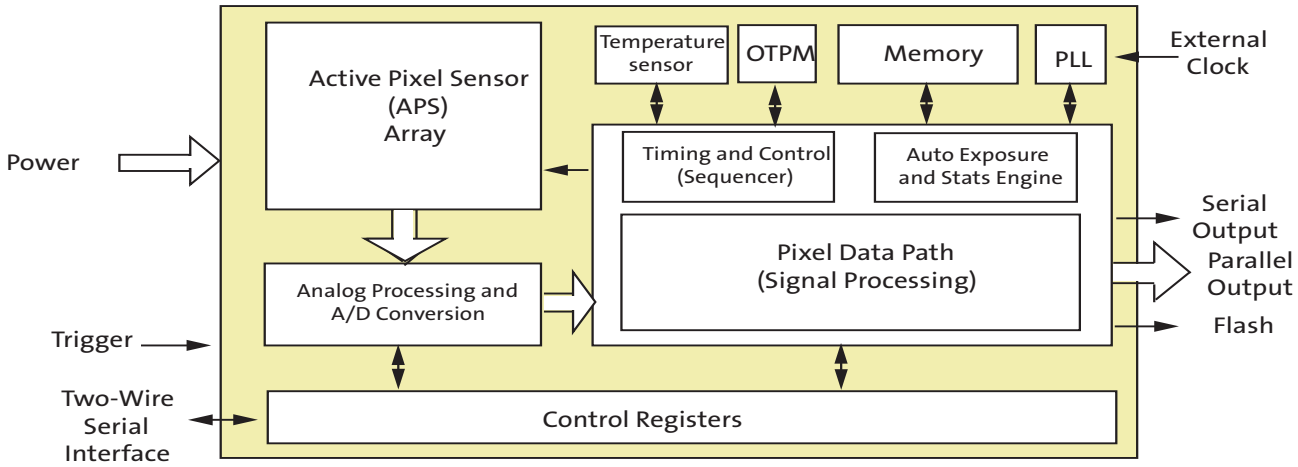
The AR0144 includes additional features to allow application-specific tuning: windowing, adjustable auto-exposure control, auto black level correction, on-board temperature sensor, row-skip and column-skip modes and binning modes.

The sensor is designed to operate in a wide temperature range (–40°C to +85°C).

Functional Overview

The AR0144 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 64 MHz. The maximum output pixel rate is 74.25 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor.

Figure 1: Block Diagram



User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.0 Mp Active- Pixel Sensor array. The AR0144 features global shutter technology for accurate capture of moving images. The exposure of the entire array is controlled by programming the integration time by register setting. All rows simultaneously integrate light prior to readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to- digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital

processing signal chain (which provides further data path corrections and applies digital gain). The pixel data are output at a rate of up to 74.25 Mp/s, in parallel to frame and line synchronization signals.

Features Overview

The AR0144 Global Shutter sensor has a wide array of features to enhance functionality and to increase versatility. A summary of features follows. Please refer to the AR0144 Developer Guide for detailed feature descriptions, register settings, and tuning guidelines and recommendations.

- 3.0 um Global Shutter Pixel
  To improve the low light performance and to capture the moving images accurately a large (3.0 um) global shutter pixel is implemented for better image optimization.
- Operating Modes
  The AR0144 works in master (video), trigger (single frame), or Auto Trigger modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two-wire serial interface for both modes.
- Window Control
  Configurable window size and blanking times allow a wide range of resolutions and frame rates. Digital binning and skipping modes are supported, as are vertical and horizontal mirror operations.
- Frame Rate:
  AR0144 is capable of running up to 60 fps at full (1280x800) resolution and 66 fps at 720p resolution.
- Embedded Data and Statistics
  The AR0144 has the capability to output image data and statistics embedded within the frame timing.
- Multi-Camera Synchronization
  The AR0144 supports advanced line synchronization controls for multi-camera (stereo) support.
- Slave Mode
  The slave mode feature of the AR0144 supports triggering the start of a frame readout from an input signal that is supplied from an external source. The slave mode signal allows for precise control of frame rate and register change updates.
- Context Switching and Register Updates
  Context switching may be used to rapidly switch between two sets of register values. Refer to the AR0144 Developer Guide for a complete description of context switchable registers.
- Gain
  A programmable analog gain of 1x to 16x applied globally to all color channels is available along with a digital gain of 1x to 16x that may be configured on a per color channel basis.
- Automatic Exposure Control
  The integrated automatic exposure control may be used to ensure optimal settings of exposure and gain are computed and updated every other frame. Refer to the AR0144 Developer Guide for more details.

- MIPI
  The AR0144 Global Shutter image sensor supports two lanes of MIPI data. Compliant to MIPI standards:
  – MIPI Alliance Standard for CSI-2 version 1.2
  – MIPI Alliance Standard for D-PHY version 1.0
- PLL
  An on chip PLL provides reference clock flexibility and supports spread spectrum sources for improved EMI performance.
- Reset
  The AR0144 may be reset by a register write, or by a dedicated input pin.
- Output Enable
  The AR0144 output pins may be tri-stated using a dedicated output enable pin.
- Temperature Sensor
- Black Level Correction
- Row Noise Correction
- Test Patterns
  Several test patterns may be enabled for debug purposes. These include a solid color, color bar, fade to gray, and a walking 1s test pattern.
- Silicon / OTPM Revision Information
  A revision register is provided to read out (via I2C) silicon and OTPM revision information. This will be helpful to distinguish material if there are future OTPM or silicon revisions.
- Lens Shading Correction
  A lens shading correction algorithm is included for potential low Z height applications.
- Compression
  AR0144 can optionally compress 12-bit data to 10-bit using A-law compression.

Pixel Data Format

Pixel Array Structure

The AR0144 pixel array is configured as 1484 columns by 856 rows, (see Figure 2). The dark pixels are optically black and are used internally to monitor black level. Of the left 180 columns, 168 are dark pixels used for row noise correction. Of the bottom 32 rows of pixels, 8 of the dark rows are used for black level correction. There are 1300 columns by 820 rows of optically active pixels. While the sensor's format is 1280 x 800, the additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for monochrome or color versions. The central 1288 x 808 pixel active area is surrounded with optically transparent dummy pixels and non-optically transparent barrier pixels to improve image uniformity within the active area. Not all barrier pixels can be read out. The optical center of the readable active pixels can be found between X_ADDR 649 and 650, and between Y_ADDR 409 and 410.

Figure 2: Pixel Array Description

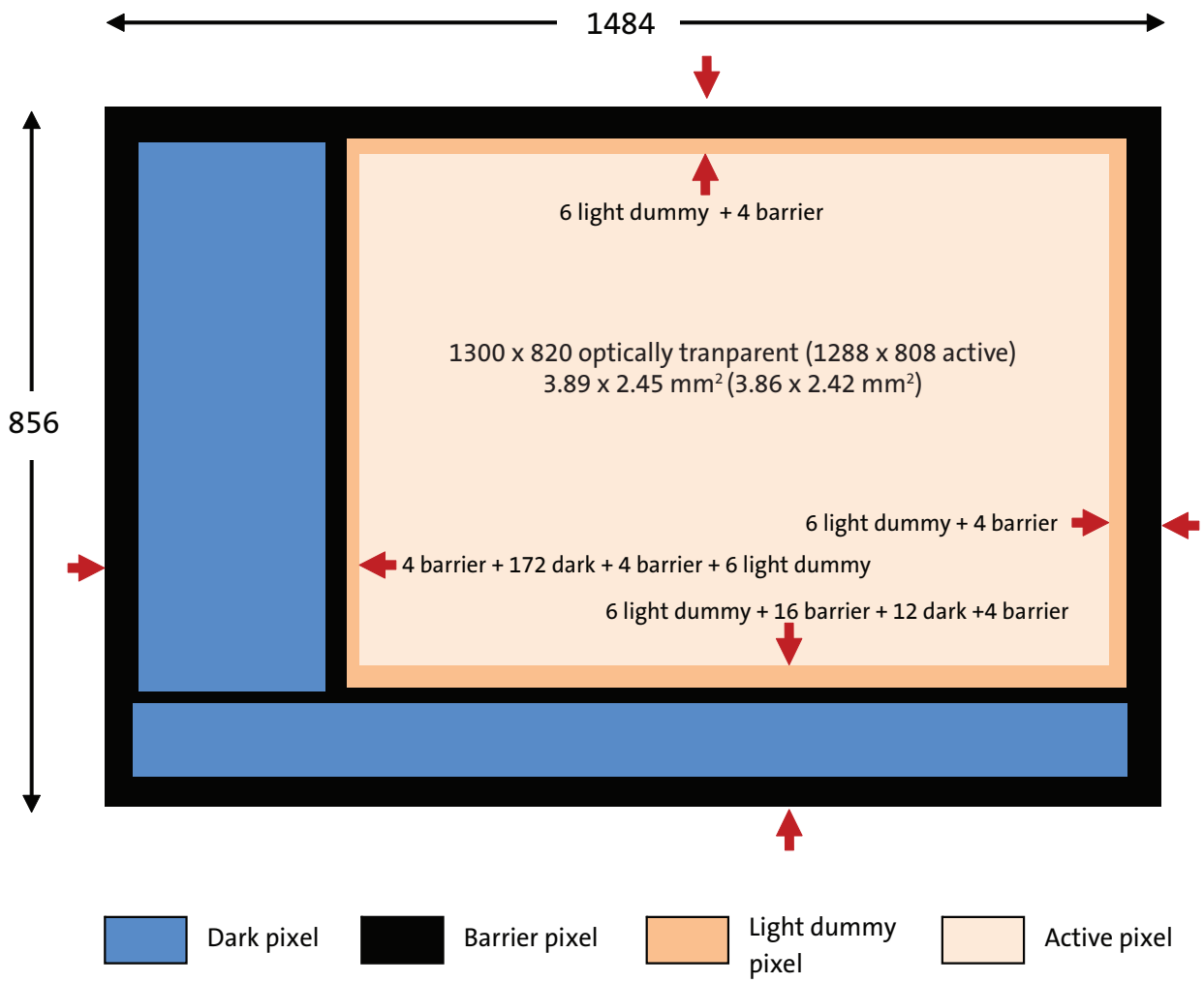
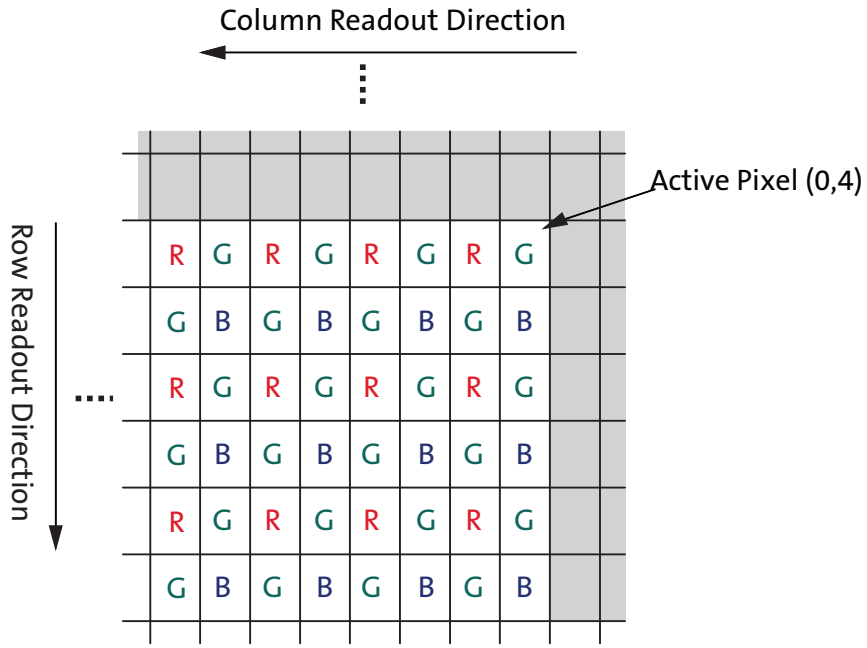


Figure 3: Pixel Color Pattern Detail (Top Right Corner)



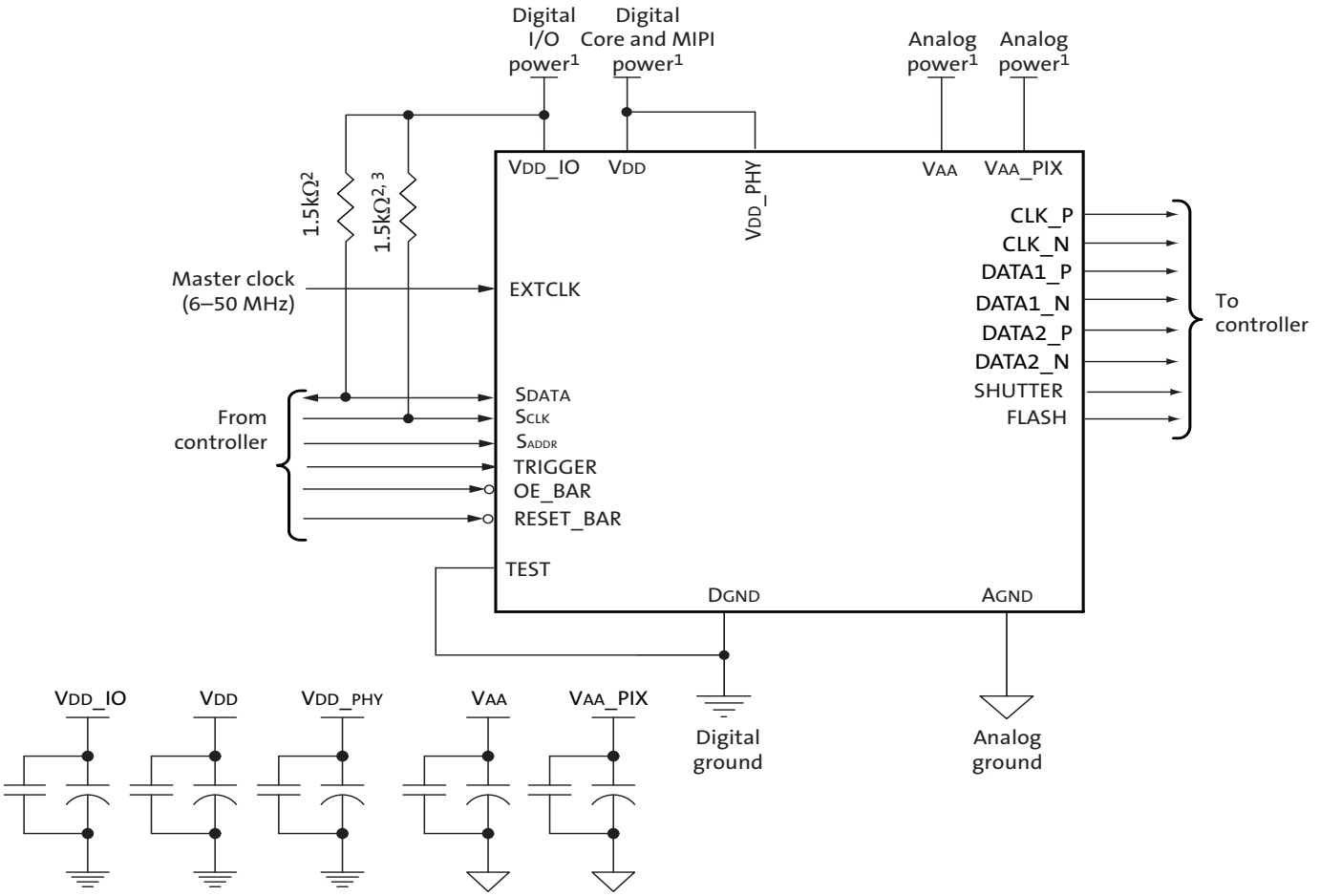
Default Readout Order

By convention, the sensor core pixel array is shown with the first addressable (logical) pixel (0,4) in the top right corner (see Figure 3). This reflects the actual layout of the array on the die. Also, the physical location of the first pixel data read out of the sensor in default condition is that of pixel (6,10).

Configuration and Pinout

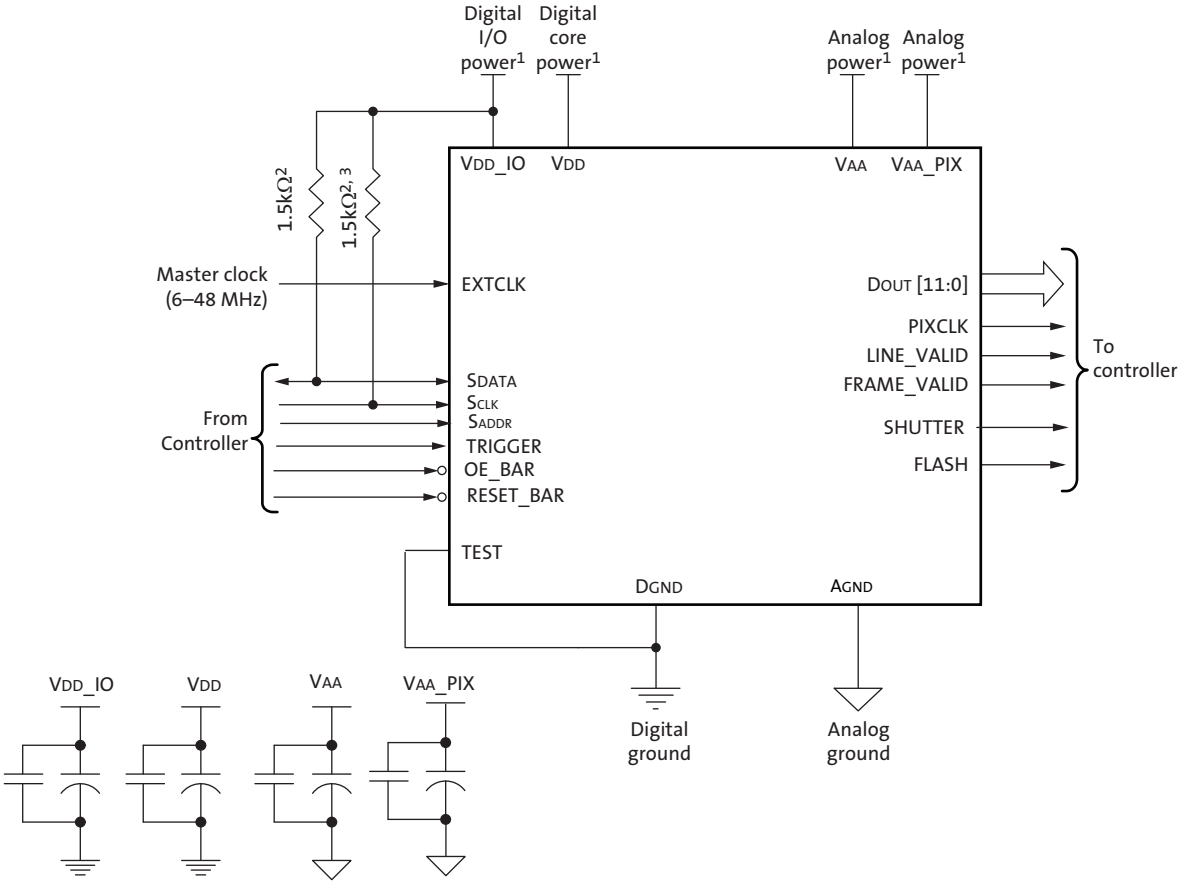
The figures and tables below show a typical configuration for the AR0144 image sensor and show the package pinouts.

Figure 4: Typical Configuration: Serial Two-Lane MIPI Interface



Notes:
1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5kΩ, but it may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. The parallel interface output pads can be left unconnected if the serial output interface is used.
5. ON Semiconductor recommends that 0.1µF and 10µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0144 demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.

Figure 5: Typical Configuration: Parallel Pixel Data Interface



Notes:
1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5kΩ, but it may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. The serial interface output pads can be left unconnected if the parallel output interface is used.
5. ON Semiconductor recommends that 0.1µF and 10µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0144 demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.

Table 3: 5.545 x 5.565 mm 69-ball CSP Ball Package

	1	2	3	4	5	6	7	8	9
A	DGND	VDD_IO	VDD	DATA2_P	CLK_P	DATA1_P	SHUTTER	TEST	
B	LINE_VALID	VDD	EXTCLK	DATA2_N	CLK_N	DATA1_N	SADDR	VDD_IO	
C	DOUT11	VDD_IO	PIXCLK	FRAME_VALID	VDD_PHY	VDD	SCLK	VDD_IO	
D	DOUT7	DOUT8	DOUT9	DOUT10	DGND	DGND	OE_BAR	VDD	AGND
E	DOUT5	DOUT6	VDD_IO	DOUT4	DOUT3	SDATA	TRIGGER	DGND	Reserved
F	DGND	VDD	DOUT2	DOUT1	DOUT0	FLASH	DGND	DGND	VAA_PIX
G	RESET_BAR	VAA	AGND	VDD	VDD	VDD	AGND	VAA	Reserved
H	VAA	VAA	AGND	DGND	DGND	DGND	AGND	VAA	VAA

Table 4: Pin Descriptions - 69-Ball CSP Package

Name	CSP Ball	Type	Description
DATA1_N	B6	Output	MIPI serial data, lane 1, differential N.
DATA1_P	A6	Output	MIPI serial data, lane 1, differential P.
DATA2_N	B4	Output	MIPI serial data, lane 2, differential N.
DATA2_P	A4	Output	MIPI serial data, lane 2, differential P.
CLK_N	B5	Output	MIPI serial clock differential N.
CLK_P	A5	Output	MIPI serial clock differential P.
VAA	G2, G8, H1, H2, H8, H9	Power	Analog power.
EXTCLK	B3	Input	External input clock.
VDD_PHY	C5	Power	MIPI power. (May leave unconnected if parallel interface is used)
DGND	A1, D5, D6, E8, F1, F7, F8, H4, H5, H6	Power	Digital GND.
VDD	A3, B2, C6, D8, F2, G4, G5, G6	Power	Digital power.
AGND	D9, G3, G7, H3, H7	Power	Analog GND.
SADDR	B7	Input	Two-Wire Serial address select.
SCLK	C7	Input	Two-Wire Serial clock input.
SDATA	E6	I/O	Two-Wire Serial data I/O.
VAA_PIX	F9	Power	Pixel power.
LINE_VALID	B1	Output	Asserted when DOUT line data is valid.
FRAME_VALID	C4	Output	Asserted when DOUT frame data is valid.
PIXCLK	C3	Output	Pixel clock out. DOUT is valid on rising edge of this clock.
SHUTTER	A7	Output	Control signal to drive external light sources.
FLASH	F6	Output	Control signal to drive external light sources.
VDD_IO	A2, B8, C2, C8, E3	Power	I/O supply power.
DOUT8	D2	Output	Parallel pixel data output.
DOUT9	D3	Output	Parallel pixel data output.
DOUT10	D4	Output	Parallel pixel data output.
DOUT11	C1	Output	Parallel pixel data output (MSB)
TEST	A8	Input	Manufacturing test enable pin (connect to DGND).
DOUT4	E4	Output	Parallel pixel data output.
DOUT5	E1	Output	Parallel pixel data output.
DOUT6	E2	Output	Parallel pixel data output.
DOUT7	D1	Output	Parallel pixel data output.
TRIGGER	E7	Input	Exposure synchronization input.
OE_BAR	D7	Input	Output enable (active LOW).
DOUT0	F5	Output	Parallel pixel data output (LSB)
DOUT1	F4	Output	Parallel pixel data output.
DOUT2	F3	Output	Parallel pixel data output.
DOUT3	E5	Output	Parallel pixel data output.
RESET_BAR	G1	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
Reserved	E9, G9	n/a	Reserved (do not connect).

Two-Wire Serial Register Interface

The two-wire serial interface bus enables read/write access to control and status registers within the AR0144.The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off-chip by a 1.5kΩ resistor. Either the slave or master device can drive SDATA LOW—the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two-wire serial interface specification allow the slave device to drive SCLK LOW; the AR0144 uses SCLK as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements:

1. a (repeated) start condition
2. a slave address/data direction byte
3. an (a no) acknowledge bit
4. a message byte
5. a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a WRITE, and a “1” indicates a READ. The default slave addresses used by the AR0144 are 0x20 (write address) and 0x21 (read address) in accordance with the specification. Alternate slave addresses of 0x30 (write address) and 0x31 (read address) can be selected by enabling and asserting the SADDR input.

An alternate slave address can also be programmed through R0x31FC.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No-Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a “0” indicates a write and a “1” indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

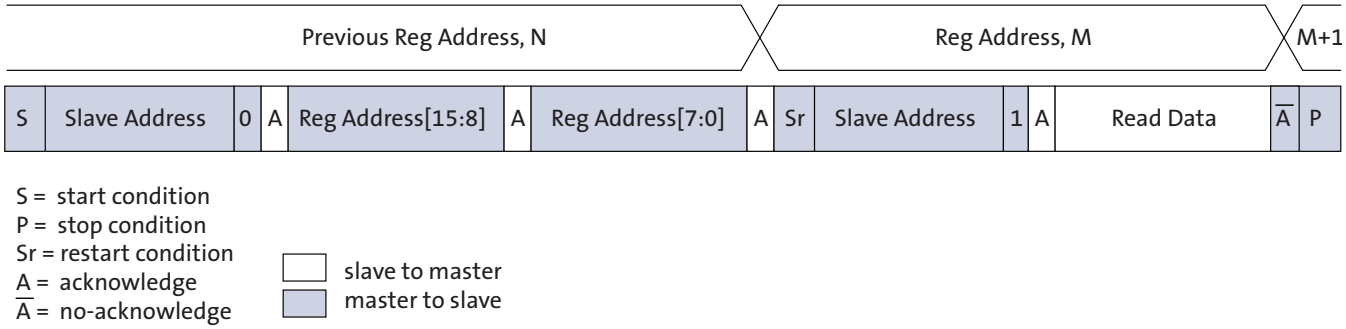
If the request was a WRITE, the master then transfers the 16-bit register address to which the WRITE should take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8-bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The slave’s internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Single READ from Random Location

This sequence (Figure 6 on page 15) starts with a dummy WRITE to the 16-bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8-bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. Figure 6 shows how the internal register address maintained by the AR0144 is loaded and incremented as the sequence proceeds.

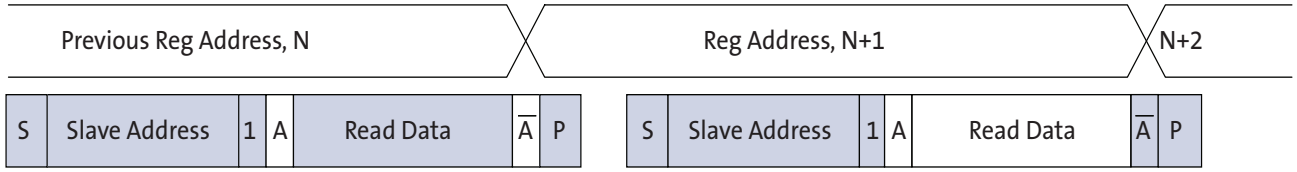
Figure 6: Single READ from Random Location



Single READ from Current Location

This sequence (Figure 7) performs a read using the current value of the AR0144 internal register address. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

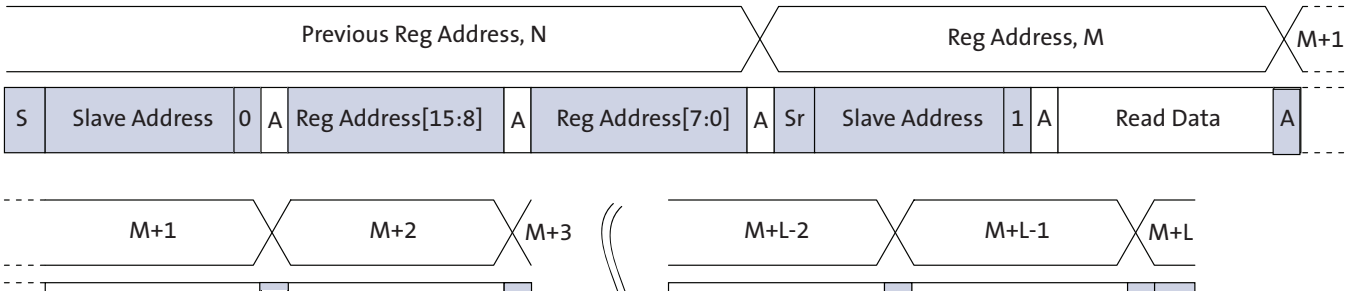
Figure 7: Single READ from Current Location



Sequential READ, Start from Random Location

This sequence (Figure 8) starts in the same way as the single READ from random location (Figure 6). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

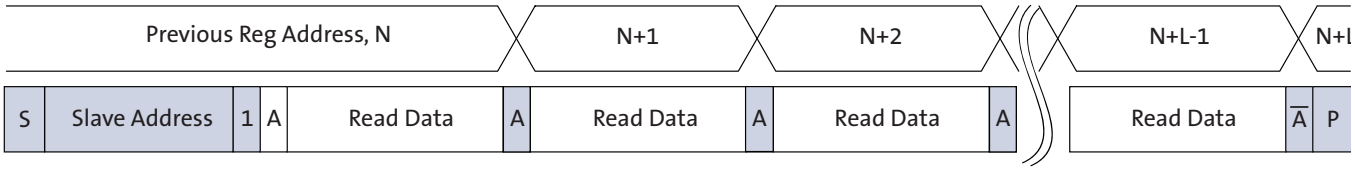
Figure 8: Sequential READ, Start from Random Location



Sequential READ, Start from Current Location

This sequence (Figure 9) starts in the same way as the single READ from current location (Figure 7 on page 15). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

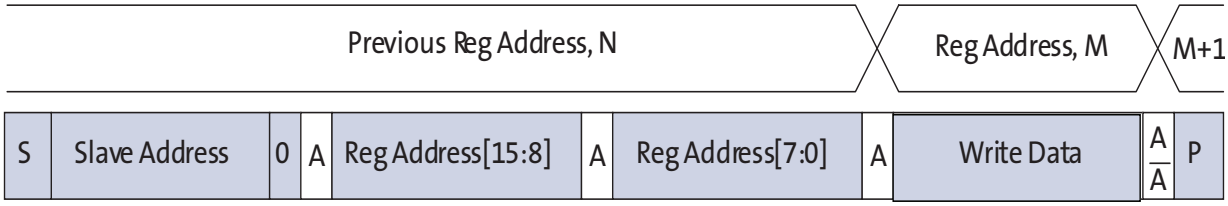
Figure 9: Sequential READ, Start from Current Location



Single WRITE to Random Location

This sequence (Figure 10) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

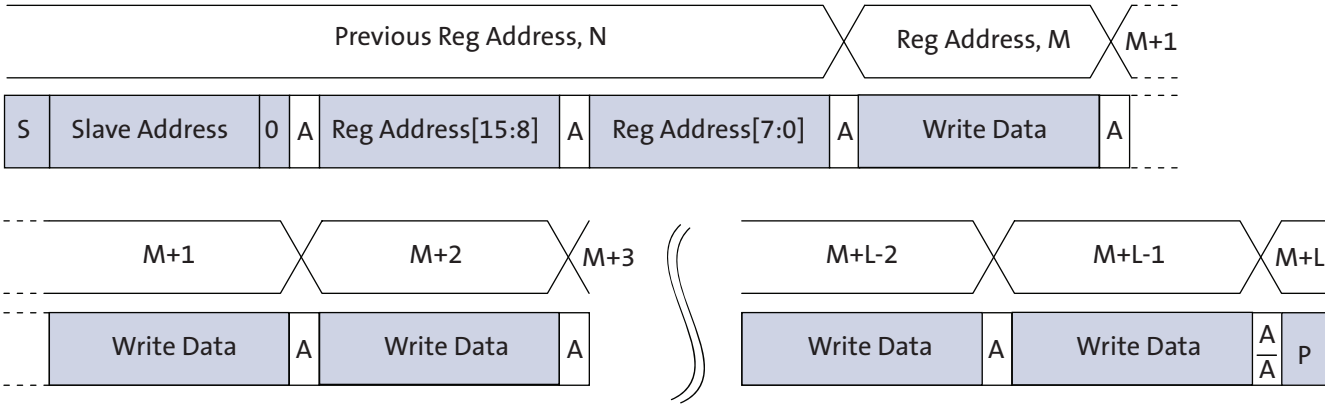
Figure 10: Single WRITE to Random Location



Sequential WRITE, Start at Random Location

This sequence (Figure 11) starts in the same way as the single WRITE to random location (Figure 10). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

Figure 11: Sequential WRITE, Start at Random Location



Electrical Specifications

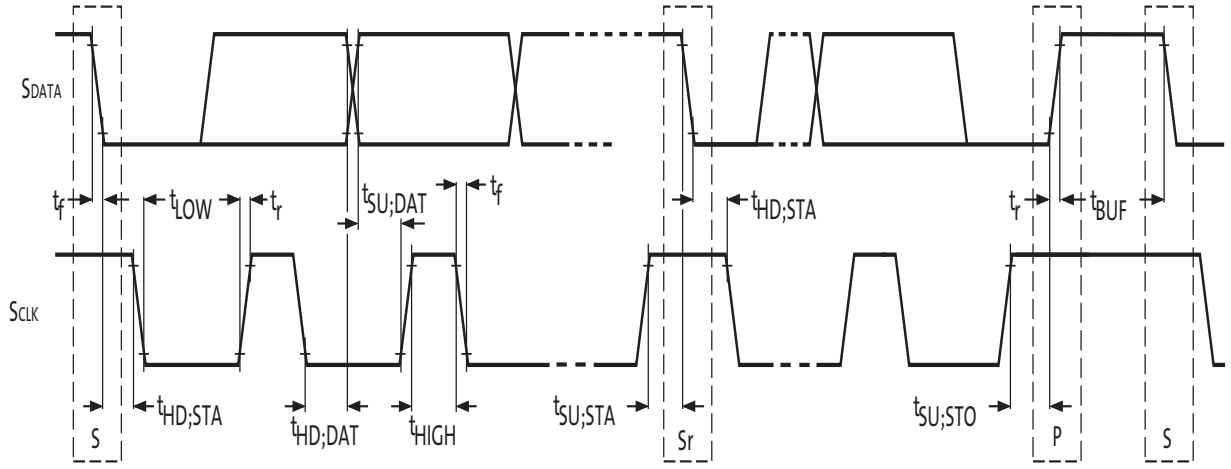
Unless otherwise stated, the following specifications apply to the following conditions:

VDD = VDD_PHY = 1.2V ±0.06; VDD_IO = VAA = VAA_PIX = 2.8V ± 0.3V;
T_A = -40°C to +105°C; output load = 10pF; PIXCLK frequency = 74.25 MHz; MIPI off.

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 12 and Table 5.

Figure 12: Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Table 5: Two-Wire Serial Bus Characteristics

[f]EXTCLK = 27 MHz; VDD = 1.2V; VDD_IO = 2.8V; VAA = 2.8V; VAA_PIX = 2.8V; VDD_PHY = 1.2V; T_A = 25°C

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	f_{SCL}	0	100	0	400	KHz
Hold time (repeated) START condition.						
After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	µS
LOW period of the SCLK clock	t_{LOW}	4.7	-	1.3	-	µS
HIGH period of the SCLK clock	t_{HIGH}	4.0	-	0.6	-	µS
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µS
Data hold time:	$t_{HD;DAT}$	0[4]	3.45[5]	0[6]	0.9[5]	µS
Data set-up time	$t_{SU;DAT}$	250	-	100[6]	-	nS
Rise time of both SDATA and SCLK signals	t_r	-	1000	20 + 0.1Cb[7]	300	nS
Fall time of both SDATA and SCLK signals	t_f	-	300	20 + 0.1Cb[7]	300	nS
Set-up time for STOP condition	$tS_{U;STO}$	4.0	-	0.6	-	µS

Table 5: Two-Wire Serial Bus Characteristics

^{f}EXTCLK = 27 MHz; V_{DD} = 1.2V; V_{DD}_IO = 2.8V; V_{AA} = 2.8V; V_{AA}_PIX = 2.8V; V_{DD}_PHY = 1.2V; T_A = 25°C

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µS
Capacitive load for each bus line	Cb	-	400	-	400	pF
Serial interface input pin capacitance	C_{IN_SI}	-	3.3	-	3.3	pF
SDATA max load capacitance	C_{LOAD_SD}	-	30	-	30	pF
SDATA pull-up resistor	RSD	1.5	4.7	1.5	4.7	KΩ

Notes:
1. This table is based on I^{2}C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I^{2}C-compatible.
3. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1V_{DD} levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
5. The maximum ^{t}HD;DAT has only to be met if the device does not stretch the LOW period (^{t}LOW) of the SCLK signal.
6. A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system, but the requirement ^{t}SU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line ^{t}r max + ^{t}SU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCLK line is released.
7. Cb = total capacitance of one bus line in pF.

I/O Timing

By default, the AR0144 launches pixel data, FV and LV with the falling edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV and LV using the rising edge of PIXCLK. The launch edge of PIXCLK can be configured in register R0x3028. See Figure 13 and Table 6 for I/O timing (AC) characteristics.

Figure 13: I/O Timing Diagram

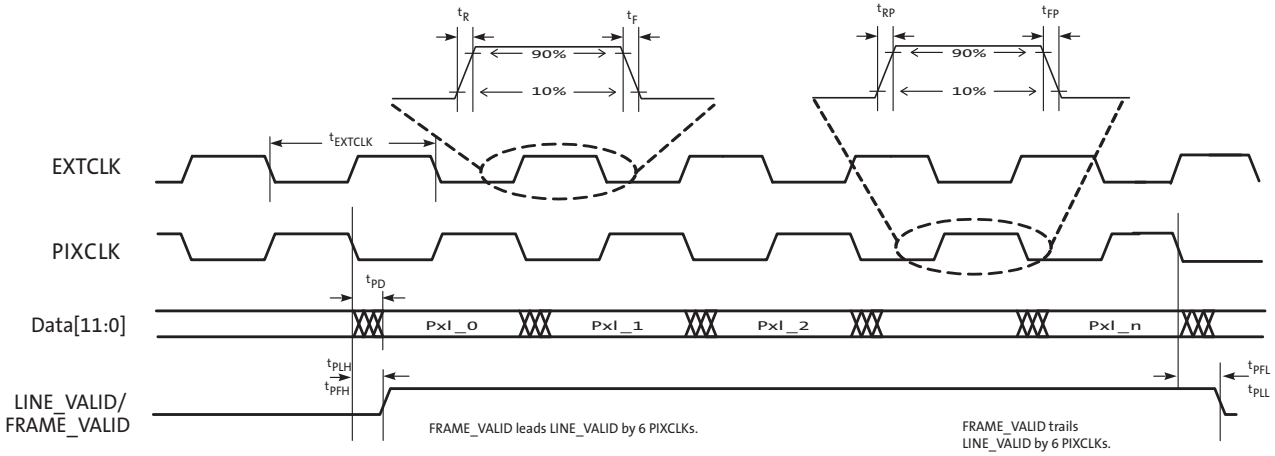


Table 6: I/O Timing Characteristics, Parallel Output (1.8V V_{DD_IO})[1]

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_{EXTCLK}	Input clock frequency		6		48	MHz
t_{EXTCLK}	Input clock period		20.8		166	ns
t_R	Input clock rise time	PLL enabled		3		ns
t_F	Input clock fall time	PLL enabled		3		ns
t_{JITTER}	Input clock jitter				600	ns
t_{cp}	EXTCLK to PIXCLK propagation delay	Nominal voltages, PLL disabled, PIXCLK slew rate = 4	5.7		14.3	ns
t_{RP}	PIXCLK rise time	PCLK slew rate = 6	1.3		4.0	ns
t_{FP}	PIXCLK fall time	PCLK slew rate = 6	1.3		3.9	ns
	PIXCLK duty cycle		45	50	55	%
f_{PIXCLK}	PIXCLK frequency	PIXCLK slew rate = 6, Data slew rate = 7	6		74.25	MHz
t_{PD}	PIXCLK to data valid	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PFH}	PIXCLK to FV HIGH	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PLH}	PIXCLK to LV HIGH	PIXCLK slew rate = 6, Data slew rate = 7	-3		1.5	ns
t_{PFL}	PIXCLK to FV LOW	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PLL}	PIXCLK to LV LOW	PIXCLK slew rate = 6, Data slew rate = 7	-3		1.5	ns
C_{IN}	Input pin capacitance			2.5		pf

Notes: 1. Minimum and maximum values are taken at 125°C junction, 2.5V and -40°C junction, 3.1V. All values are taken at the 50% transition point. The loading used is 10 pF.
2. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

Table 7: I/O Timing Characteristics, Parallel Output (2.8V V_{DD}_IO)[1]

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_{EXTCLK}	Input clock frequency		6		48	MHz
t_{EXTCLK}	Input clock period		20.8		166	ns
t_R	Input clock rise time	PLL enabled		3		ns
t_F	Input clock fall time	PLL enabled		3		ns
$t_{jJITTER}$	Input clock jitter				600	ns
t_{cp}	EXTCLK to PIXCLK propagation delay	Nominal voltages, PLL disabled, PIXCLK slew rate = 4	5.3		13.4	ns
t_{RP}	PIXCLK rise time	PCLK slew rate = 6	1.3		4.0	ns
t_{FP}	PIXCLK fall time	PCLK slew rate = 6	1.3		3.9	ns
	PIXCLK duty cycle		45	50	55	%
f_{PIXCLK}	PIXCLK frequency	PIXCLK slew rate = 6, Data slew rate = 7	6		74.25	MHz
t_{PD}	PIXCLK to data valid	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PFH}	PIXCLK to FV HIGH	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PLH}	PIXCLK to LV HIGH	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PFL}	PIXCLK to FV LOW	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PLL}	PIXCLK to LV LOW	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
C_{IN}	Input pin capacitance			2.5		pf

Notes: 1. Minimum and maximum values are taken at 125°C junction, 2.5V and -40°C junction, 3.1V. All values are taken at the 50% transition point. The loading used is 10 pF.
2. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

Table 8: I/O Rise Slew Rate (2.8V V_{DD}_IO)[1]

Parallel Slew Rate (R0x306E[15:13])	Min	Typ	Max	Units
0	1.02	1.76	2.52	V/ns
1	1.2	2.05	3.14	V/ns
2	1.35	2.38	3.52	V/ns
3	1.57	2.72	4	V/ns
4	1.76	2.9	4.49	V/ns
5	1.87	3.16	4.88	V/ns
6	2.07	3.5	5.35	V/ns
7	2.22	3.75	5.77	V/ns

Note: 1. Minimum and maximum values are taken at 125°C junction, 2.5V and -40°C junction, 3.1V. The loading used is 10 pF.

Table 9: I/O Fall Slew Rate (2.8V V_{DD}_IO)[1]

Parallel Slew Rate (R0x306E[15:13])	Min	Typ	Max	Units
0	0.8	1.33	2.01	V/ns
1	1.05	1.71	2.51	V/ns
2	1.28	2.14	3.07	V/ns
3	1.49	2.49	3.53	V/ns
4	1.64	2.75	4.05	V/ns
5	1.83	3.06	4.54	V/ns
6	2.01	3.38	4.86	V/ns
7	2.17	3.63	5.32	V/ns

Note: 1. Minimum and maximum values are taken at 125°C junction, 2.5V and -40°C junction, 3.1V. The loading used is 10 pF.

Table 10: I/O Rise Slew Rate (1.8V V_{DD}_IO)[1]

Parallel Slew Rate (R0x306E[15:13])	Min	Typ	Max	Units
0	0.386	0.61	1.05	V/ns
1	0.459	0.727	1.24	V/ns
2	0.528	0.849	1.41	V/ns
3	0.595	0.944	1.59	V/ns
4	0.662	1.06	1.77	V/ns
5	0.728	1.14	1.94	V/ns
6	0.792	1.26	2.11	V/ns
7	0.855	1.38	2.27	V/ns

Note: 1. Minimum and maximum values are taken at 125°C junction,1.7V and -40°C junction, 1.95V. The loading used is 10 pF.

Table 11: I/O Fall Slew Rate (1.8V V_{DD}_IO)[1]

Parallel Slew Rate (R0x306E[15:13])	Min	Typ	Max	Units
0	0.33	0.546	0.888	V/ns
1	0.43	0.713	1.16	V/ns
2	0.51	0.853	1.41	V/ns
3	0.6	1.02	1.64	V/ns
4	0.7	1.15	1.86	V/ns
5	0.77	1.3	2.04	V/ns
6	0.86	1.41	2.26	V/ns
7	0.94	1.51	2.43	V/ns

Notes: 1. Minimum and maximum values are taken at 125°C junction,1.7V and -40°C junction, 1.95V. The loading used is 10 pF.

DC Electrical Characteristics

The DC electrical characteristics are shown in Table 12, Table 13, Table 14, and Table 16.

Table 12: DC Electrical Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core digital voltage		1.14	1.2	1.26	V
V_{DD_IO}	I/O digital voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
V_{AA}	Analog voltage		2.5	2.8	3.1	V
V_{AA_PIX}	Pixel supply voltage		2.5	2.8	3.1	V
V_{DD_PHY}	MIPI supply voltage		1.14	1.2	1.26	V
V_{IH}	Input HIGH voltage		V_{DD_IO} * 0.7	–	–	V
V_{IL}	Input LOW voltage		–	–	V_{DD_IO} * 0.3	V
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{DD_IO} or D_{GND}	20	–	–	µA
V_{OH}	Output HIGH voltage		V_{DD_IO} – 0.3	–	–	V
V_{OL}	Output LOW voltage	V_{DD_IO} = 2.8V	–	–	0.4	V
I_{OH}	Output HIGH current	At specified V_{OH}	–22	–	–	mA
I_{OL}	Output LOW current	At specified V_{OL}	–	–	22	mA

Caution **Stresses greater than those listed in Table 13 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.**

Table 13: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Symbol
V_{SUPPLY}	Power supply voltage (all supplies)	–0.3	4.5	V	V_{SUPPLY}
I_{SUPPLY}	Total power supply current	–	200	mA	I_{SUPPLY}
I_{GND}	Total ground current	–	200	mA	I_{GND}
V_{IN}	DC input voltage	–0.3	V_{DD_IO} + 0.3	V	V_{IN}
V_{OUT}	DC output voltage	–0.3	V_{DD_IO} + 0.3	V	V_{OUT}
T_{STG}[1]	Storage temperature	–40	+125	°C	T_{STG}[1]

Note: 1. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 14: Operating Current Consumption for Parallel Output
V_{AA} = V_{AA_PIX} = V_{DD_IO} = 2.8V; V_{DD}= V_{DD_PHY} = 1.2V;PLL Enabled and PIXCLK = 74.25 MHz; T_A = 55°C; C_{LOAD} = 10pF

	Condition	Symbol	Min	Typ	Max	Unit
Digital operating current	Parallel, Streaming, Full resolution 60 fps	I_{DD}				mA
I/O digital operating current	Parallel, Streaming, Full resolution 60 fps	I_{DD_IO}				mA
Analog operating current	Parallel, Streaming, Full resolution 60 fps	I_{AA}				mA
Pixel supply current	Parallel, Streaming, Full resolution 60 fps	I_{AA_PIX}				mA
PLL supply current	Parallel, Streaming, Full resolution 60 fps	I_{DD_PLL}				mA

Table 15: Operating Current Consumption for MIPI Output

V_{AA} = V_{AA_PIX} = V_{DD_IO} = 2.8V; V_{DD}= V_{DD_PHY} = 1.2V;PLL Enabled and PIXCLK = 74.25 MHz; T_A = 55°C; C_{LOAD} = 10pF

	Condition	Symbol	Min	Typ	Max	Unit
Digital operating current	MIPI, Streaming, Full resolution 60 fps	I_{DD}				mA
I/O digital operating current	MIPI, Streaming, Full resolution 60 fps	I_{DD_IO}				mA
Analog operating current	MIPI, Streaming, Full resolution 60 fps	I_{AA}				mA
Pixel supply current	MIPI, Streaming, Full resolution 60 fps	I_{AA_PIX}				mA
PLL supply current	MIPI, Streaming, Full resolution 60 fps	I_{DD_PLL}				mA
PHY supply current	MIPI, Streaming, Full resolution 60fps	I_{DD_PHY}				mA

Table 16: Standby Current Consumption

Analog - V_{AA} + V_{AA_PIX}; Digital - V_{DD} + V_{DD_PHY}; T_A = 55°C

Definition	Condition	Min	Typ	Max	Unit
Soft standby (clock off, driven low)	Analog, 2.8V				µA
	Digital, 1.2V				µA
	V_{DD_IO}, 2.8V				mA
Soft standby (clock on, EXTCLK = 20 MHz)	Analog, 2.8V				µA
	Digital, 1.2V				mA
	V_{DD_IO}, 2.8V				mA
Hard reset (clock off, driven low)	Analog, 2.8V				µA
	Digital, 1.2V				µA
	V_{DD_IO}, 2.8V				mA
Hard reset (clock on, EXTCLK = 20 MHz)	Analog, 2.8V				µA
	Digital, 1.2V				µA
	Analog, 2.8V				mA

Power-On Reset Timing

Power-Up Sequence

The recommended power-up sequence for the AR0144 is shown in Figure 14. The available power supplies (VDD_IO, VDD, VDD_SLVS, VAA, VAA_PIX) must have the separation specified below.

1. Turn on VAA and VAA_PIX power supply.
2. After 0–10µs, turn on VDD_IO power supply.
3. After 0–10µs, turn on VDD_PHY and VDD power supplies.
4. After the last power supply is stable, enable EXTCLK.
5. If RESET_BAR is in a LOW state, hold RESET_BAR LOW for at least 1ms.
   If RESET_BAR is in a HIGH state, assert RESET_BAR for at least 1ms.
6. Wait 160000 EXTCLKs (for internal initialization into software standby).
7. Configure PLL, output, and image settings to desired values.
8. Wait 1ms for the PLL to lock.
9. Set streaming mode (R0x301a[2] = 1).

Figure 14: Power Up

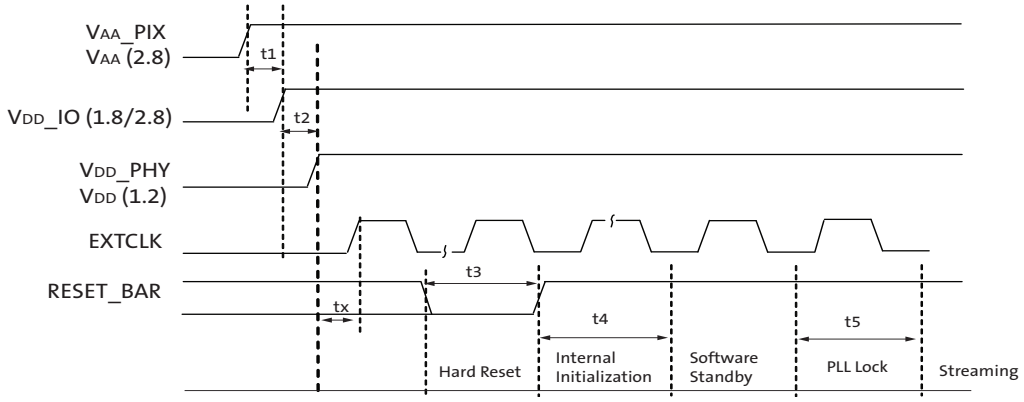


Table 17: Power-Up Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
VAA/VAA_PIX to VDD_IO	t1	0	10	–	µs
VDD_IO to VDD/VDD_PHY	t2	0	10	–	µs
Xtal settle time	tx	–	30[1]	–	ms
Hard Reset	t3	1[2]	–	–	ms
Internal Initialization	t4	160000	–	–	EXTCLKs
PLL Lock Time	t5	1	–	–	ms

Notes:
1. Xtal settling time is component-dependent, usually taking about 10 – 100 ms.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.

Power-Down Sequence

The recommended power-down sequence for the AR0144 is shown in Figure 15. The available power supplies (VDD_IO, VDD, VDD_SLVS, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off VDD_PHY/VDD.
4. Turn off VDD_IO
5. Turn off VAA/VAA_PIX.

Figure 15: Power Down

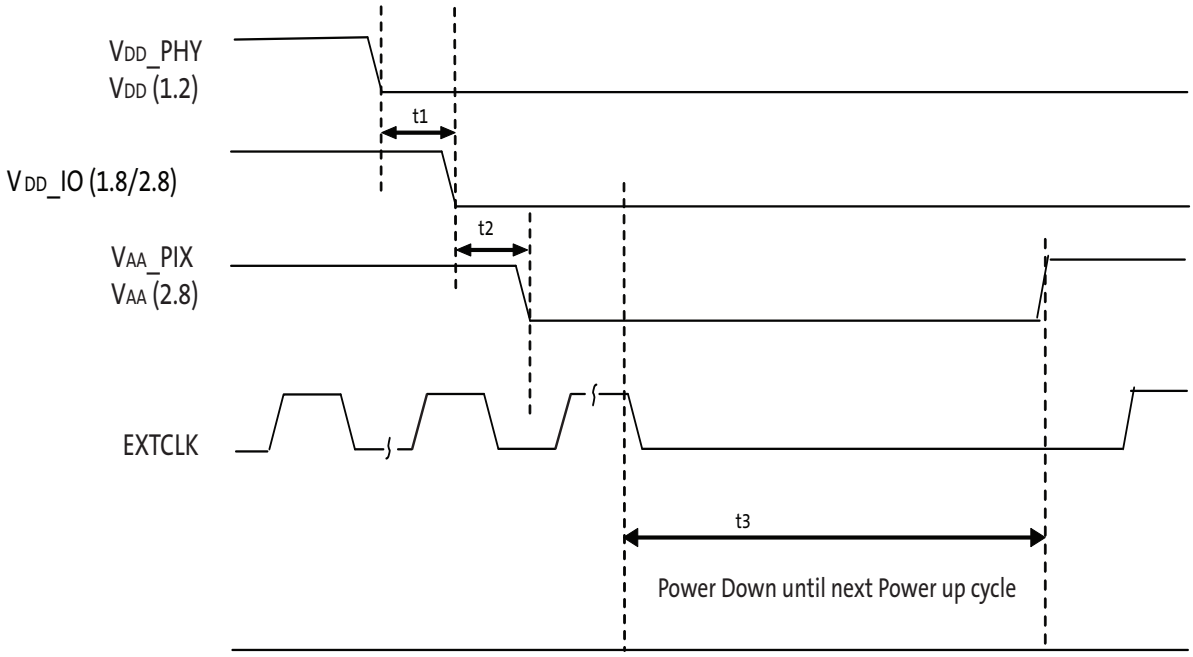


Table 18: Power-Down Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PHY / VDD to VDD_IO	t1	0	–	–	µs
VDD_IO to VAA/VAA_PIX	t2	0	–	–	µs
PwrDn until Next PwrUp Time	t3	100	–	–	ms

Note: t3 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

Figure 16: Quantum Efficiency – Monochrome Sensor (Typical)

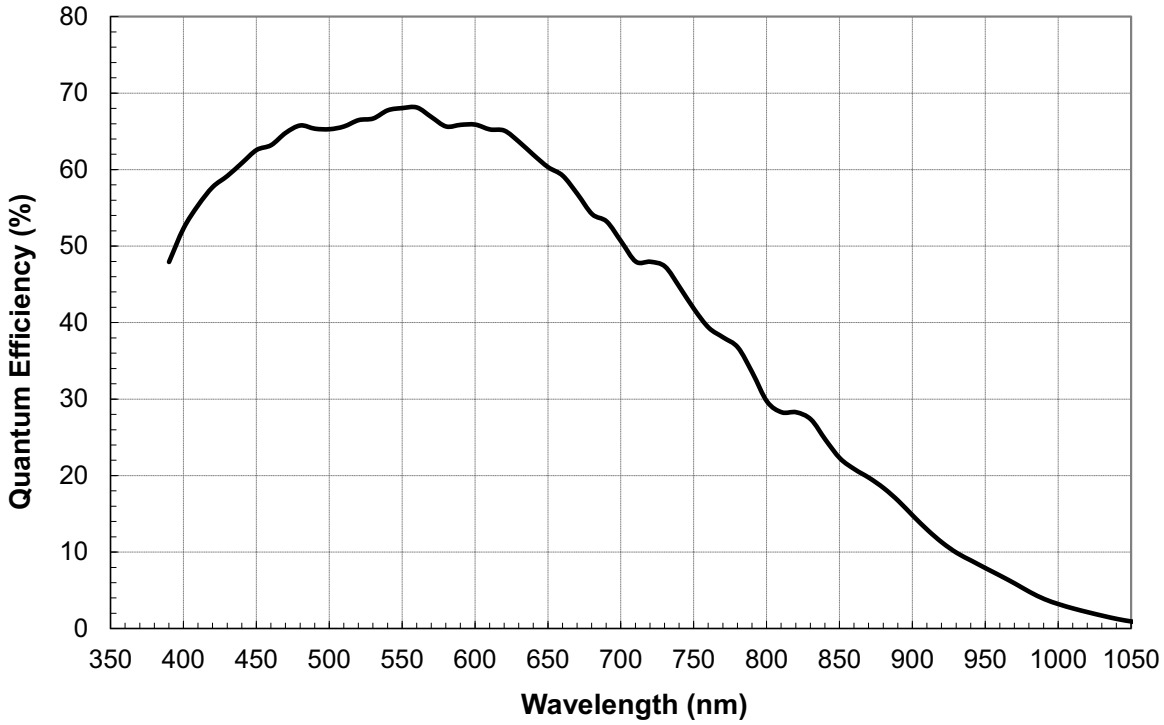


Figure 17: Quantum Efficiency – Color Sensor (Typical)

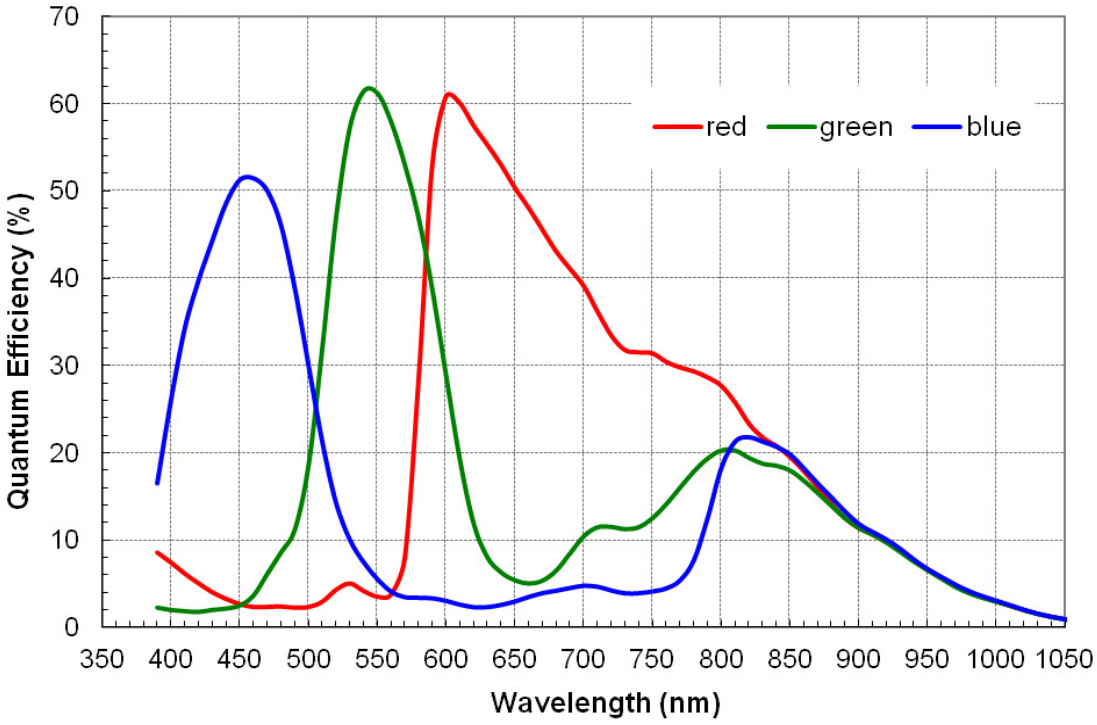


Table 19: Chief Ray Angle - 20deg

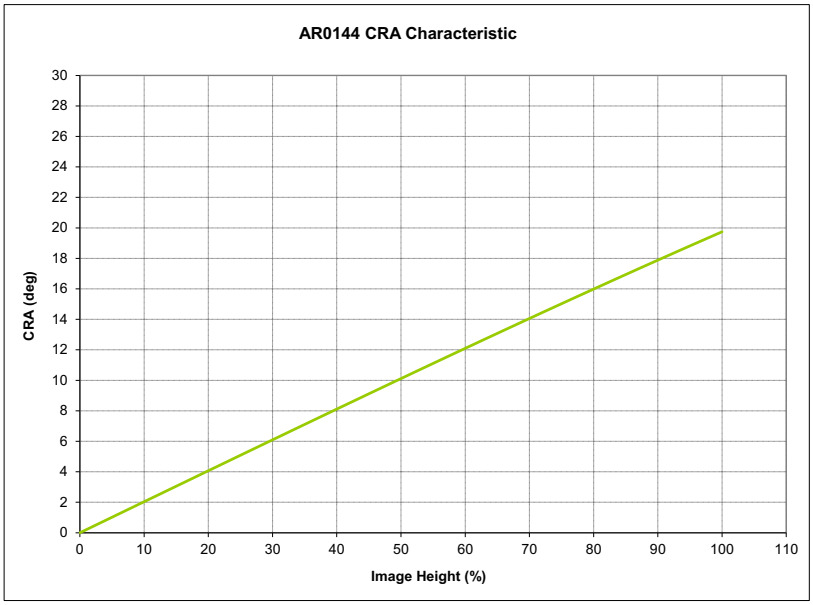
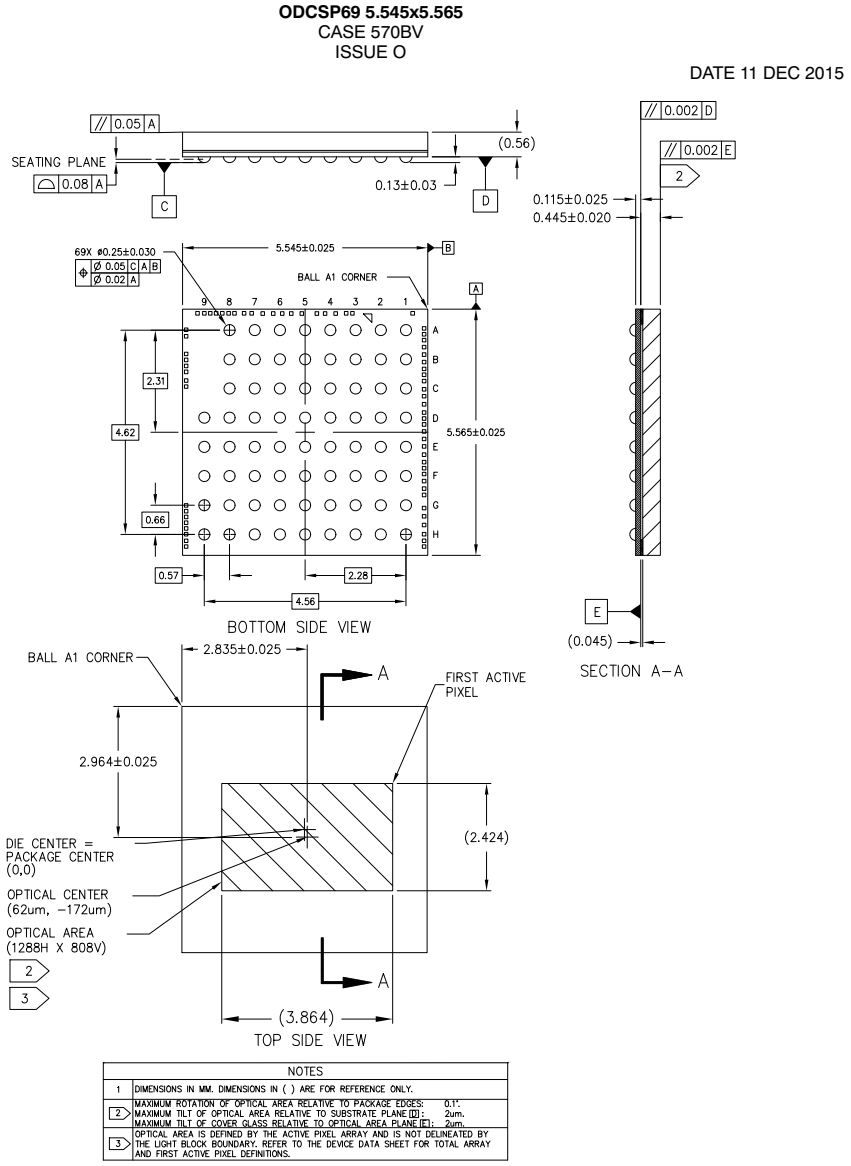


Image Height		CRA
(%)	(mm)	(deg)
0	0	0
5	0.113	1.02
10	0.226	2.03
15	0.340	3.05
20	0.453	4.07
25	0.566	5.08
30	0.679	6.10
35	0.792	7.10
40	0.906	8.11
45	1.019	9.11
50	1.132	10.11
55	1.245	11.11
60	1.358	12.10
65	1.472	13.08
70	1.585	14.05
75	1.698	15.02
80	1.811	15.98
85	1.925	16.94
90	2.038	17.88
95	2.151	18.82
100	2.264	19.74

Package Dimensions

Figure 18: 69-Ball CSP Package Outline Drawing



Notes: 4. Lid material: Borosilicate glass 0.4 thickness. Refractive index at 20C = 1.5255 @ 546 nm and 1.5231 @ 588 nm. Double side AR Coating: 530-570 nm R< 1%; 420-700 nm R < 2%.

5. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).